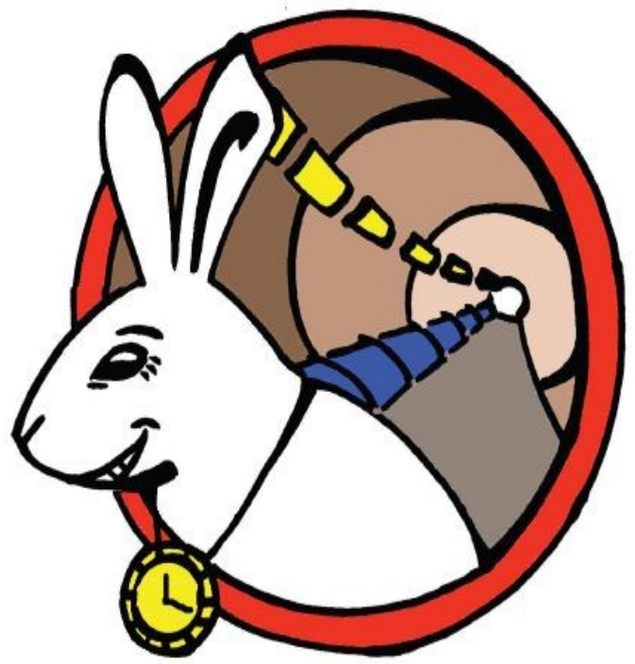
Laboratoire de Physique des 2 infinis Irène Joliot-Curie

l'Observatoire de Paris | SYRTE

Systèmes de Référence Temps-Espace



IDROGEN system

Antoine Back, Olivier Bourrion, Chafik Cheikali, **Daniel Charlet**, Eric Plaige, Paul-Eric Pottie, Monique Taurigna, Cédric Viou

cnrs

Nancay June 2023

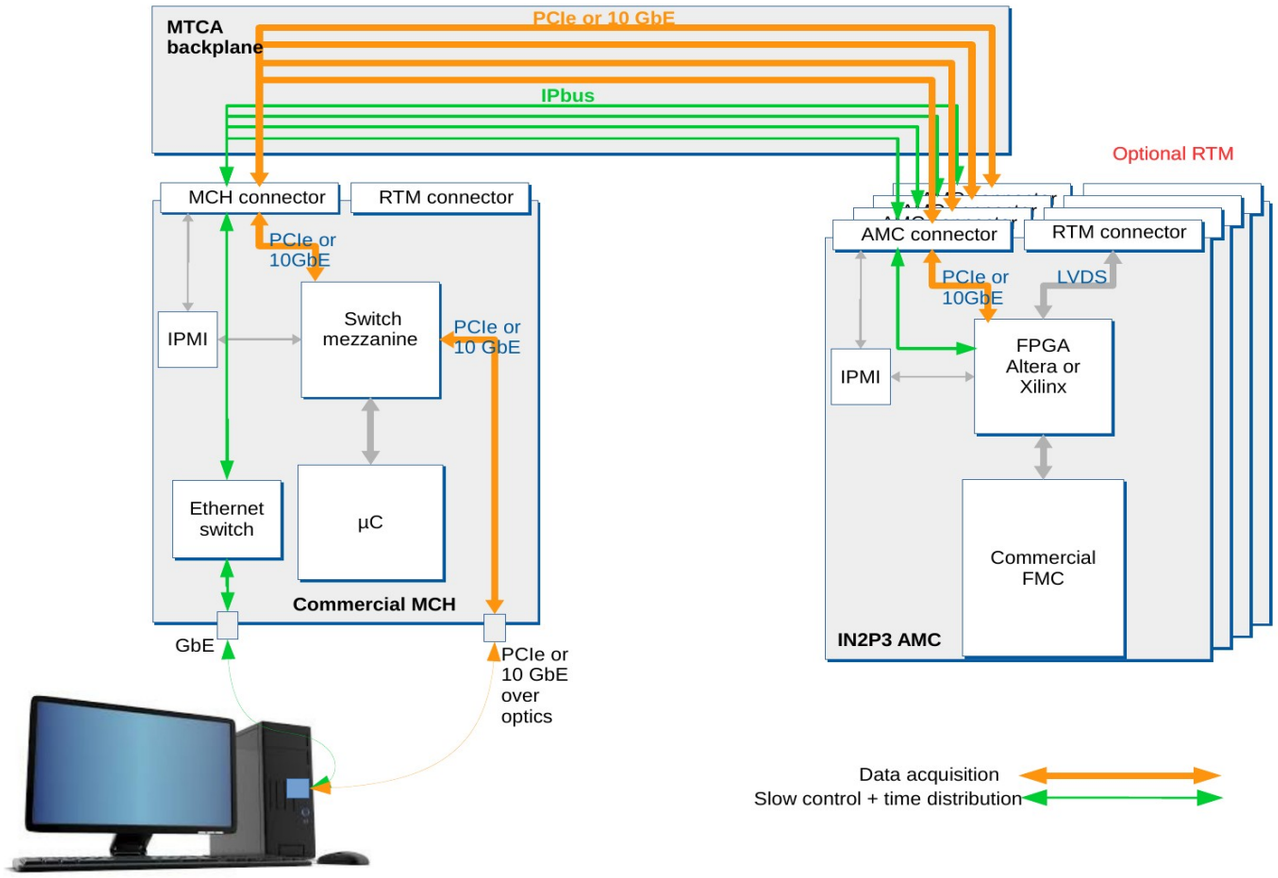
Station de Radioastronomie de Nançay

Outline

- IDROGEN system
  - Hardware_Firmware
- FMC mezzanine board
- Trigger-less acquisition system : New-COMET

IDROGEN board

Acquisition system : DAQGEN

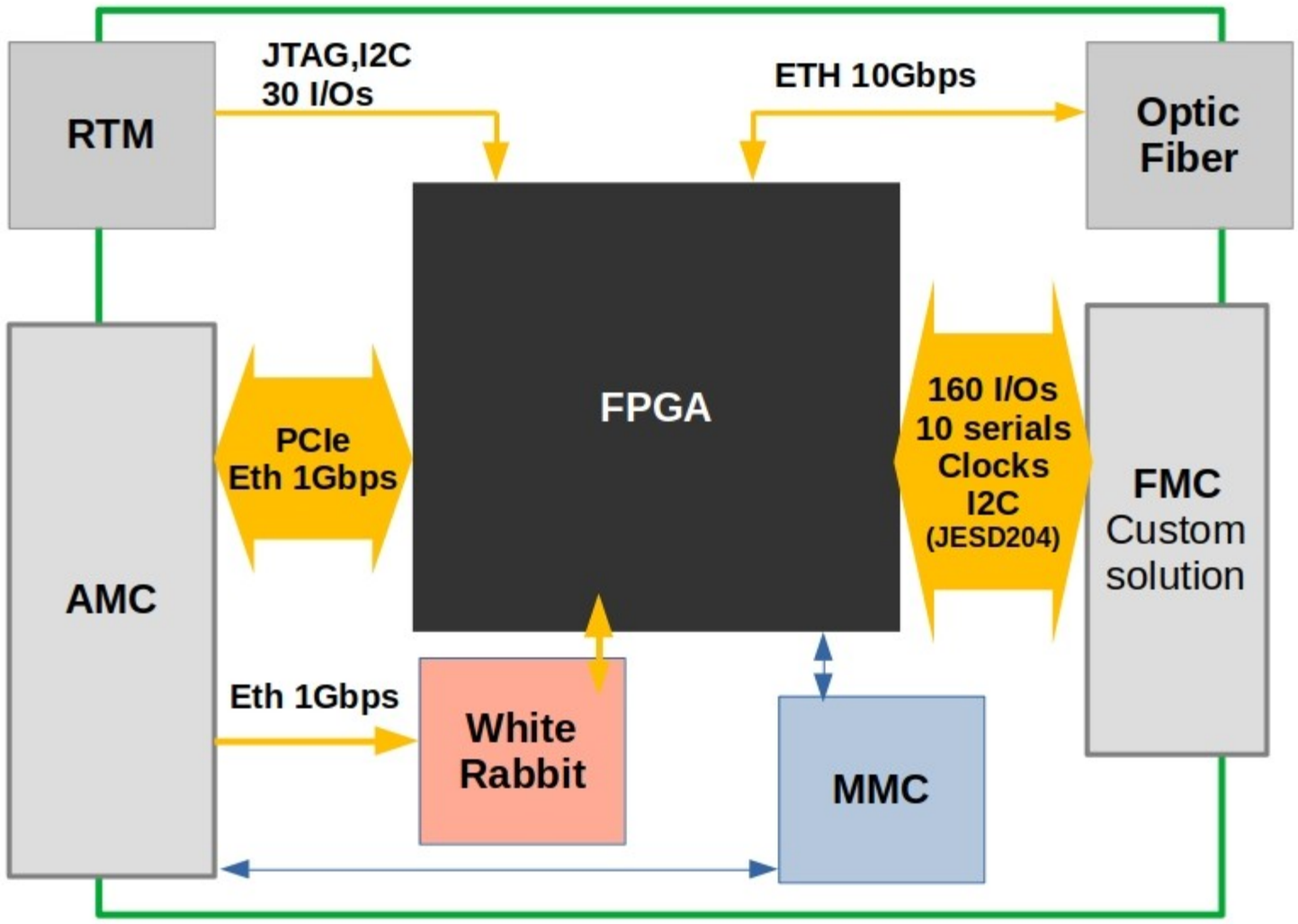


- Standard : xTCA for Physic
- Based on an off the shelf system
- Crate controler : MCH fron N.A.T
- Data read-out :
  - Backplane : PCIe 4x gen 3 / ETH 1G/10G
  - Front-side : ETH1G/10G , 2x 10G
- Board configuration Ipbus : ETH0 or SFP+
- Synchronisation : WR

- 2 boards in developement :
  - IDROGEN
  - base on INTELFPGA (IJCLAB)
  - OXIGEN (LPSC
  - Base on XILINX

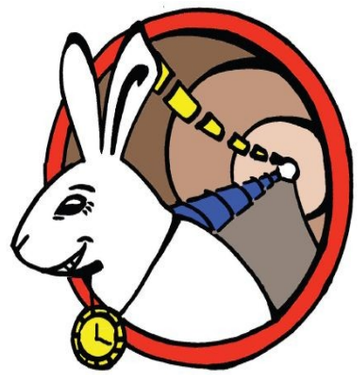
OXIGEN board

- XTCA board : LPSC development (Julien Bunmy)
  - Base on XILXINX FPGA
  - Base on IDROGEN
  - FMC carrier board
  - WR node
  - Currently in test

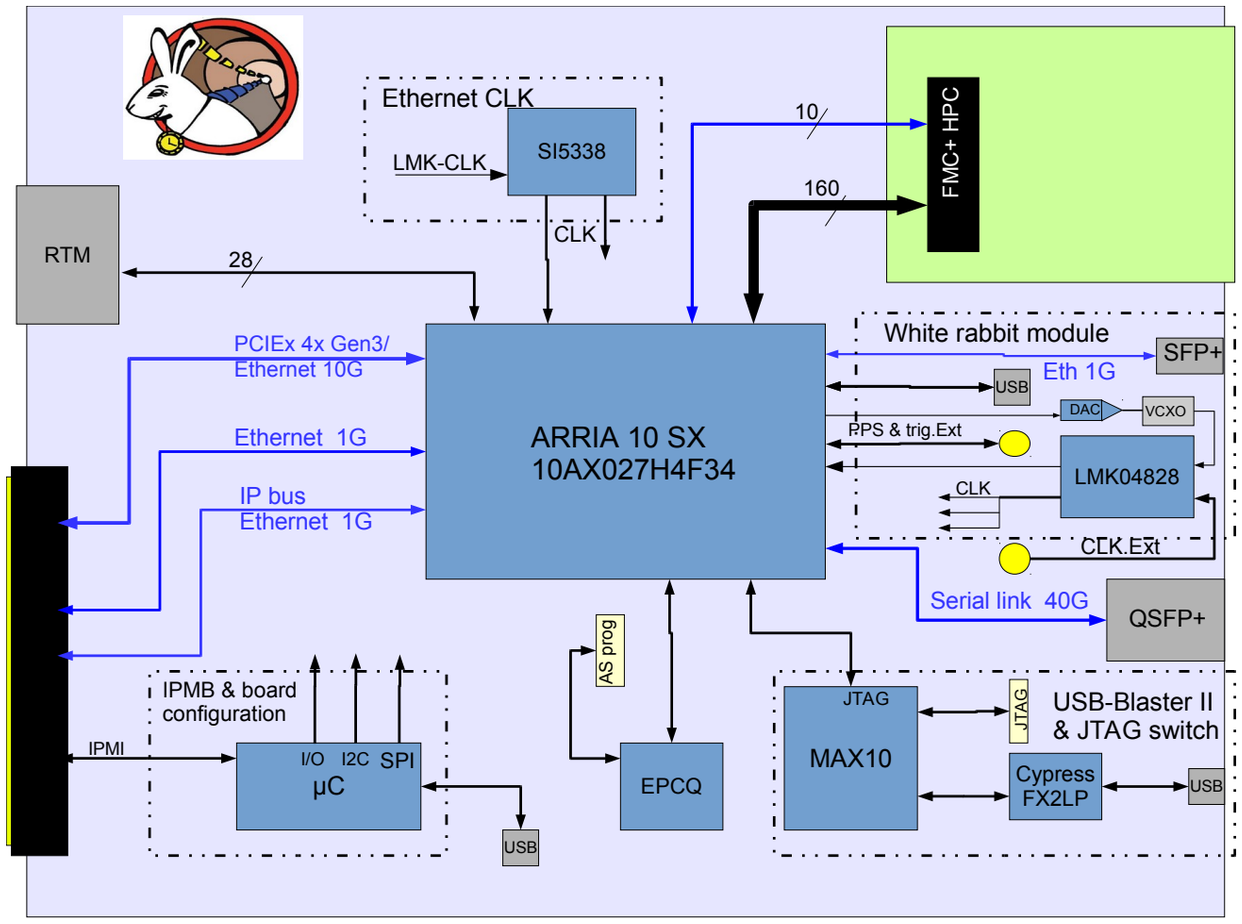


Low phase noise WR -PTP : IDROGEN board

- High performance WR low jitter
- High performance data aquisition system
- FMC+ carrier board
- Design & realization by IJCLAB
- Firmware by Nancay Observatory
- Clock expertise ans qualification by SYRTE
- Measures at SYRTE and IJCLAB

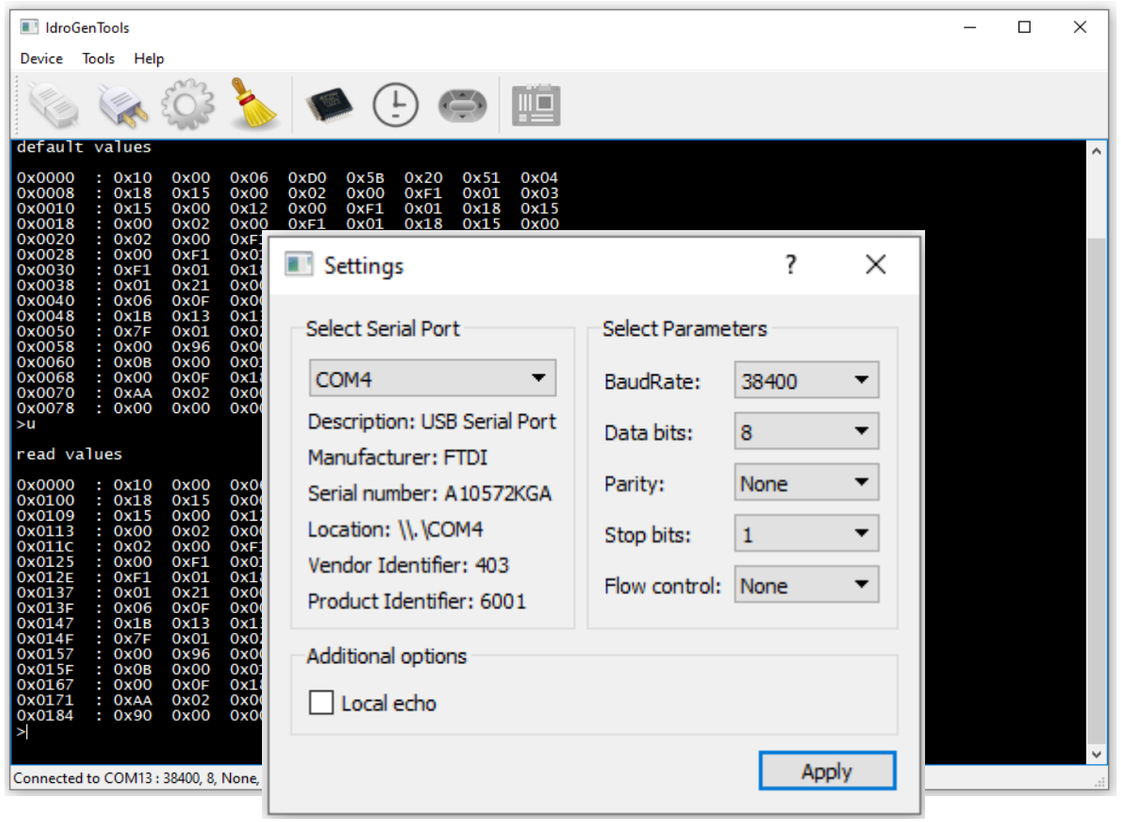


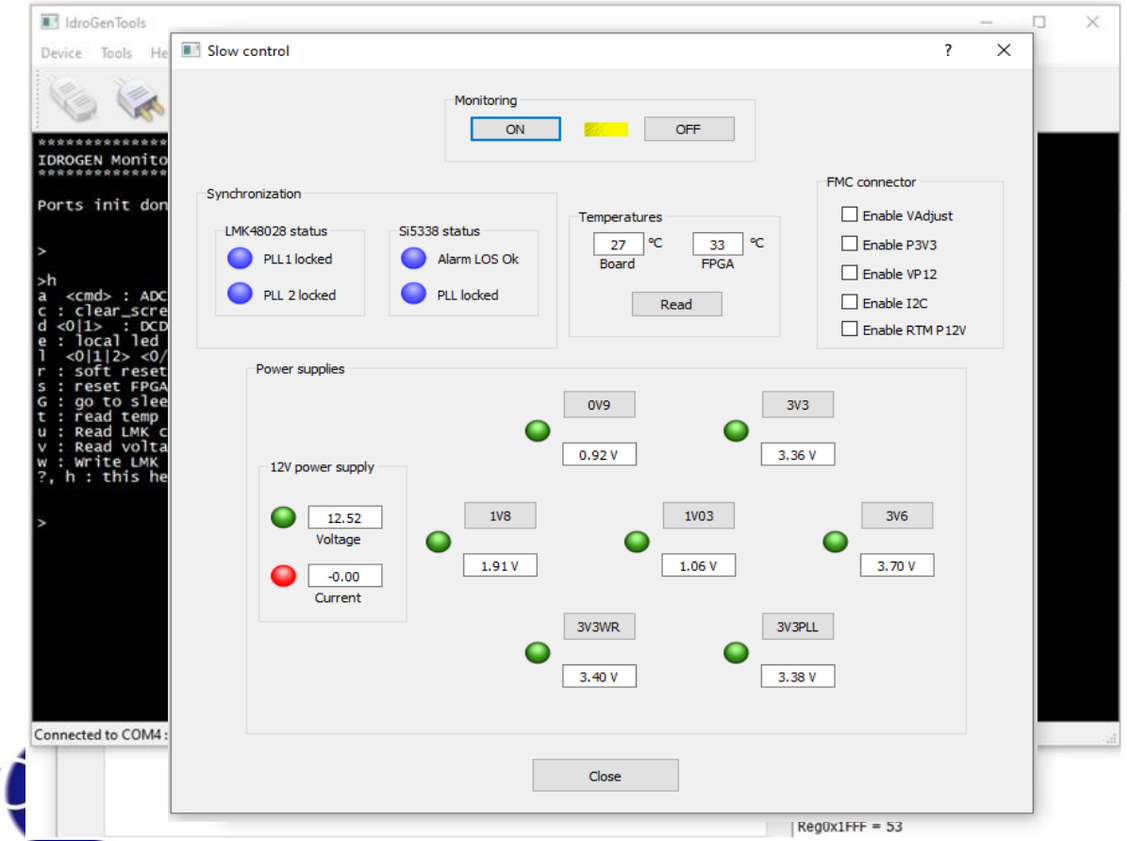
IDROGEN board main features



- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC slot)
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant.
- Front panel conectivity
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity
  - 1Gbe IPbus,PCI 4x Gen3,
  - IPMB, CLK & trigger lane.
  - RTM connector : J30

IDROGEN : Slow control

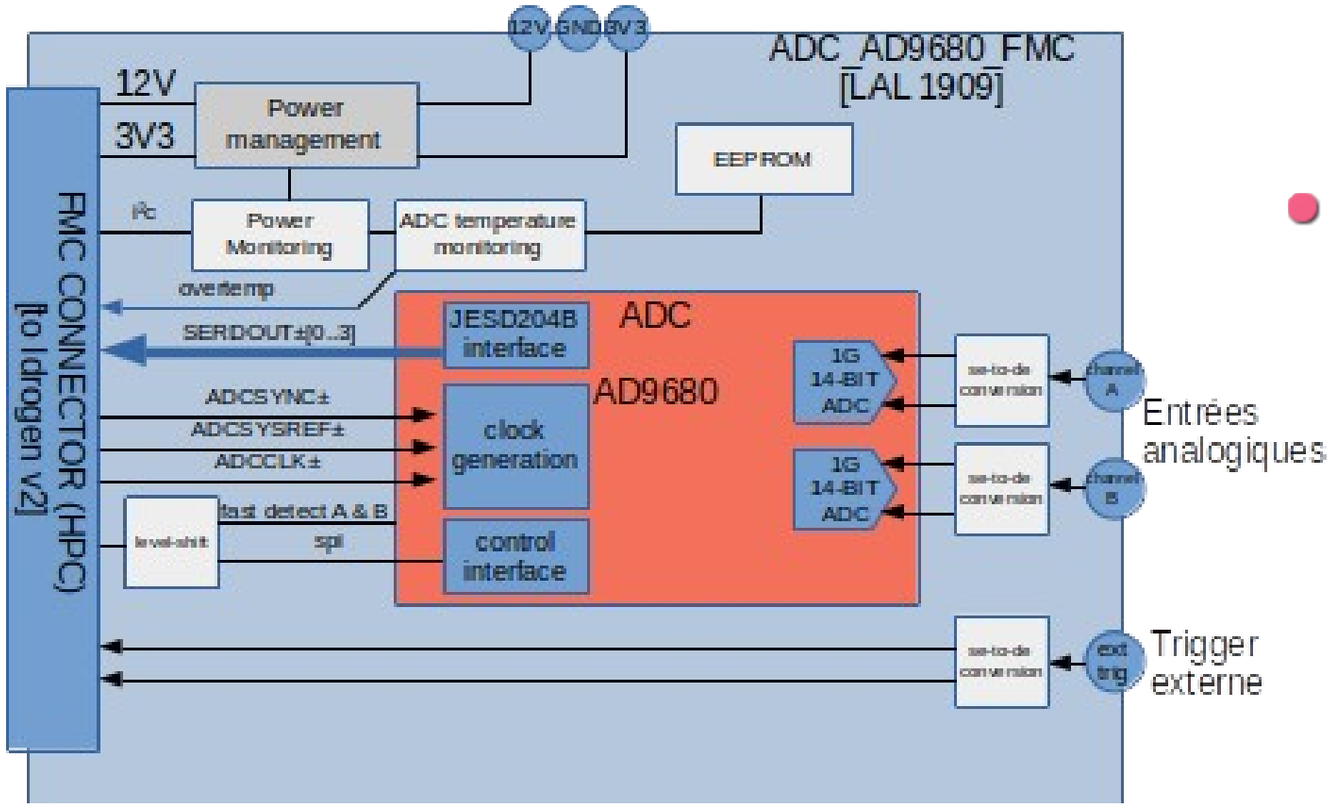




- IDROGEN MMC
  - Software for µC ATMEGA128
  - Base on MMC-DAQGEN package develop by LPSC laboratory
- IDROGEN Tools
  - USB interface
  - For configration and board debug
  - Develop in C++ with QT5 (LINUX and Windows)
- IDROGEN Config
  - For remote configuration & Status
  - Ipbus link
  - Develop in C++ with QT5 (LINUX and Windows)
- Board configuration and status :
- Power, PII configuration : LM04828 & SI5338,
- µC : ATMEGA configuration,RTM & FMC configuration

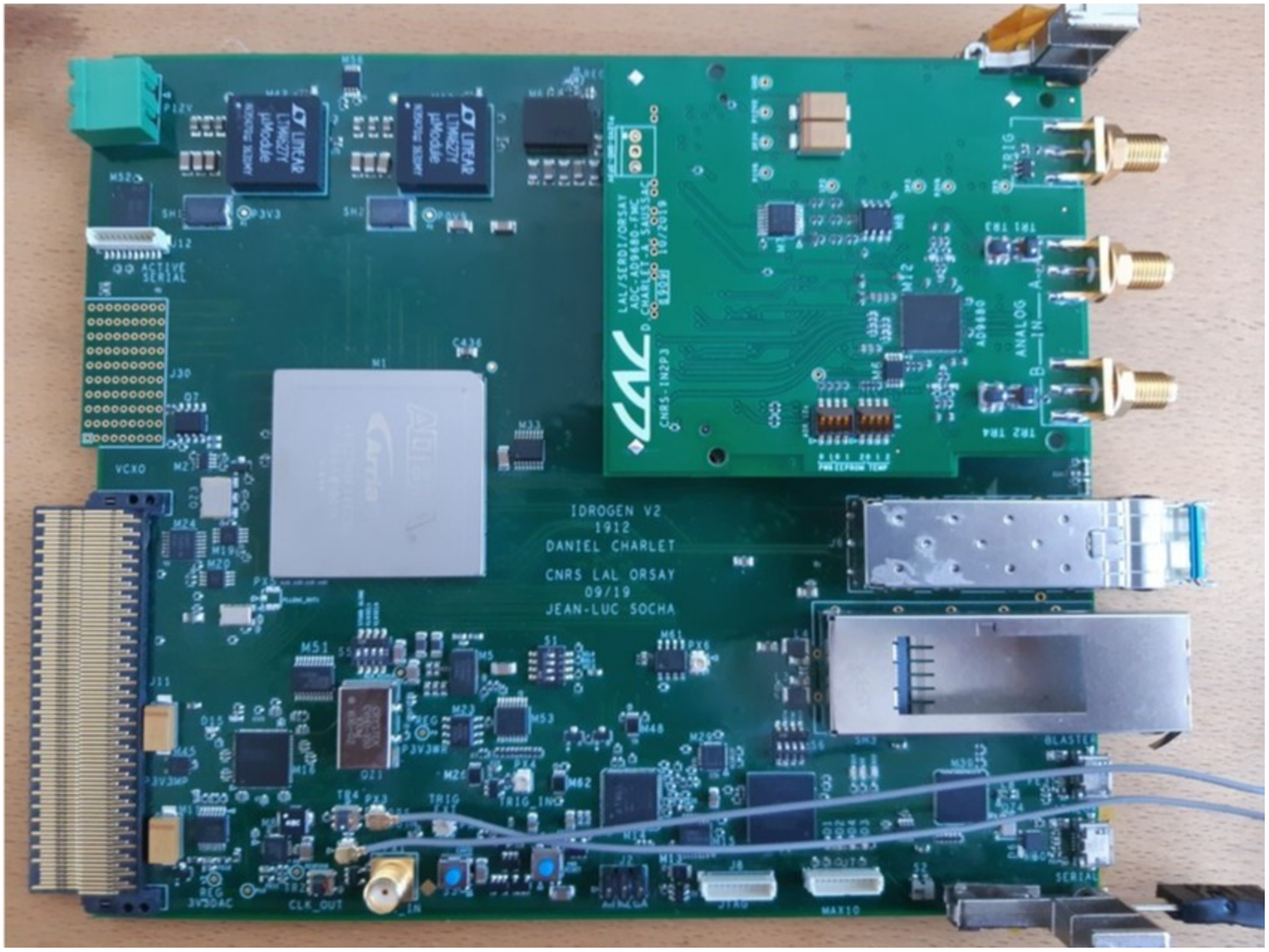
Mezzanine for IDROGEN

Mezzanine FMC ADC 1GSPS



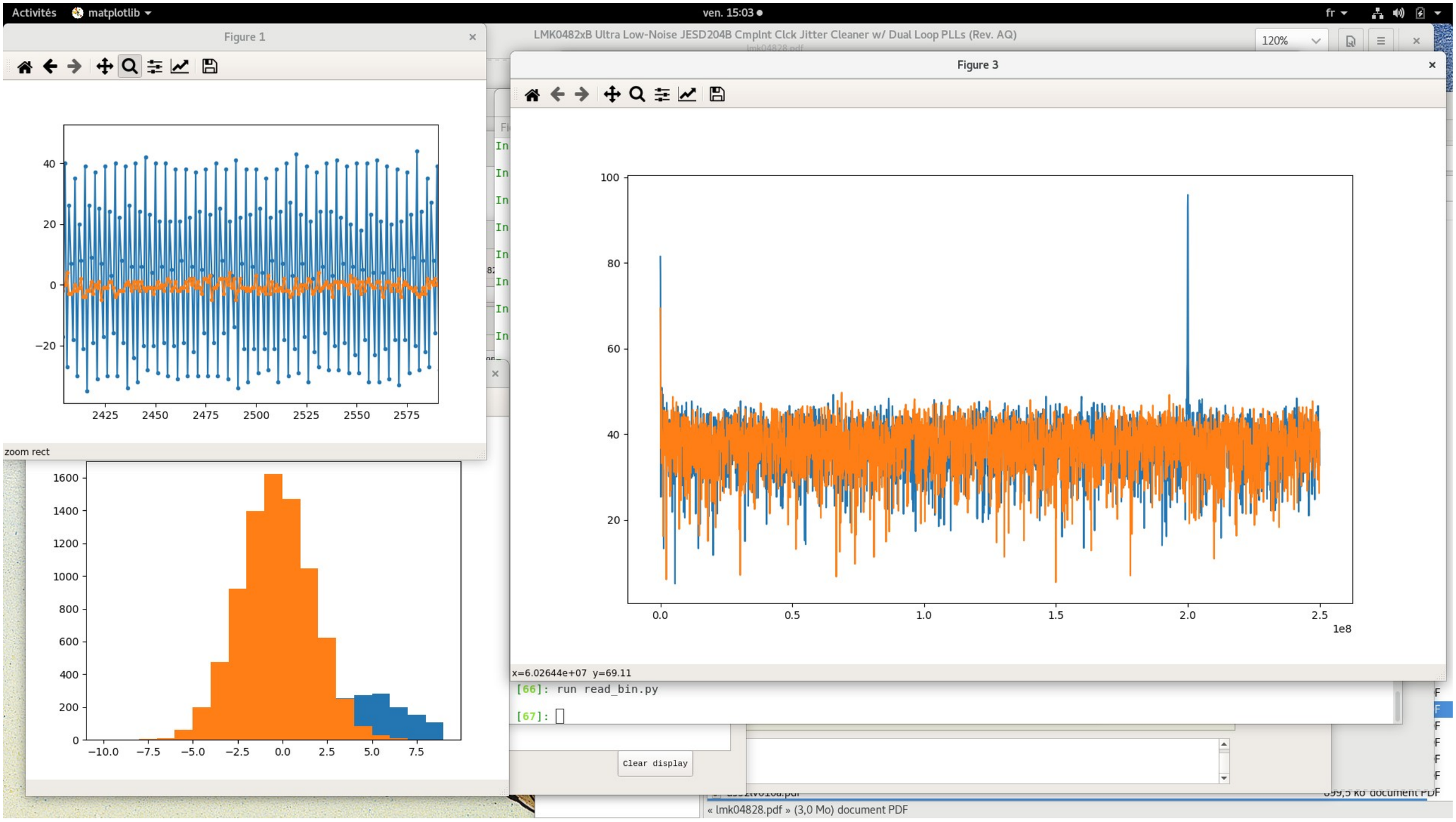
- The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :
  - includes : its own PLL.
  - ADC clock source : External clock
- Mezzanine main features :
  - VITA57.1 (FMC)
  - ADC 9680
  - 2 channels
  - 14 bits
  - 1 GSPS
  - JESD204
  - 2GHz analog bandwidth
  - External trigger in

IDROGEN + mezzanine FMC ADC 500MSPS



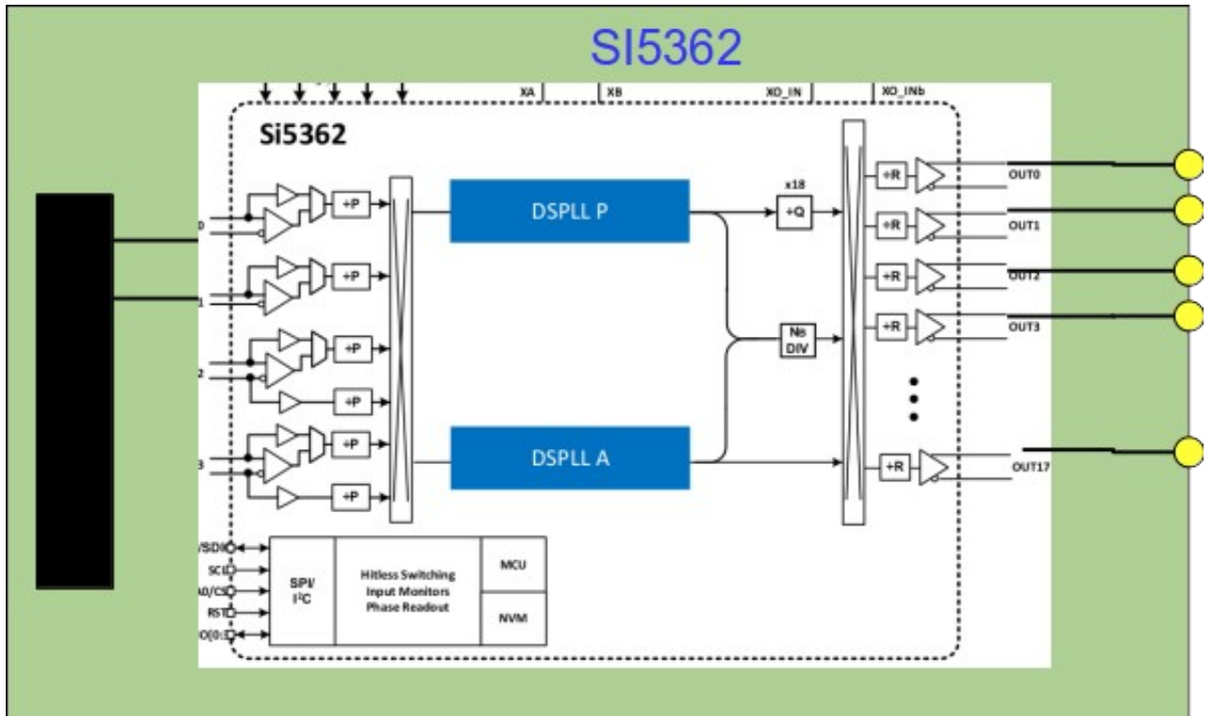
- Bandwidth 500 MHz to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x 10G Ethernet
- Configuration by IPBus 10G
- ADC 1GSPS version currently in test

IDROGEN + mezzanine FMC ADC 500MSPS

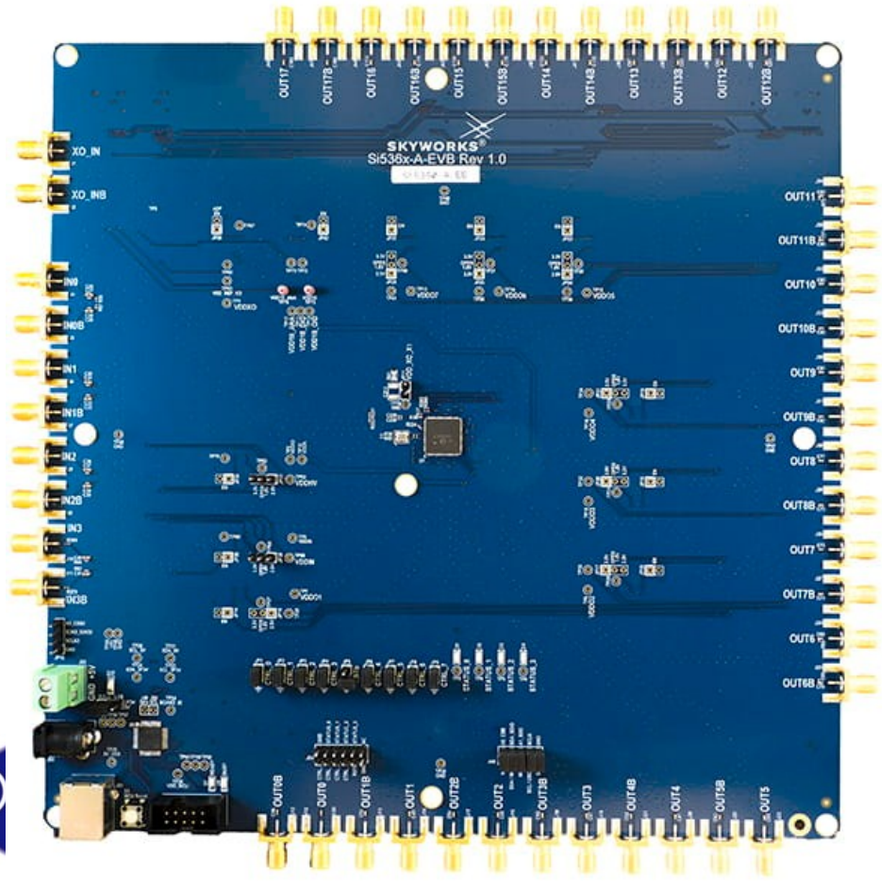


- Signal at 1.8GHz , 3rd Nyquist band

High stability frequency distribution

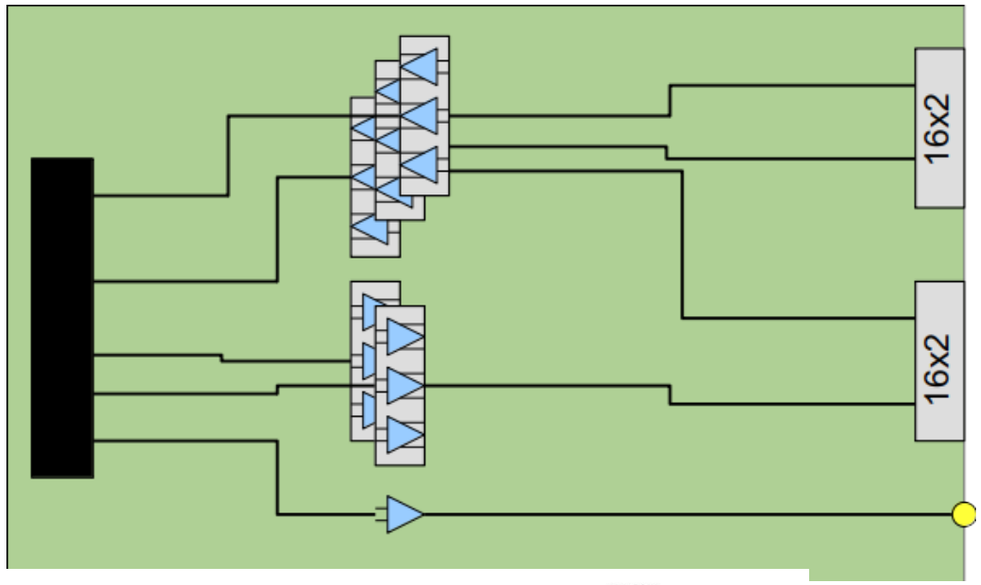


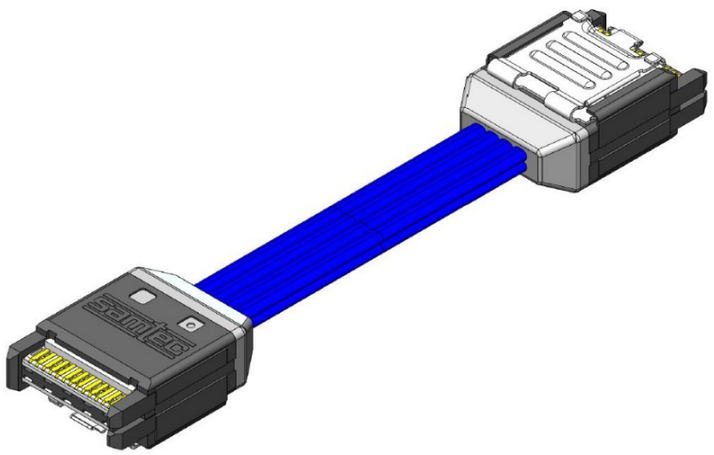
- Master oscillator distribution
- Implementation of a synthesizer on mezzanine FMC : SI5362
  - Phase jitter 55/100 fs
  - Generation of any frequency :
  - 8KHz < F > 2.75GHz
- Collaboration with accelerator department



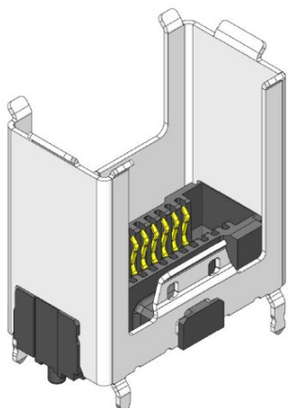
- RF filter outside
- Phase noise evaluation with EBV
- Available end 2023

IDROGEN : Parallel data bus interface





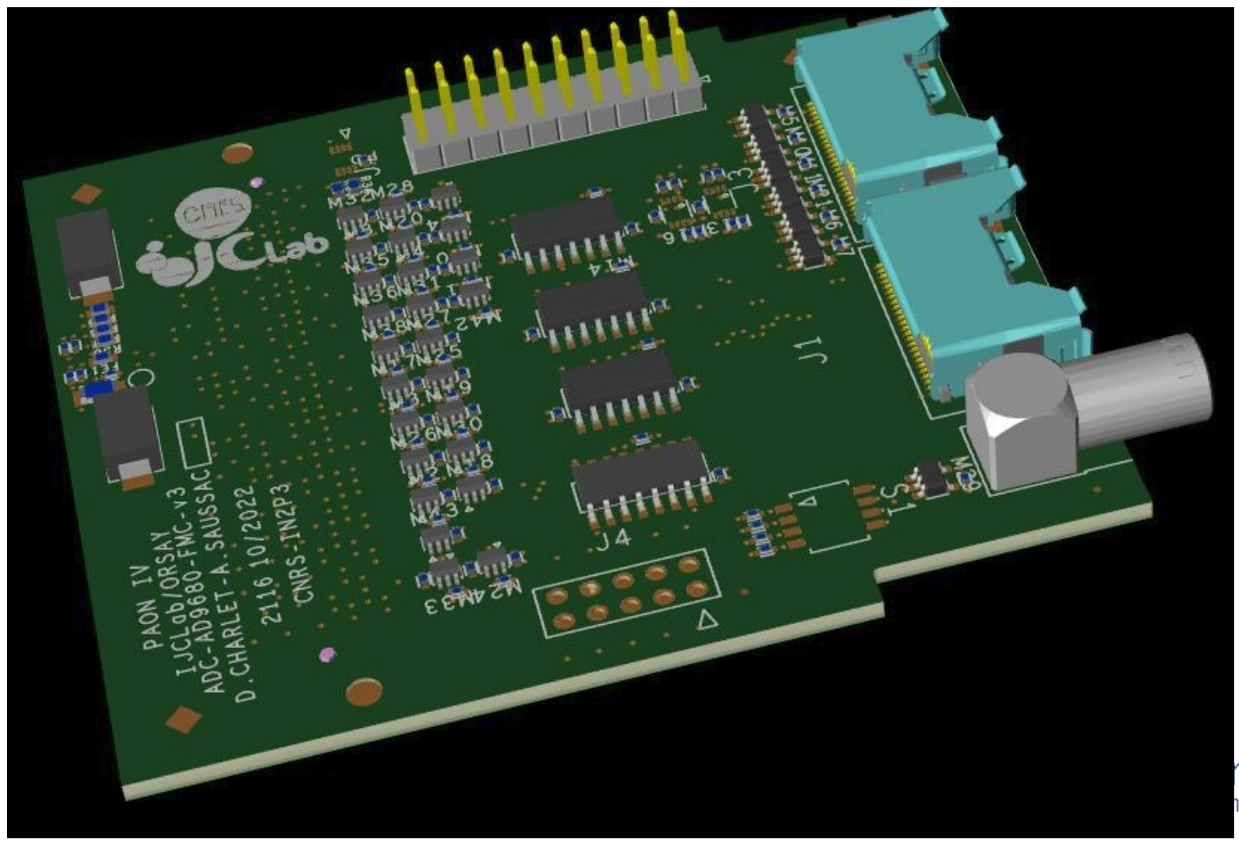
ARF6 Series – Socket, Vertical Orientation



PAM4 56 Gbps NRZ 28 Gbps

56Gbps PAM4/ 28G NRZ

- 16 bit LVDS input; 8 bit LVDS output
- MAX 9180 driver
  - Ultra low noise jitter 23ps
  - 400Mbps by link
- SAMTECH ARC6 connector
  - 12GHz
  - Off the shelf cable
- Signal services : CLK out, I2C, test, ..
- Available mid 2023
- Marie-Lise Mercier LP Clermont rooting

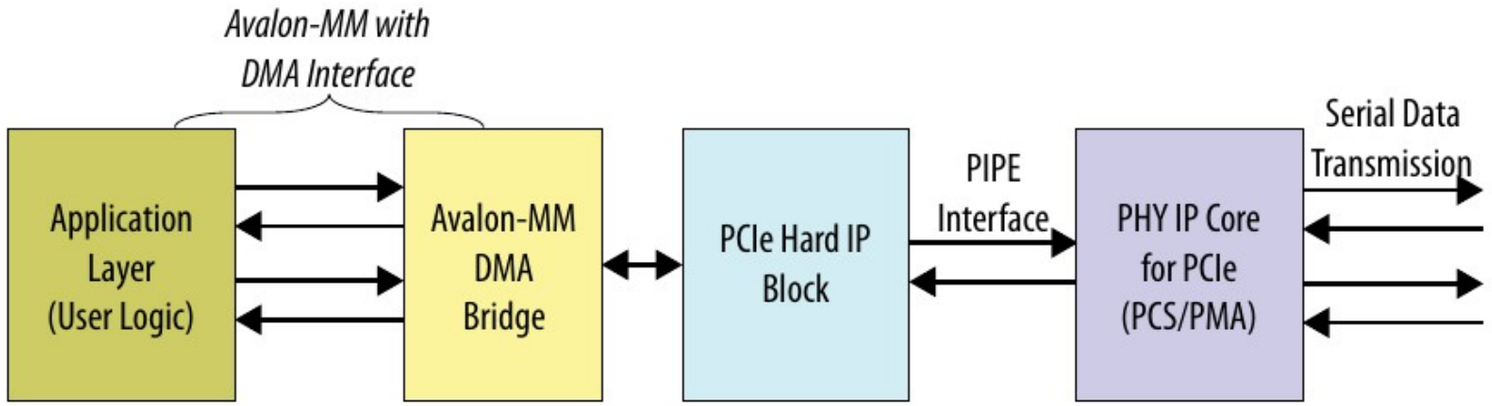


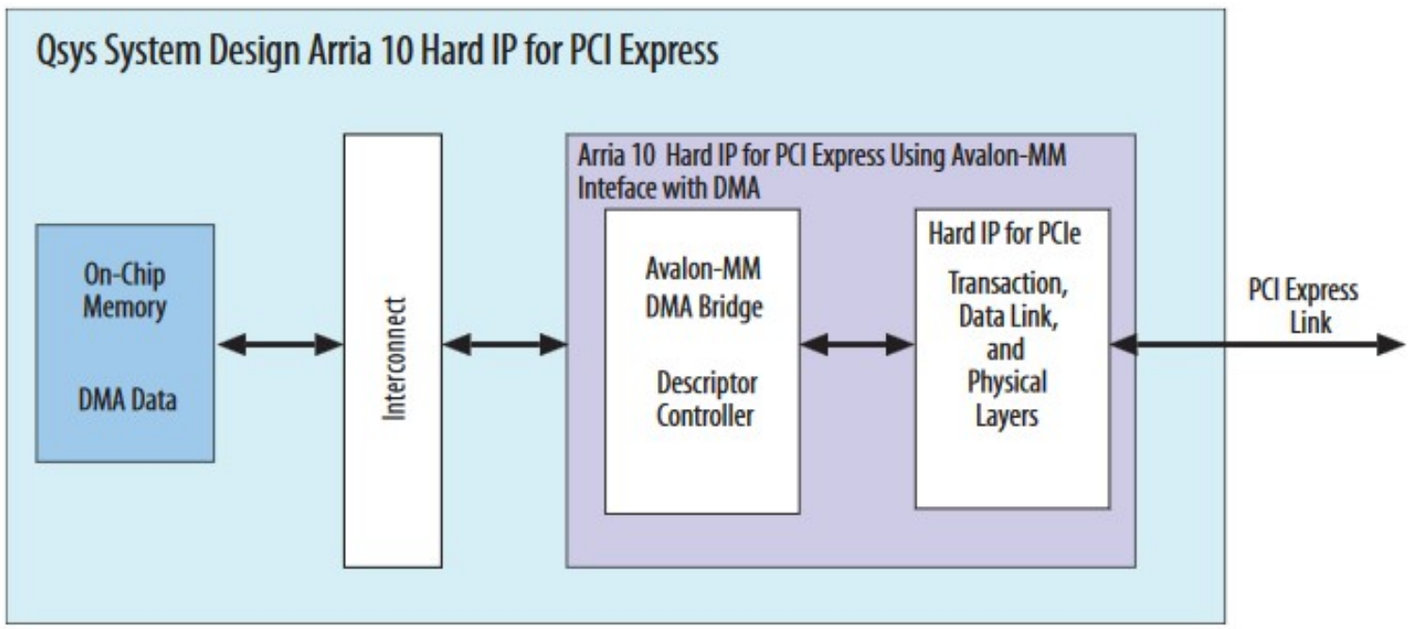
IDROGEN : Firmwares

- WhiteRabbit
  - Development of CERN & GSI
  - Adaptation for ARRIA 10
- IpBus 1G & 10G
  - Development by LPSC laboratory
  - Adaptation by IJCLAB for ARRIA 10
- Streamer UDP 1G/10G
  - IJCLAB development
- PCIexpress v1
  - Based on INTEL-FPGA
- PCIexpress v2 (in development)
  - Based on CERN LHCb development
  - High and continuous data rate acquisition
- GBT 2 PCIe
  - Based on CPPM LHCb for PCIE40 development
- JESD 204B for high speed ADC
  - Base on INTEL-FPGA IP
- Parallel 64 data acquisition
  - For 2 ADC 125MBPS 16bits
- IpBus on WR link
  - One optical link : timing, synchronisation, configuration, data readout
  - IJCLAB development

IDROGEN PCIe V1

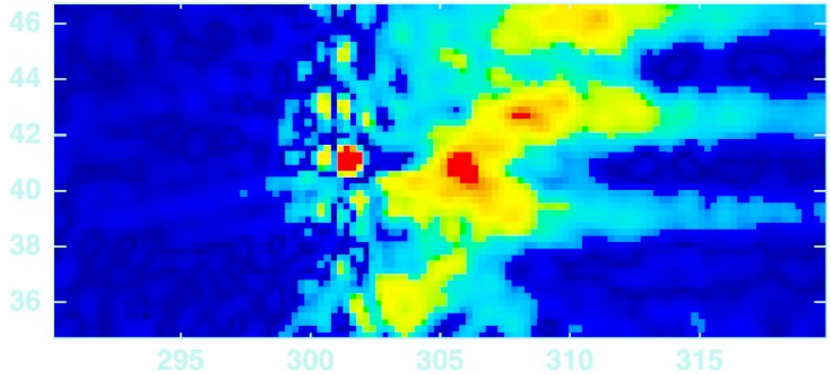
- Based on INTEL IP
  - Gen 3 4x End-point mode, 128-bit layer interface payload 256 bytes
- Can perform
  - Access of the PCIe host with the Bar0 to Bar5 interfaces
  - Access of FPGA logic by Avalon MM interface
  - DMA transfers



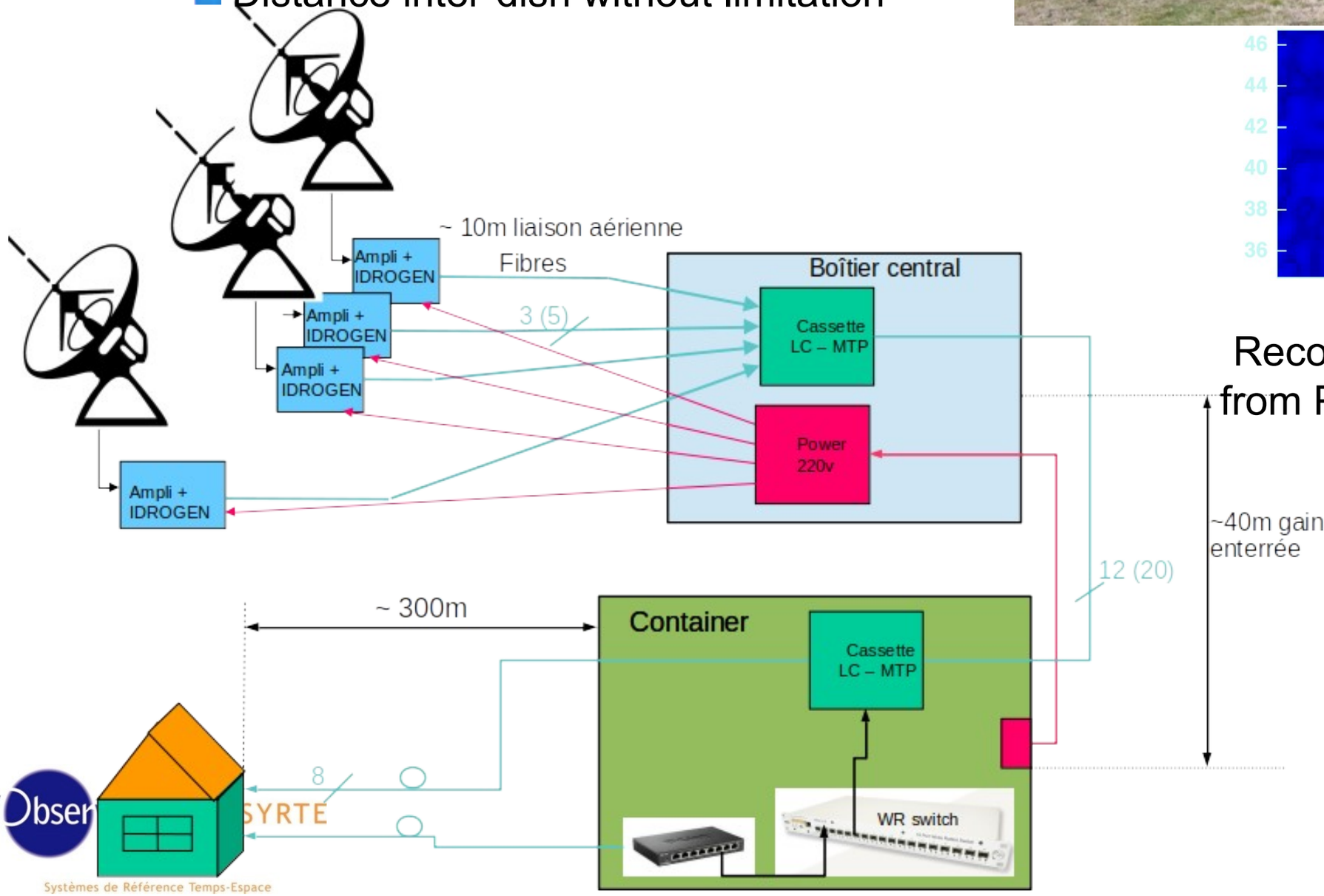


PAON IV : configuration in development

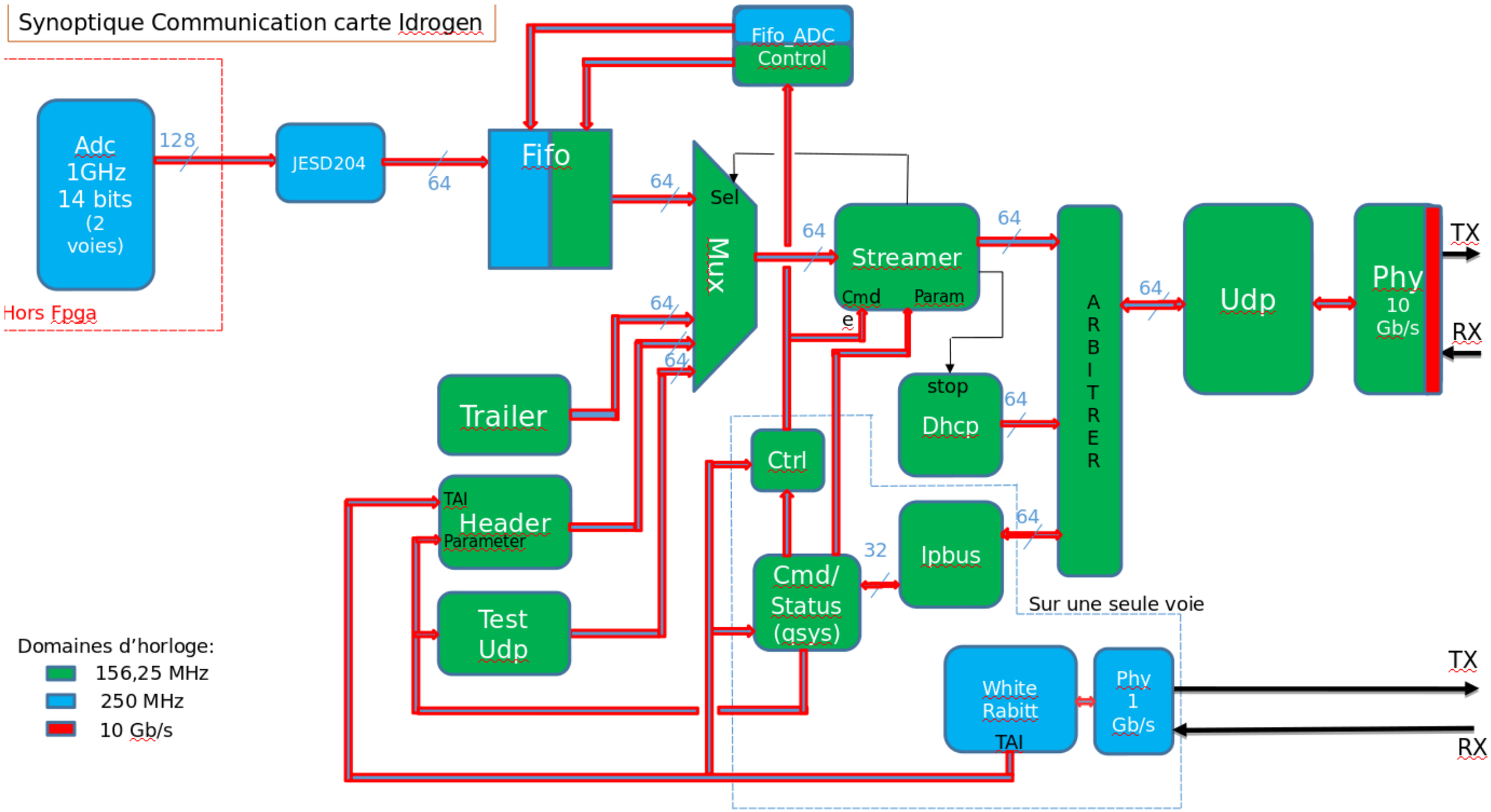
- Interferometer radio : 4 dishes of 5m
- 3D mapping of atomic hydrogen
  - 4 IDROGEN board
  - High bandwidth : 500MHz
  - 8 ADC 14b 1GS/s
  - Synchronised by WR
  - Distance inter-dish without limitation



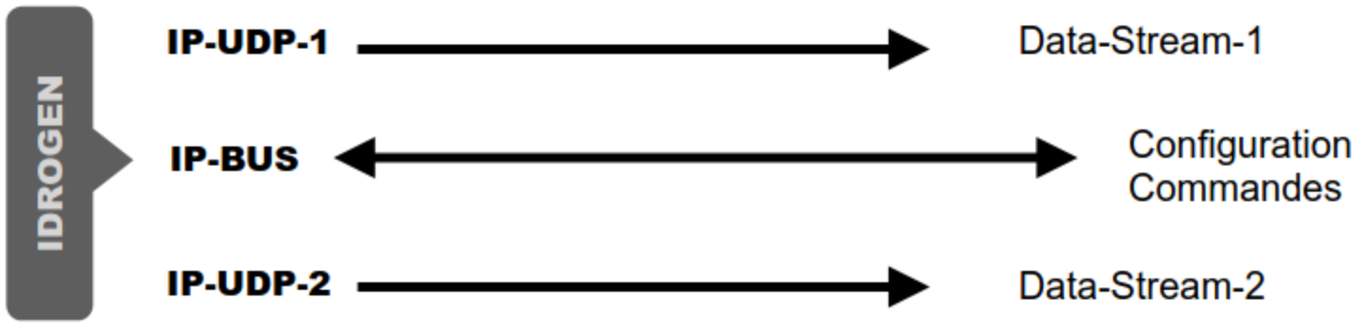
Reconstructed map at 1420.4 MHz from PAON-4 Nov.2016 observations



IDROGEN firmware PAON IV : readout architecture



IDROGEN firmware : Ethernet readout



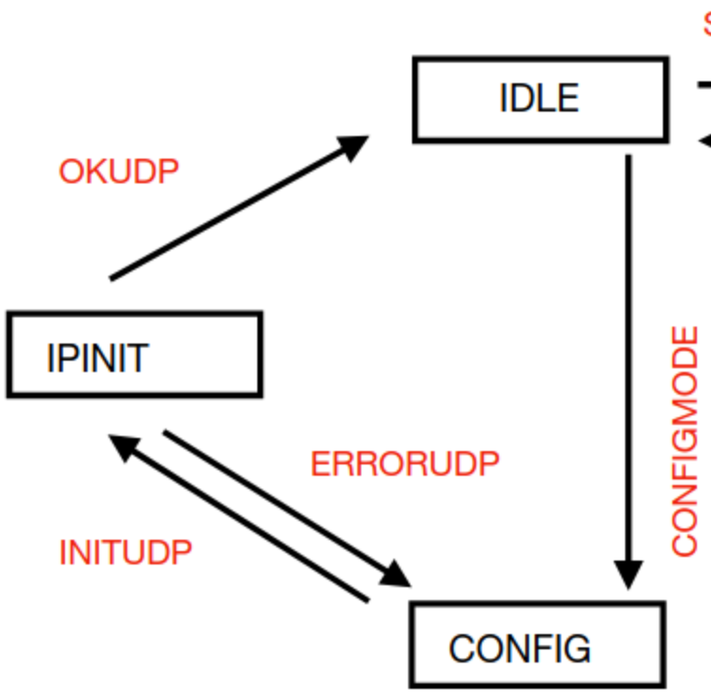
- 2 ETH 10G links
- 1 Ipbus 10G link, share with UDP link
- Multi Jumbo frame by event

- Header : 4 x 64b
  - Start mark : 4bytes
  - Paquet lenght : 2bytes
  - Paquet number : 2 bytes
  - Sernum paquet : 4 bytes
  - Board/Channel ID : 2 bytes
  - DataDescriptor : 2 bytes
  - TAI : 8 bytes
  - Reserve 8 bytes
- Trailer : 64b
  - Reserve 4bytes
  - Trailer mark 4bytes

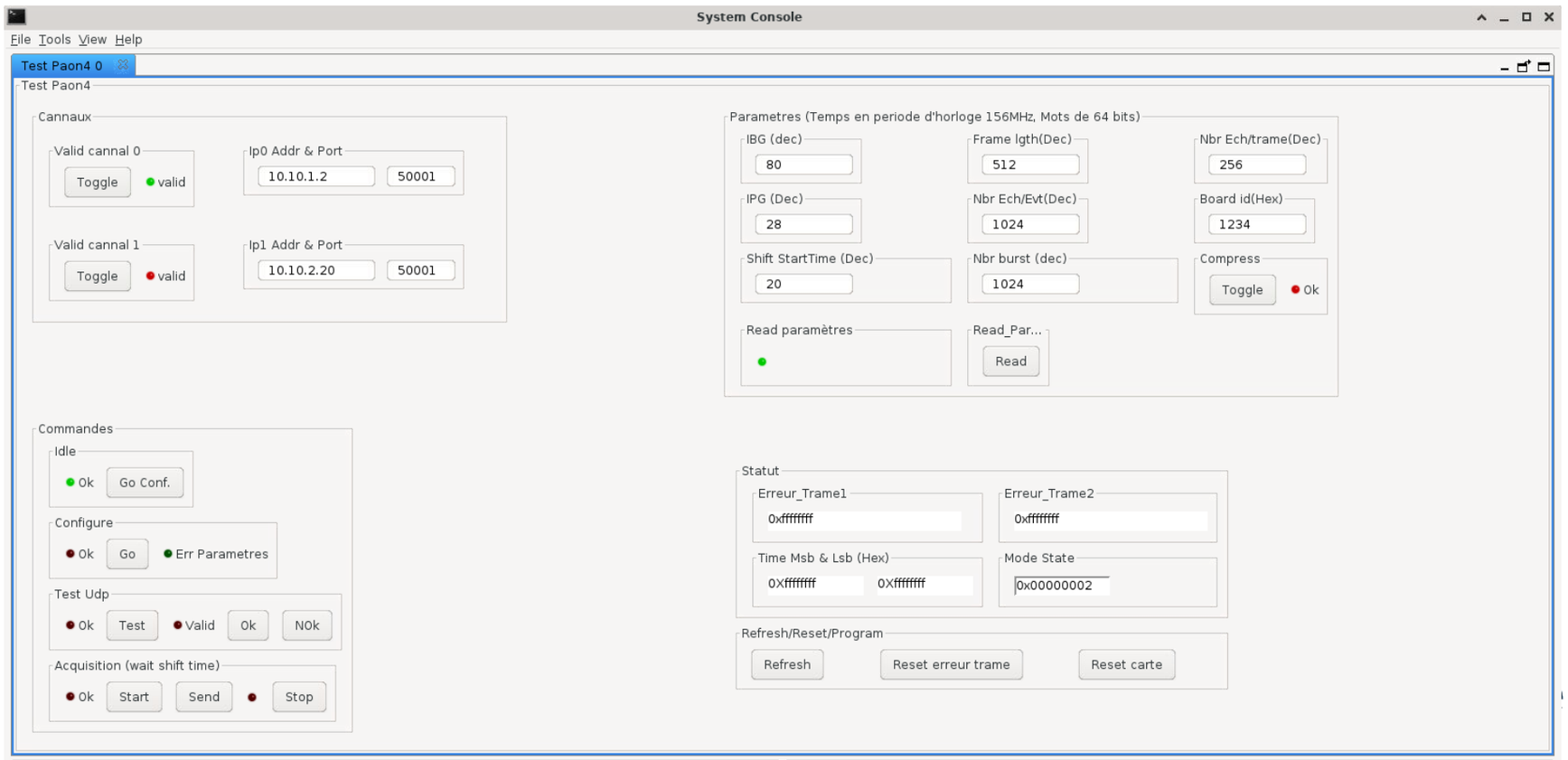
IDROGEN firmware : Data readout

IPG IPG IPG

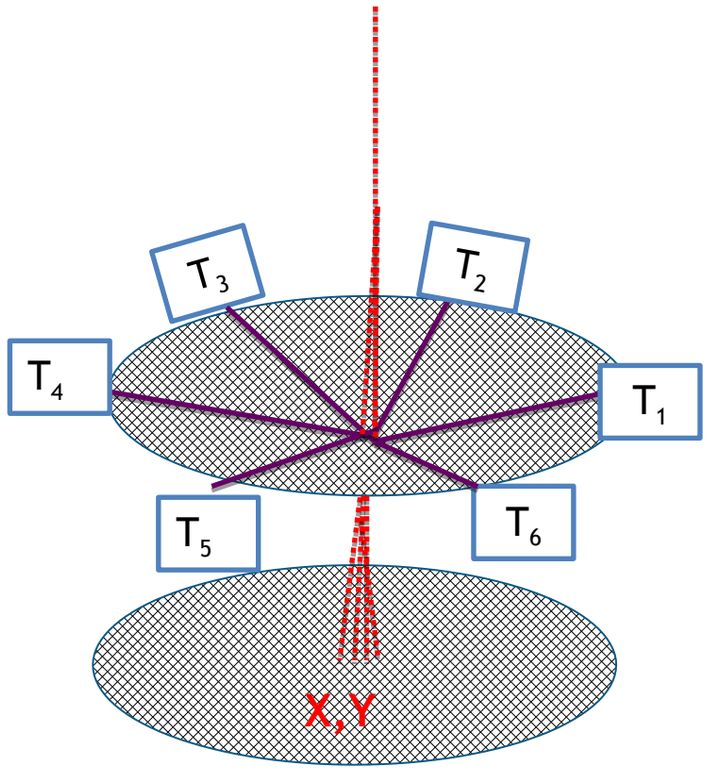
- Flow control
  - Inter Packet Gap : time between UDP paquest
  - Inter Bus Gap : Time between paquet group



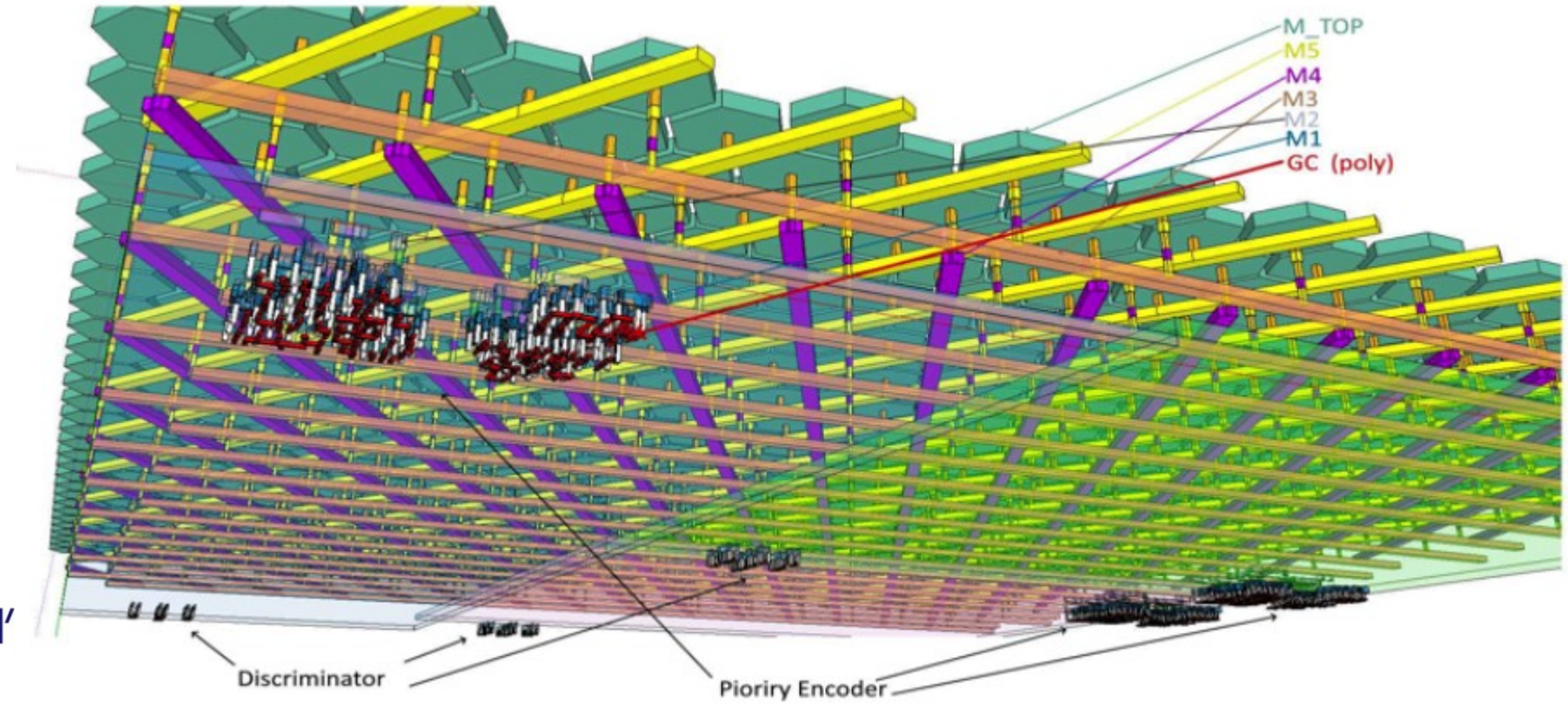
- Command, configuration and control
- Manage by IpBus
  - 4 states



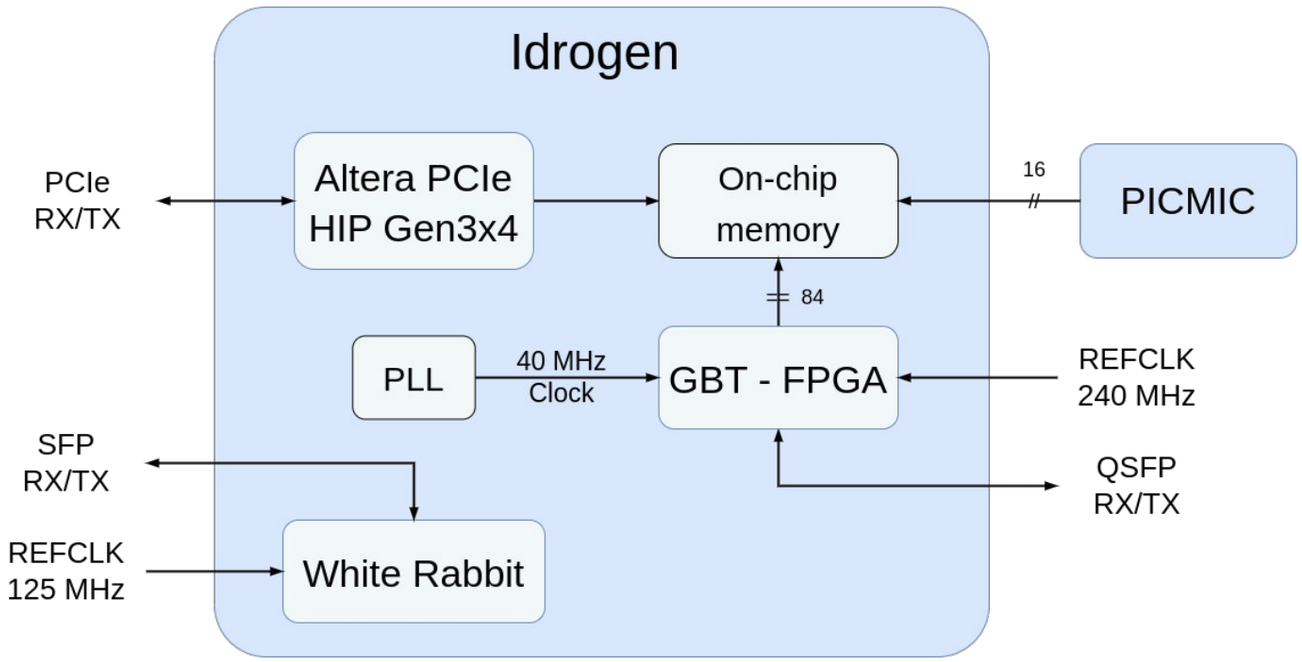
IDROGEN PICMIC detector: readout architecture



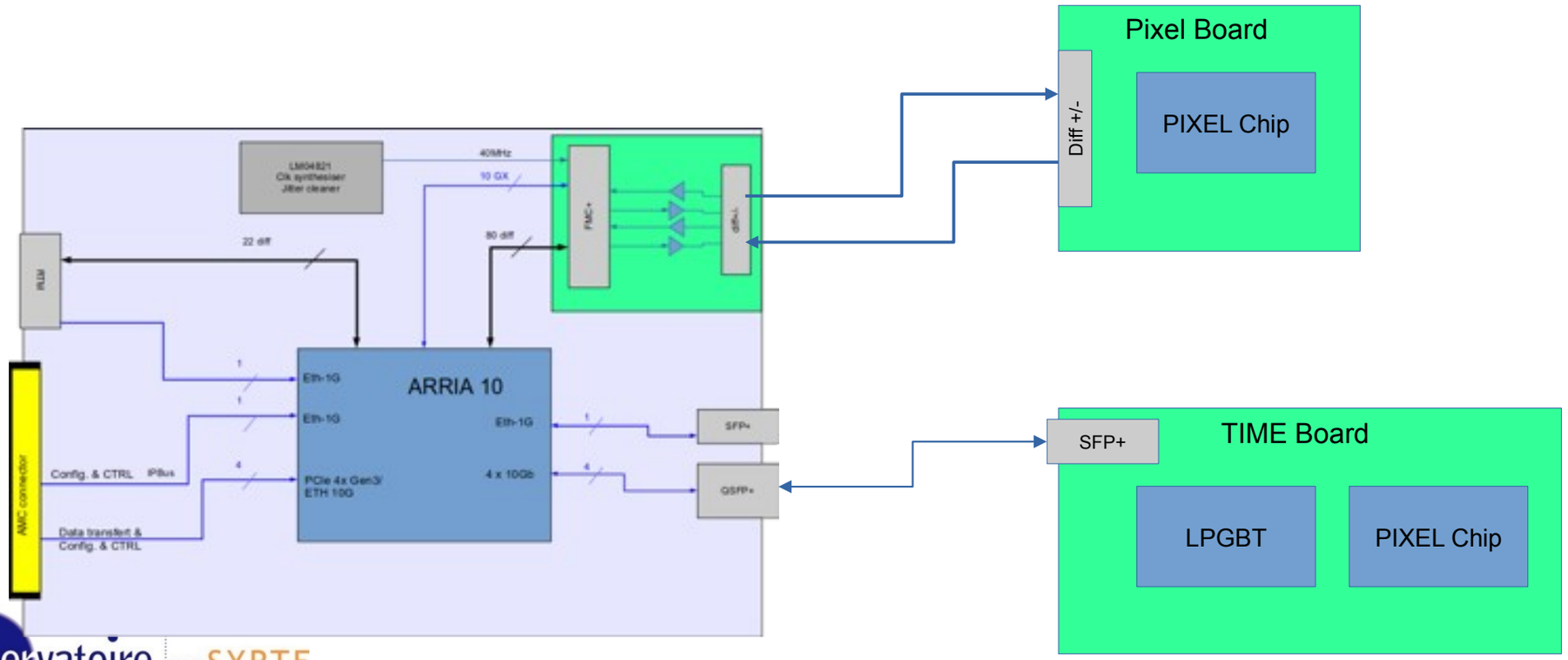
- PICMIC : high time and spatial resolution detector
  - Pixel detector
    - Position :Parallel PICMIC chip readout bus (IP2I)
    - Time : PICOTDC with GBT readout (IPNL)
    - Acquisition : IDROGEN
    - Synchronization and time tagging by WR
    - Readout and Command & Control by PCIe



IDROGEN firmware PICMIC : readout architecture



- Data readout
  - PCIE Gen 3 4x End-point mode, 128-bit layer interface payload 256 bytes
  - DMA readout (INTEL IP)
- Data acquisition
  - Spatial data : LVDS parallel interface (IJCLAB firmware)
  - Timing : GBT (CPPM firmware)

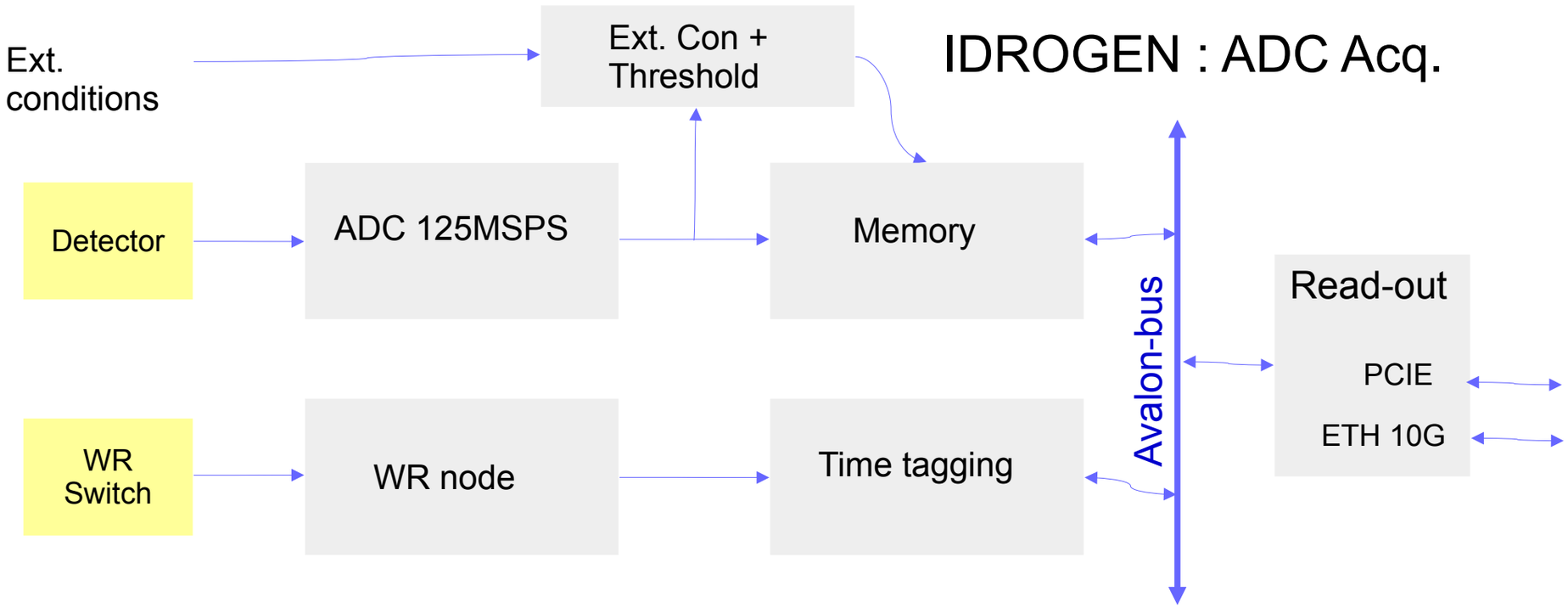


Systèmes de Référence Temps-Espace

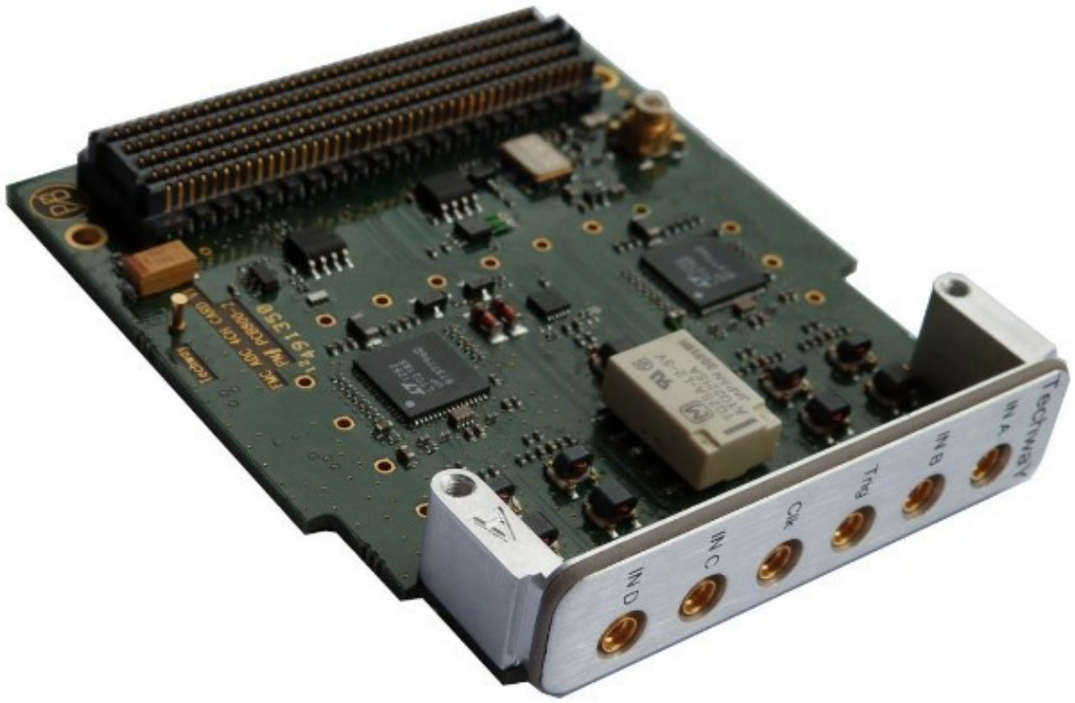
Trigger-less acquisition system : New-Comet

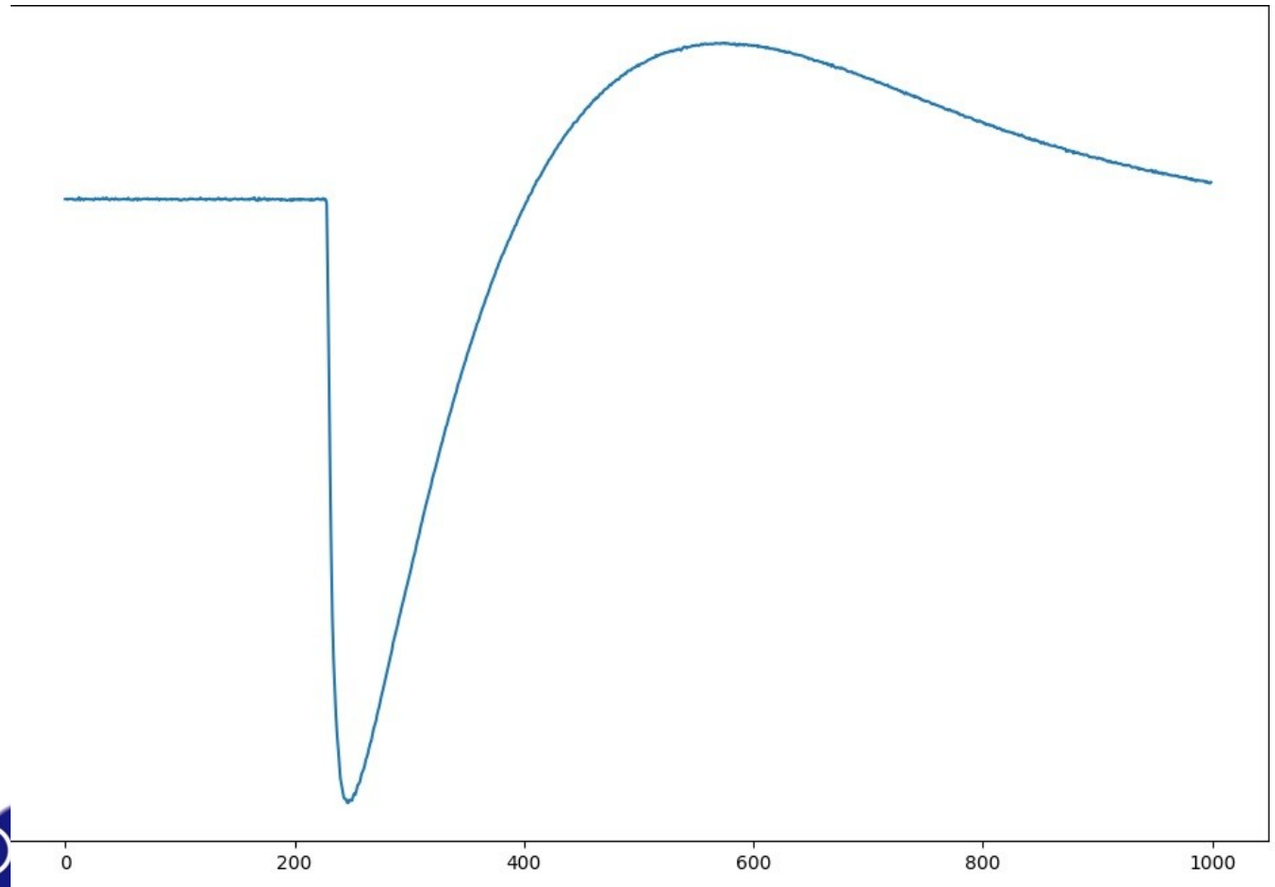
Trigger less acquisition system : New-COMET

- Trigger-less detector acquisition system
- Continuous signal coding : 4 x 125MSPS 16bits
- WhiteRabbit time tagging
- High level treatment performed by the acquisition software
- Energy and timing correlation made by acquisition software



Trigger less acquisition system : New-COMET





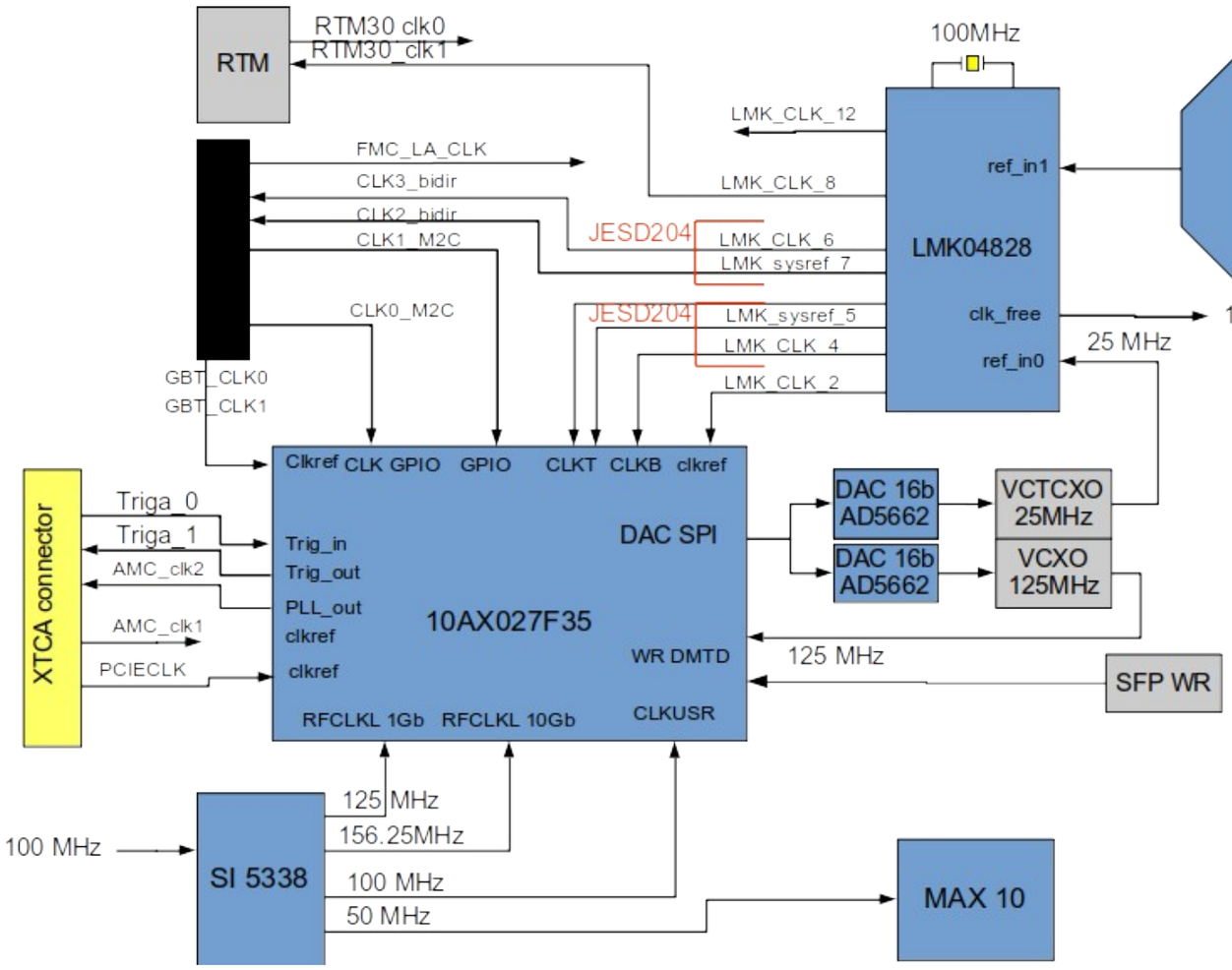
- Off the shelf mezzanine
- No dead-time data transfer
  - 10G Eth or PCIe gen3 4x
- Data memory with sliding window
- Data taging by WR
  - 4ns timing resolution
  - Jitter ~13ps/200ps RMS at 1000s

Systèmes de Référence Temps-Espace

Conclusion

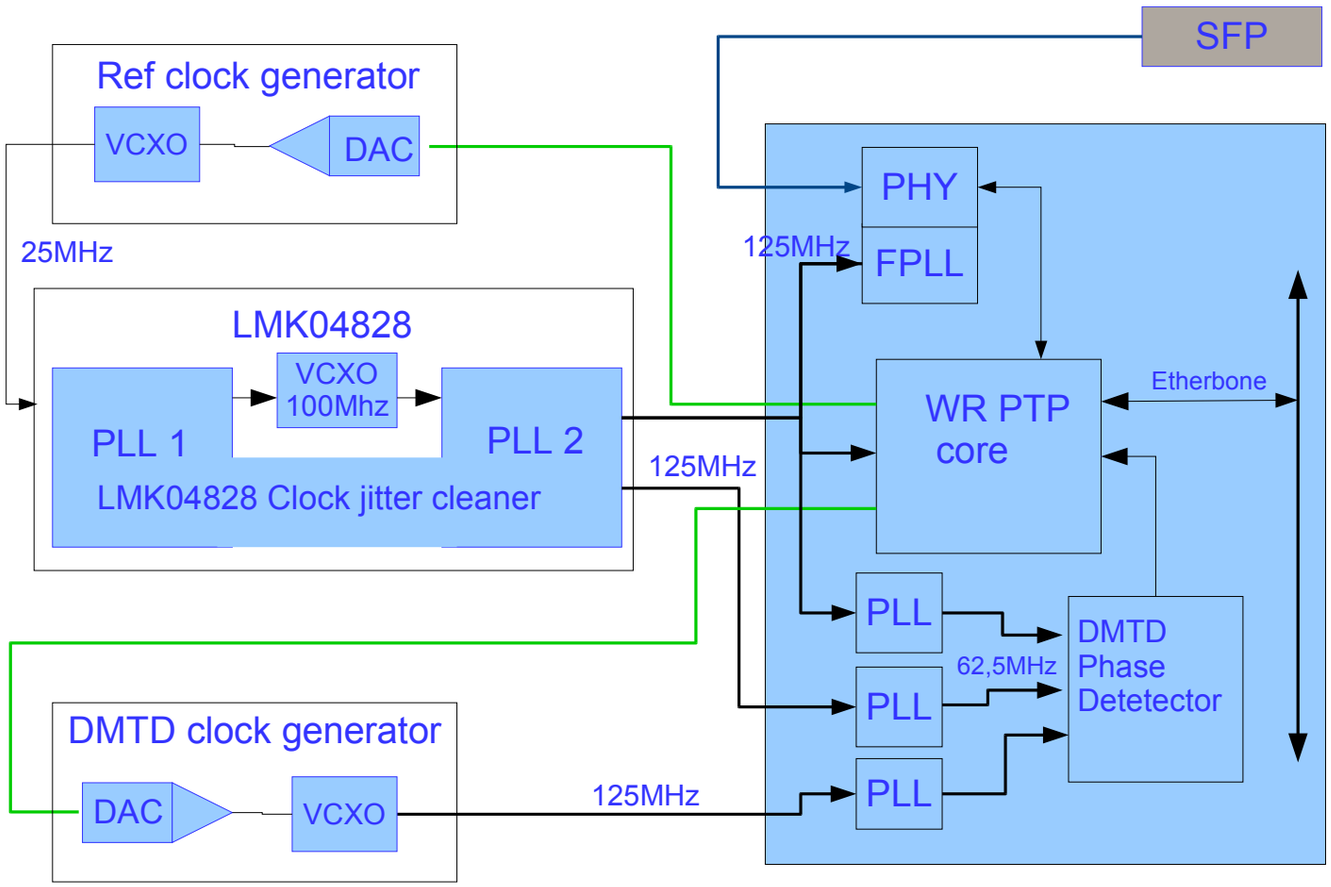
- 15 boards have been produced
- For 5 laboratories of IN2P3 and INSU institutes
- New collaboration with KEK accelerator
- New version will be designed due to components obsolescence
  - Design Autumn 2023
- Very versatile system
- State of the art for the WR node performance : accuracy and precision
- Data transfer functionalities :
  - informatics protocol : PCIe, ETH1G/10G
  - Dedicated : GBT, JESD204B
- Customize functionalities could be implement using dedicated FMC mezzanine or off the shelf mezzanine : DAC, ADC, I/O, serial I/O, ...

IDROGEN : Clock tree



- LMK4828 clock in :
  - White-Rabbit module.
  - SMA connector.
  - RMT30 connector : CLK0.
  - FMC connector : LA_CLK.
  - AMC connector : TCLKB.
- LMK4828 clock out :
  - FMC connector JESD204 compliant : Clk2_bidir, Clk3_bidir .
  - RTM : CLK1
  - FPGA : CLKREF, clk.
  - AMC_CLK2
- FPGA receives also direct clocks from different sources :
  - FMC connector
  - AMC connector
  - RTM connector

IDROGEN : WhitRabbit implementation



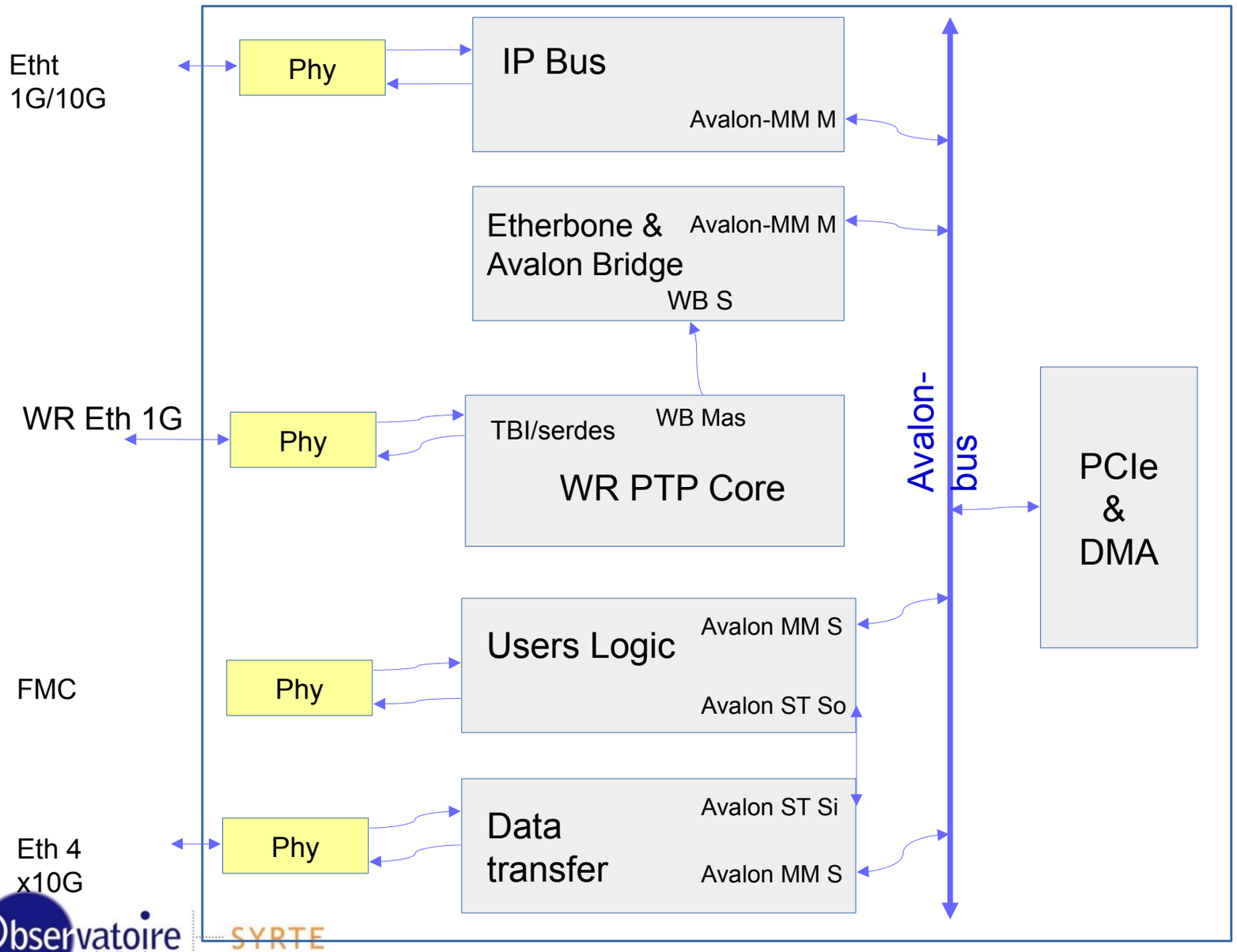
The WhiteRabbit IDROGEN hardware is based on CERN open hardware with Enhancements

- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
  - Tx/Rx routing equalisation

Backup

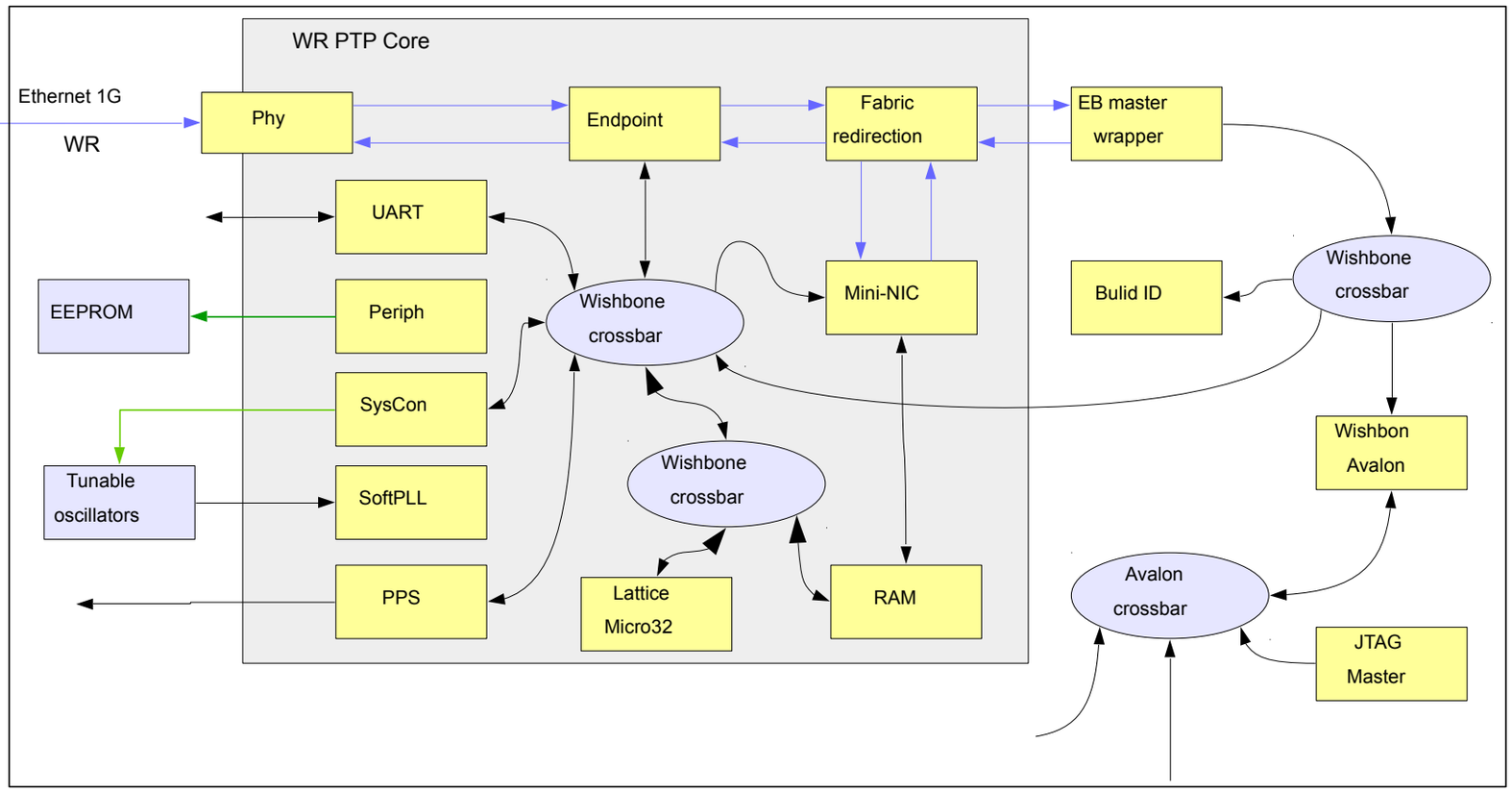
IDROGEN firmware architecture

- The firmware is developped using QSYS system integration tools.
- Two QSYS Avalon masters : IPBus & WR
  - WhiteRabbit PTP core, Avalon master bus
    - Manages all functionalities for the WR
    - Manages the Etherbone protocol
    - Interfaces to FPGA core by Wishbone to Avalon interface.



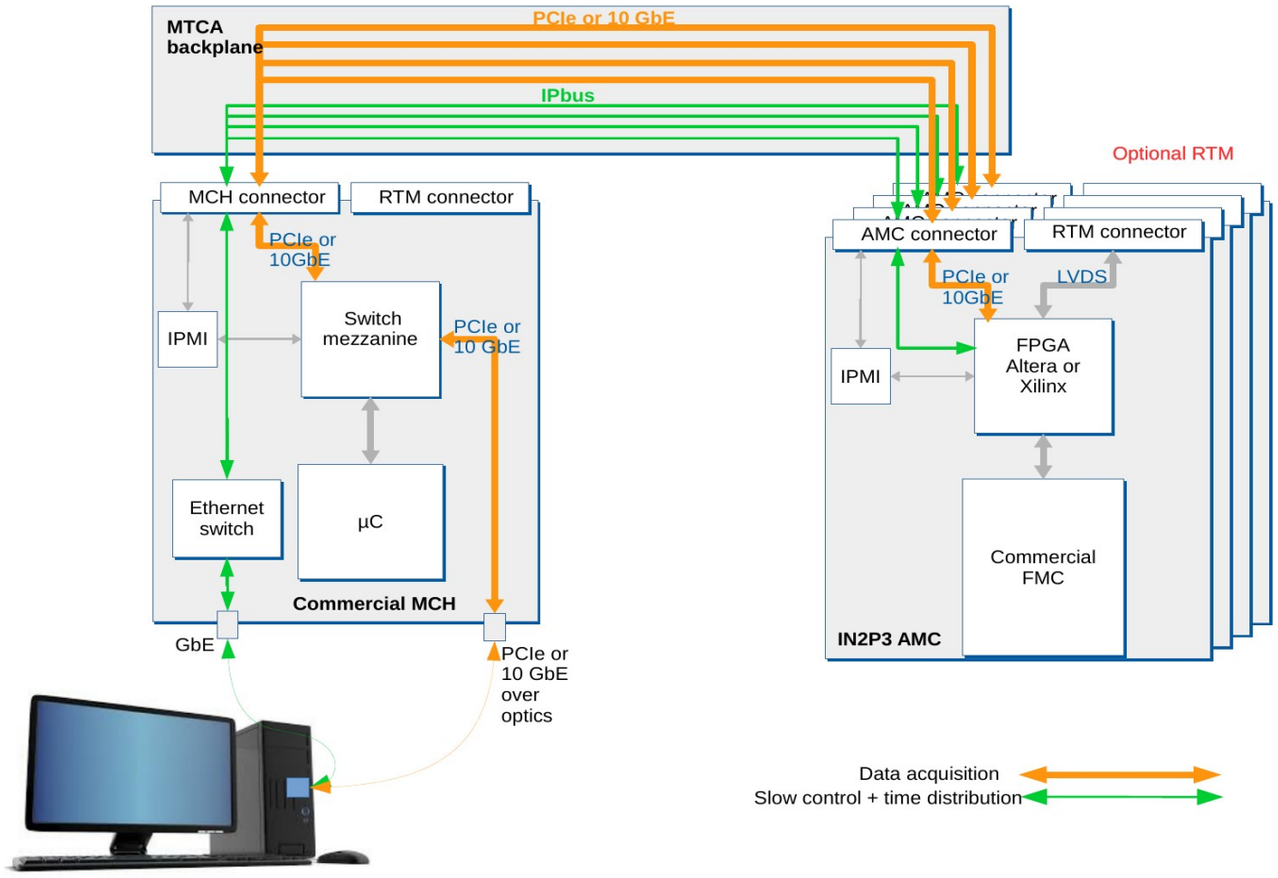
- IPbus, Avalon master bus
  - Slow-control
  - Data read-out
- Users Logic, interface to FMC connector.
  - Avalon Slave interface.
  - Avalon Streaming source to data-transfer module
- Data transfer, data read-out
  - 2 x 10G Ethernet
  - PCIe Gen3 x4
  - 40G Ethernet (if IP available at IN2P3)

WiteRabbit firmware



- All numerical module fully included in FPGA
- Fully coded in VHDL (including phy)
- Based on Lattice-Micro32 µ-controler (writing in VHDL code)
- Communication to FPGA core with Wishbone interface.
- Interface Wishbone to Avalon (LAL/Obs. development)
- Open firmware
  - At the origin developed for Xilinx.
  - Development for ALTERA
    - ARRIA2 & 5 GSI (recently 10)
    - ARRIA 10 Nancay/LAL
- System clock 62.5Mhz
  - Future development 125Mhz

Acquisition system : DAQGEN



- Standard : xTCA for Physic
- Based on an off the shelf system
- Crate controler : MCH fron N.A.T
- Data read-out :
  - Backplane : PCIe 4x gen 3 / ETH 1G/10G
  - Front-side : ETH1G/10G , 2x 10G
- Board configuration Ipbus : ETH0 or SFP+
- Synchronisation : WR