Laboratoire d'Annecy de Physique des Particules

Retour GTC 2022 : GPU Technical Conference

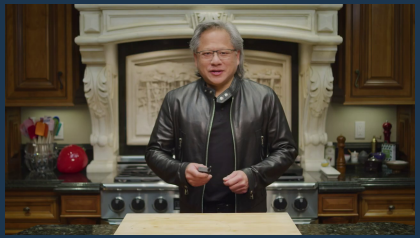
Pierre Aubert

ESCAPE
cherenkov telescope array
cnrs
UNIVERSITÉ SAVOIE MONT BLANC

Introduction

GTC 2022 `https://gtc22.event.nvidia.com/`

This is not possible to summarize **987** talks !



Keynotes video link

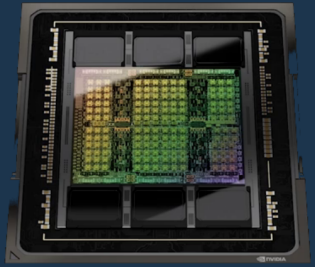
Only focus on :

- **Hardwares** evolution
- **Compilers** evolution
- **Programming Languages** evolution
- **Job Communication**
- **Data Compression/Decompression**
- **Machine Learning** / **Deep Learning** evolution and use
- How all (will) work together (with a bit of **Forum ORAP**)

Hardware evolution

Hardware evolution

H100 (Hopper)



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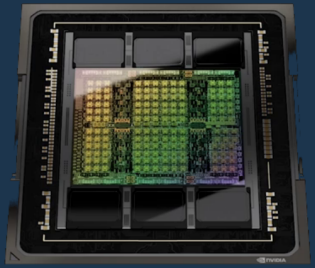
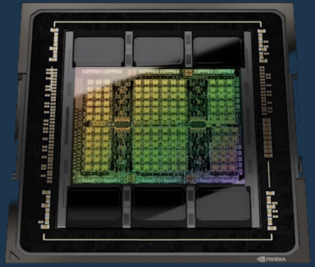


H100 SXM5 and PCie

Hardware evolution

4 nm (A100 7 nm)

H100 (Hopper)



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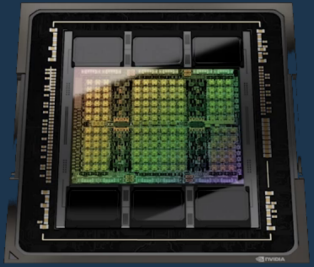

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Compute Capabilites 9.0

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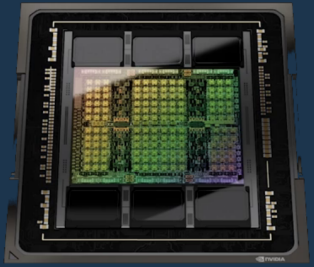

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132 SMs (tensor core Gen4) 8448 Cores

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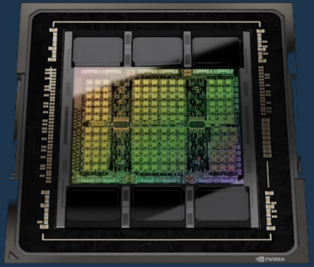

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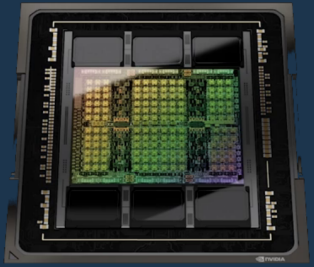

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3 TB/s Bandwidth (HBM3)

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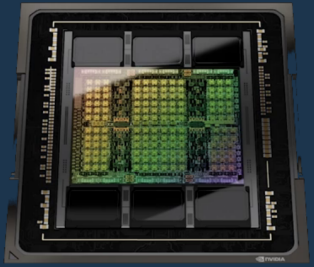

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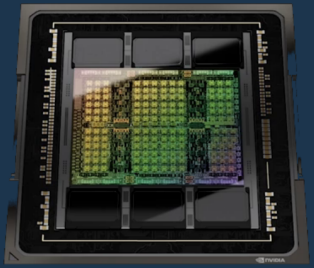

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MIG Gen 2 with confidential computing
(all instances have Image/Video decoding)

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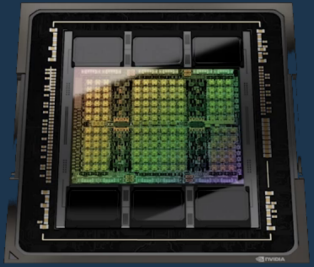

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A lot a computing precisions

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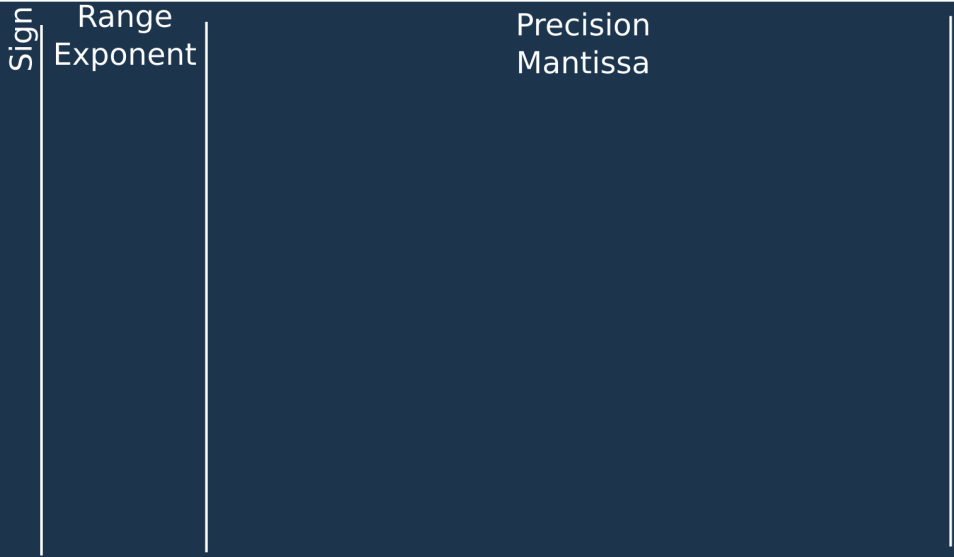

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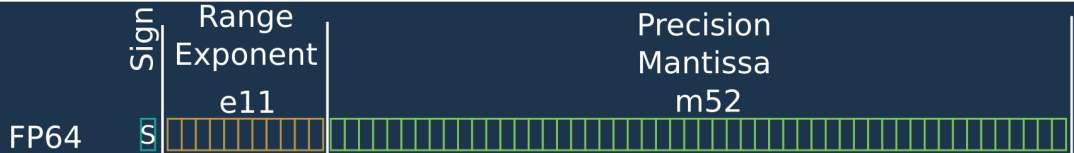

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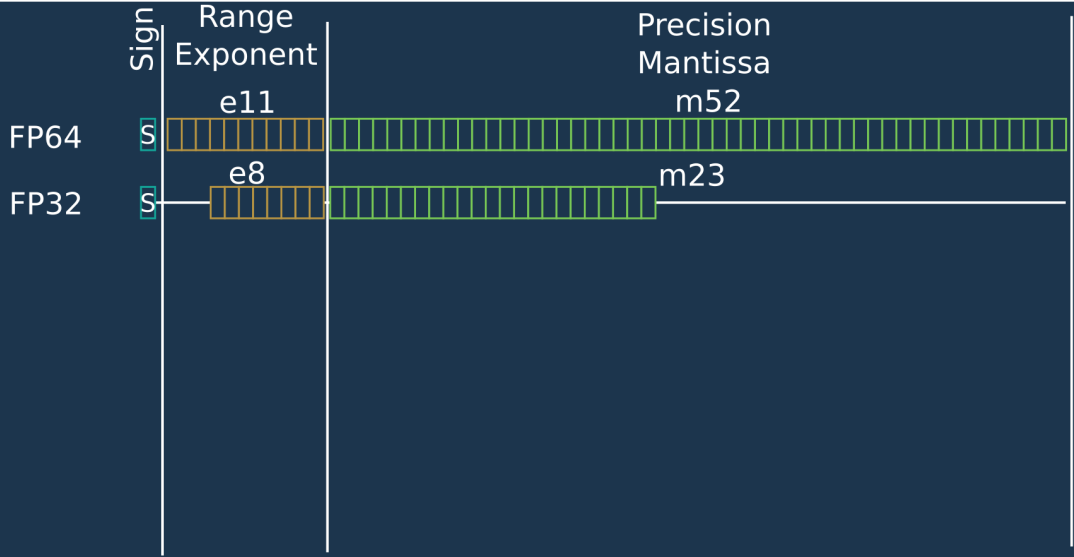

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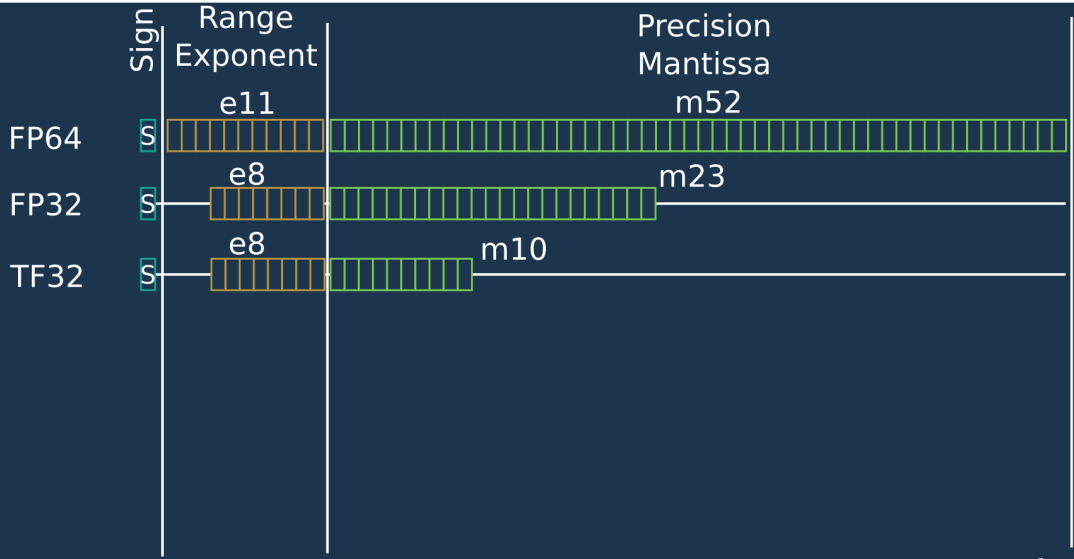

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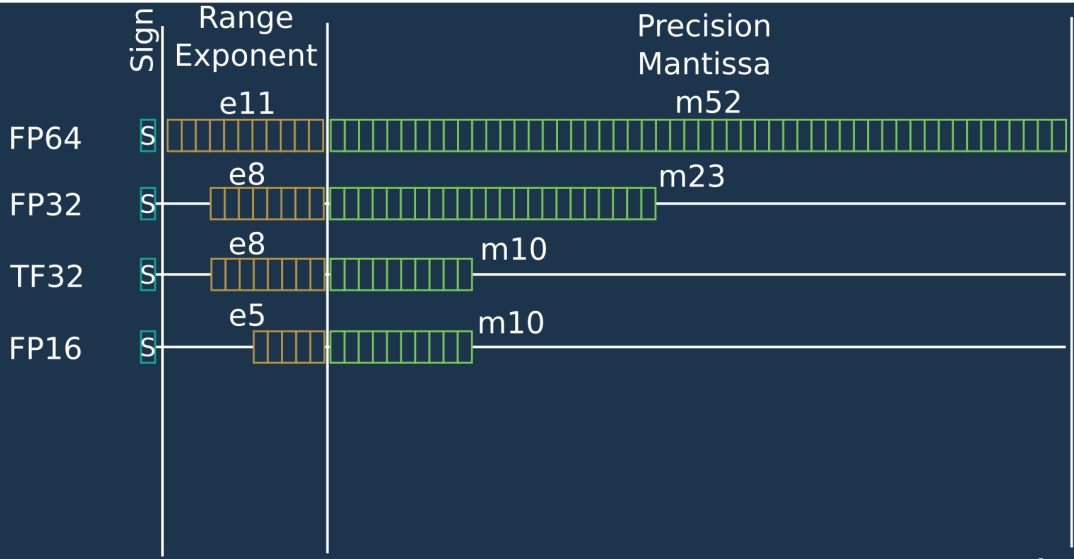

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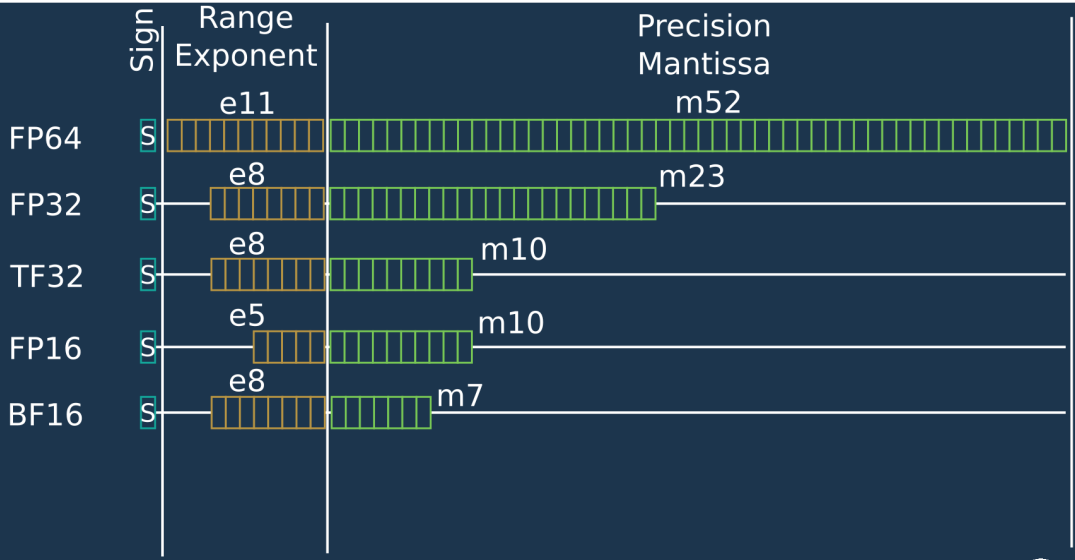

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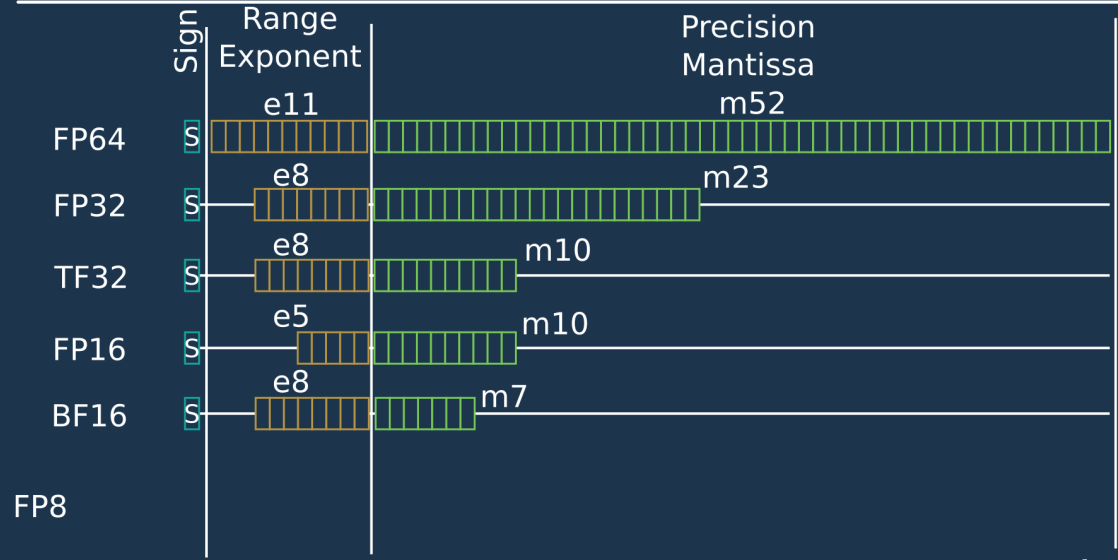

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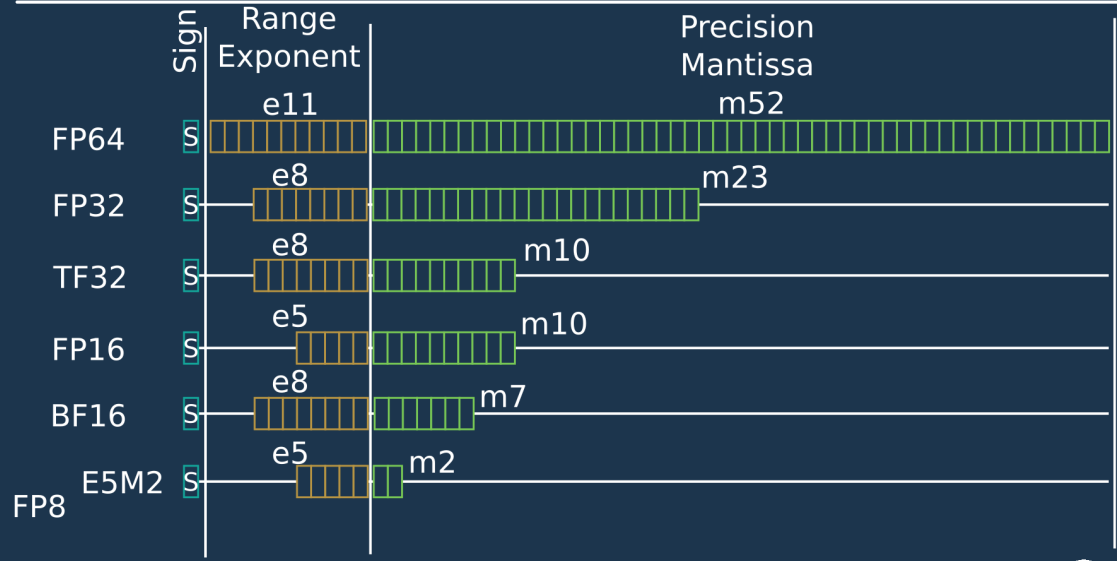

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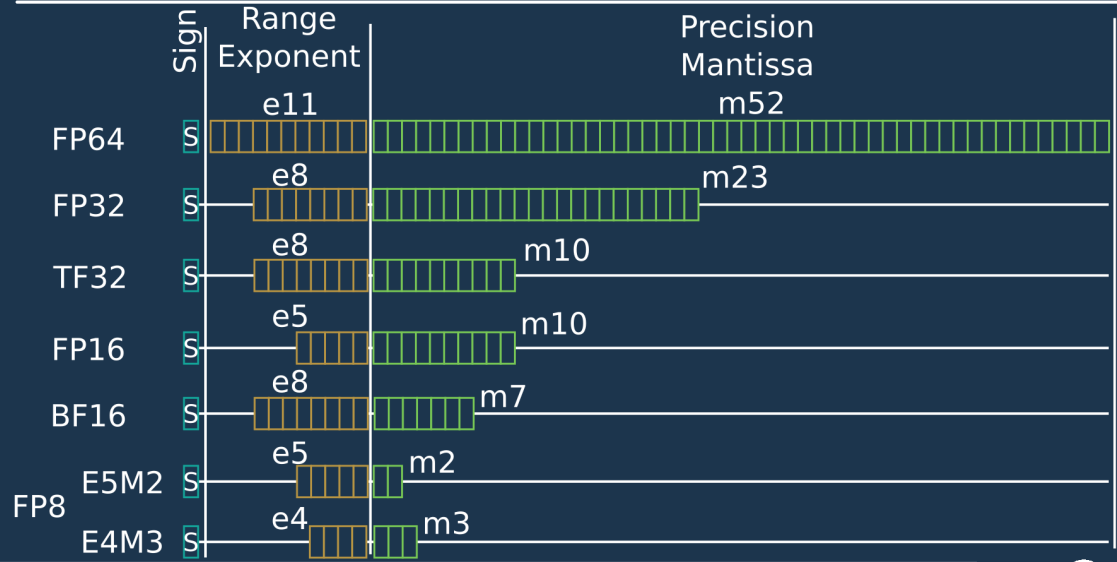

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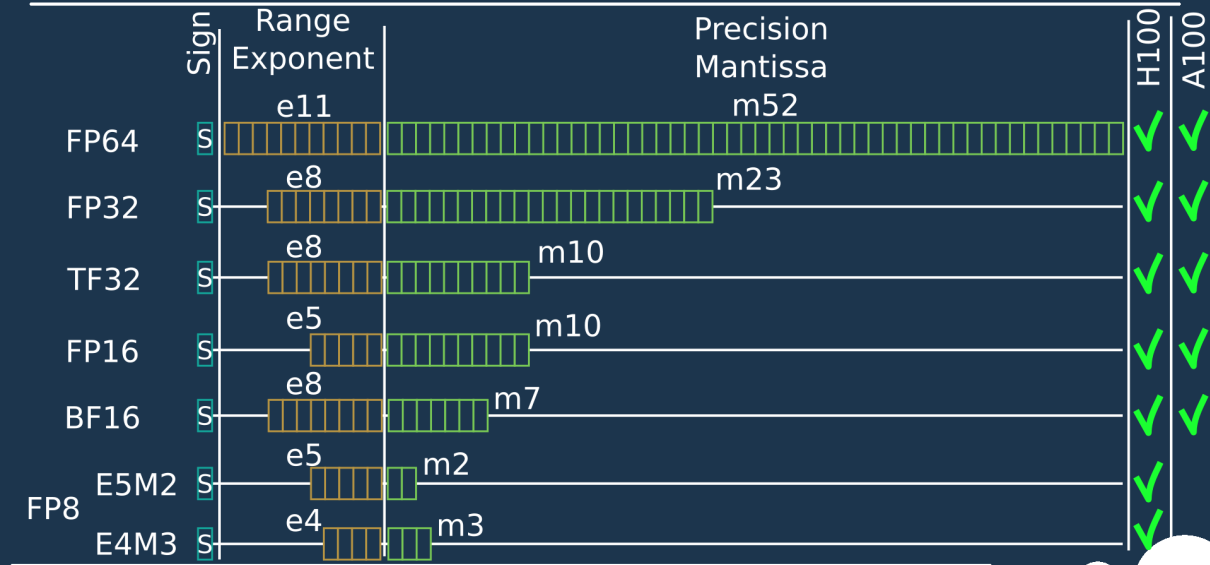
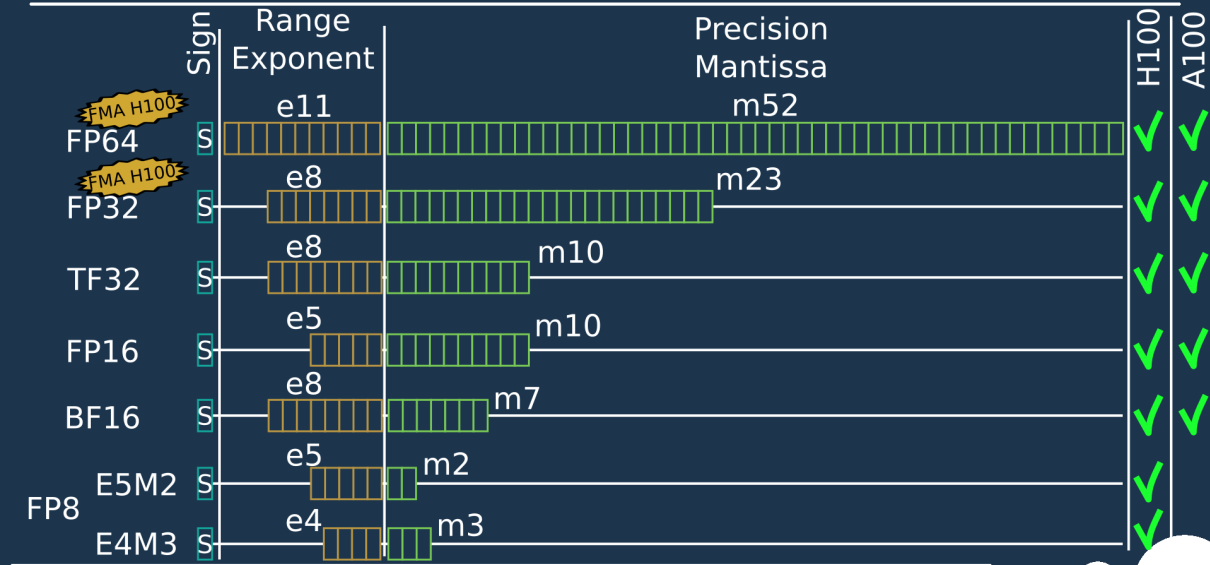


Computing Precision



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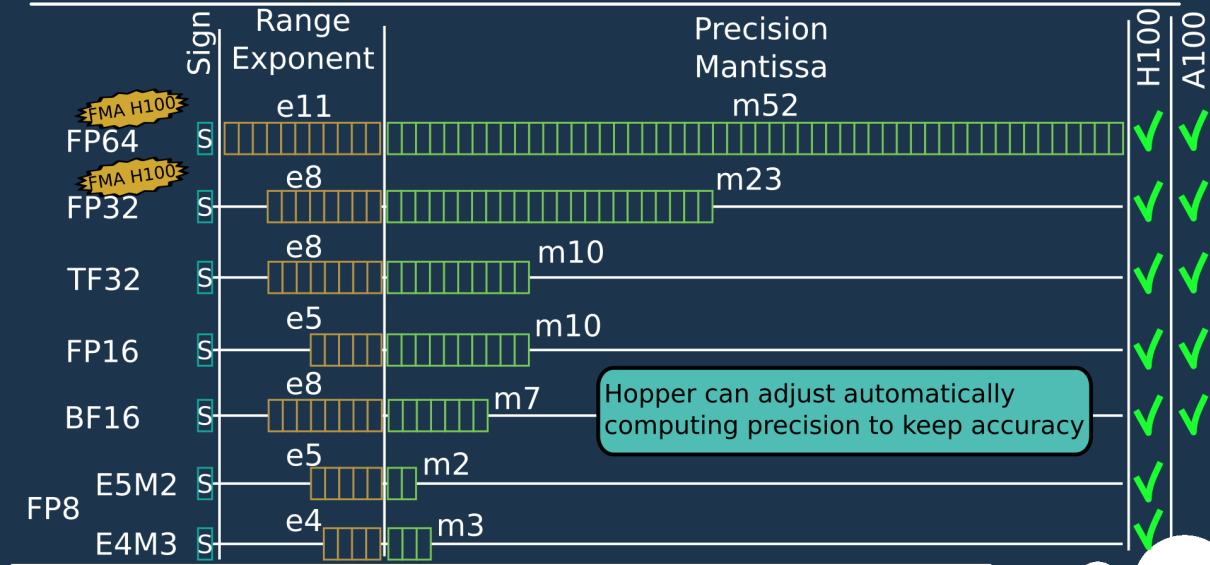
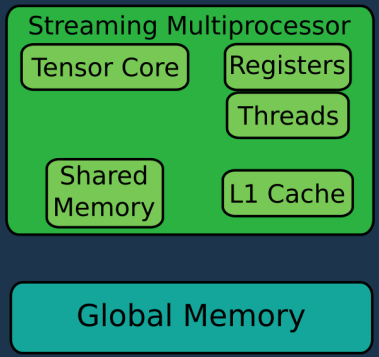


Thread acceleration

Thread acceleration

Tensor Memory Acceleration (TMA)



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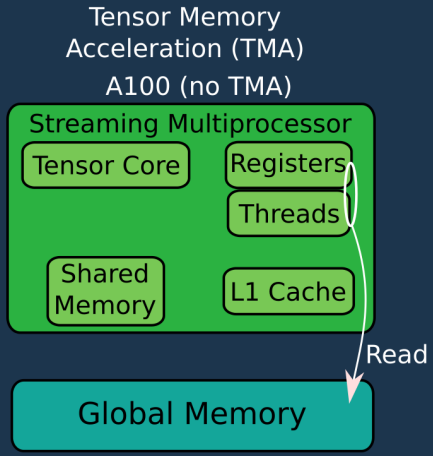

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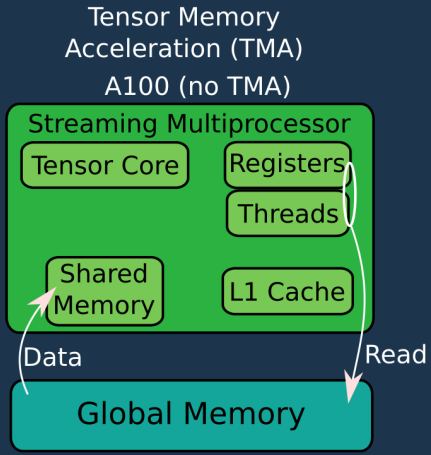

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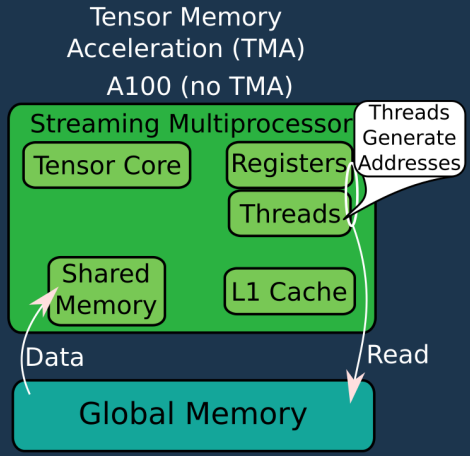

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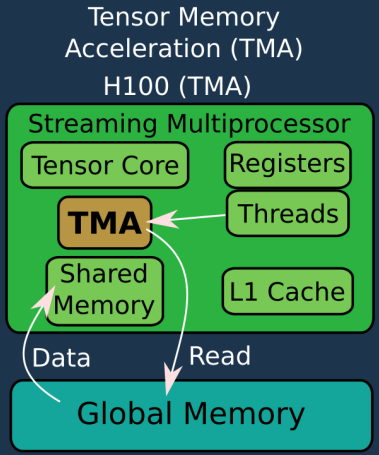

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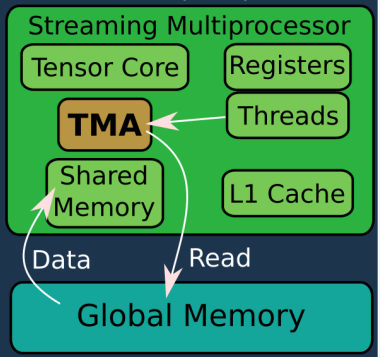
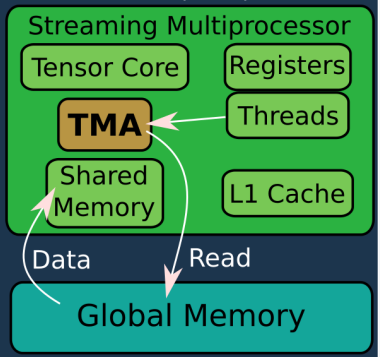


Distributed shared memory

Thread acceleration

Tensor Memory Acceleration (TMA)

H100 (TMA)



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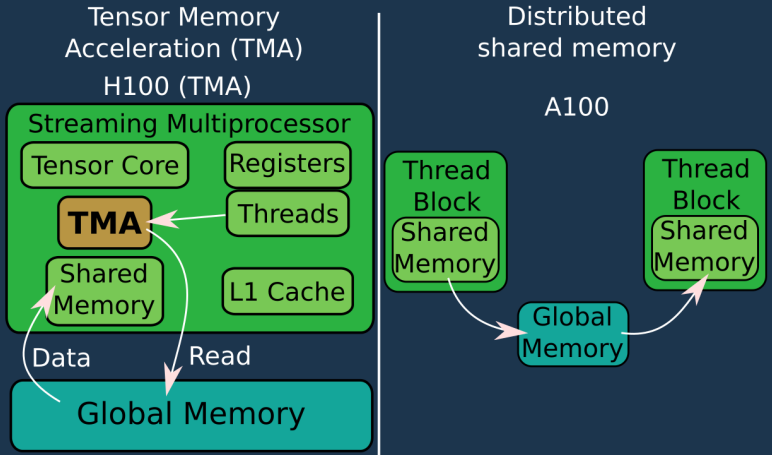

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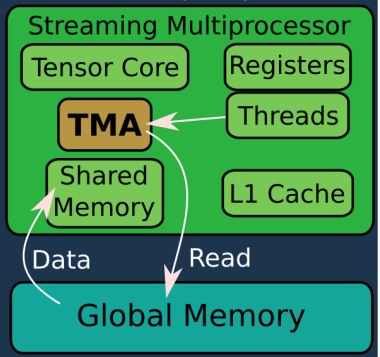

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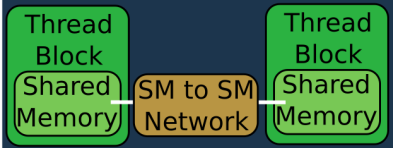

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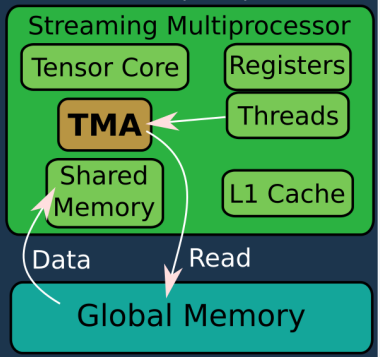

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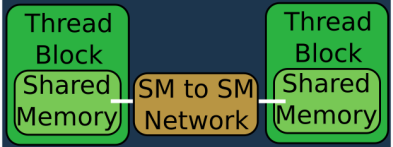

Asynchronous Transaction Barrier

Thread acceleration

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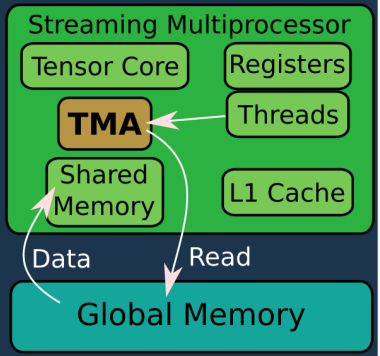

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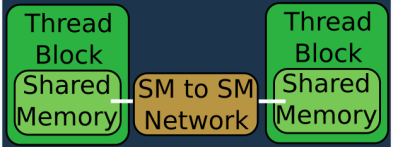

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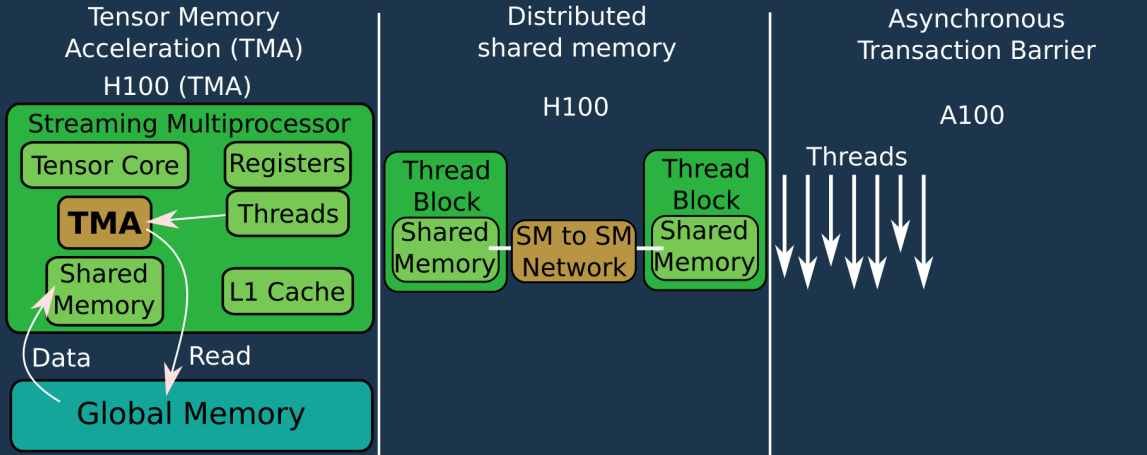

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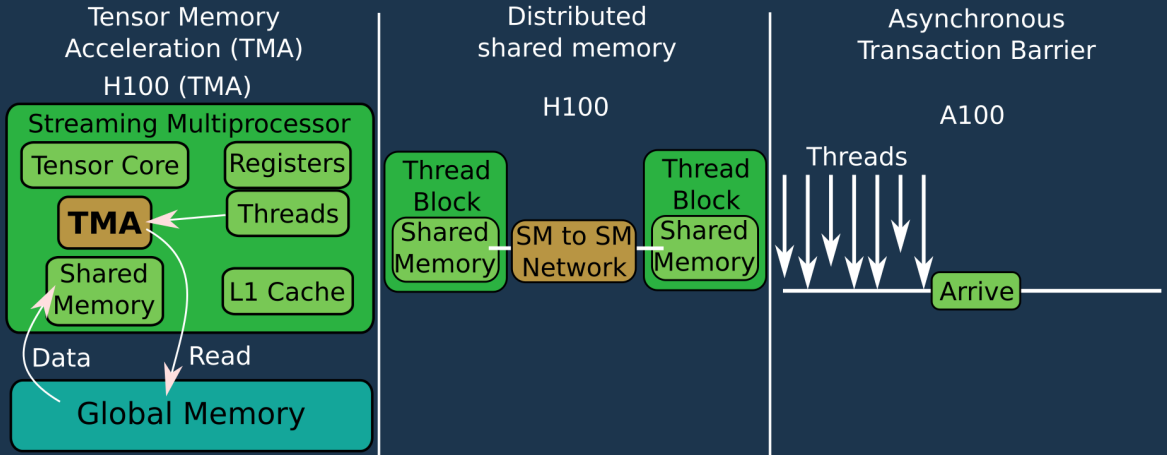

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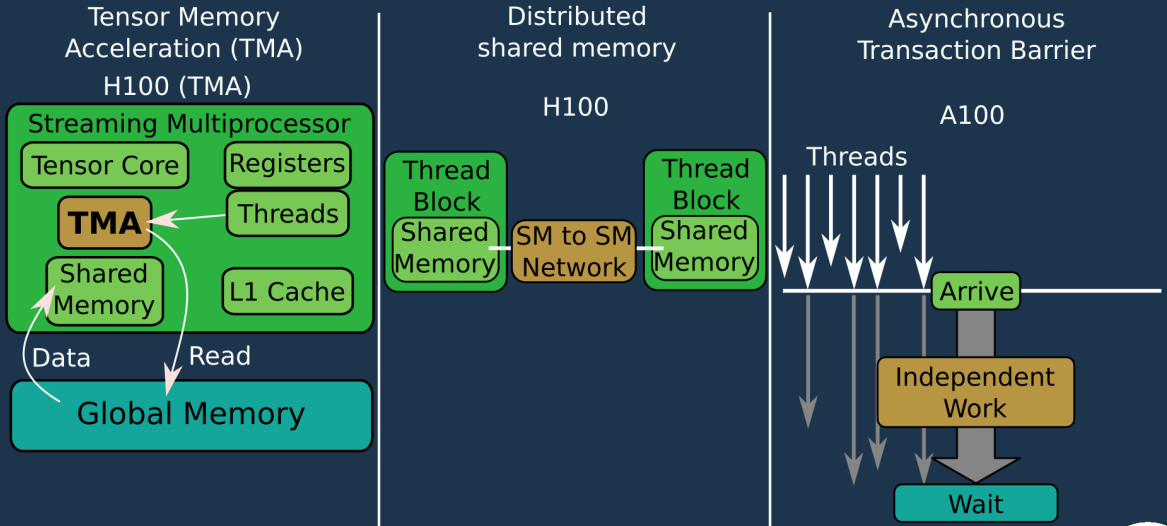

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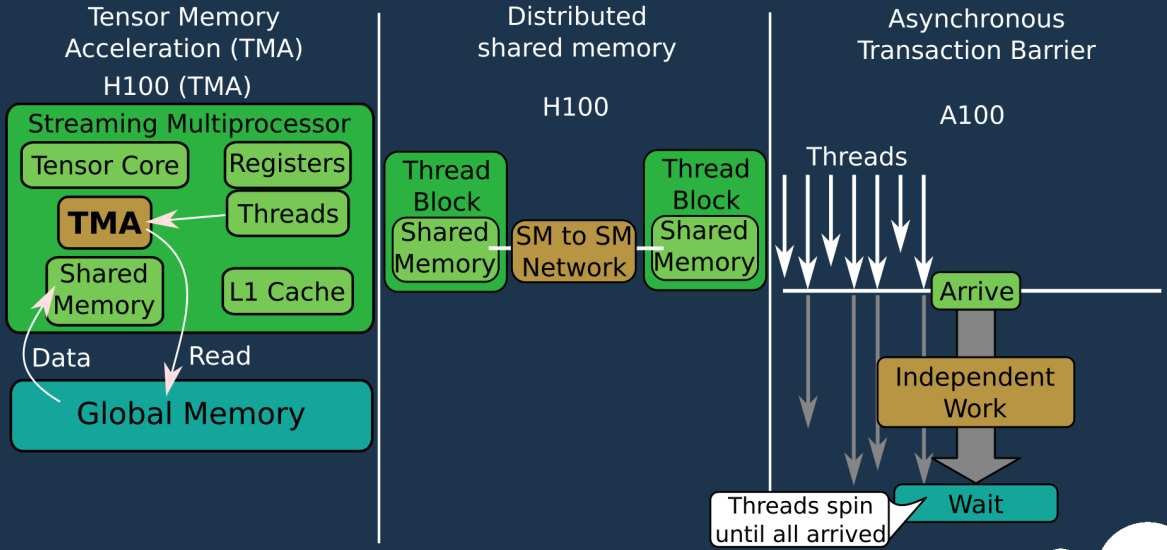

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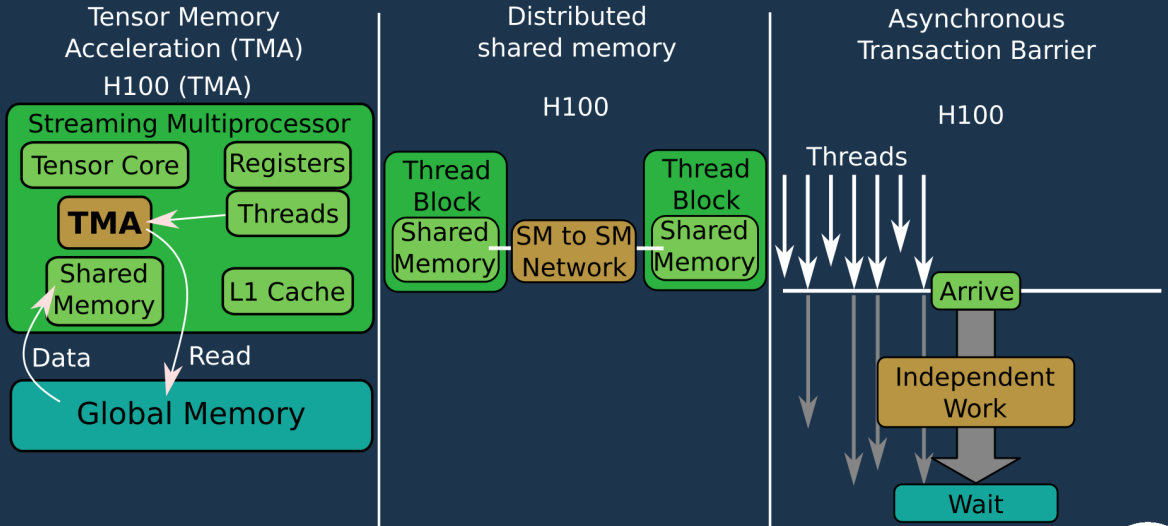

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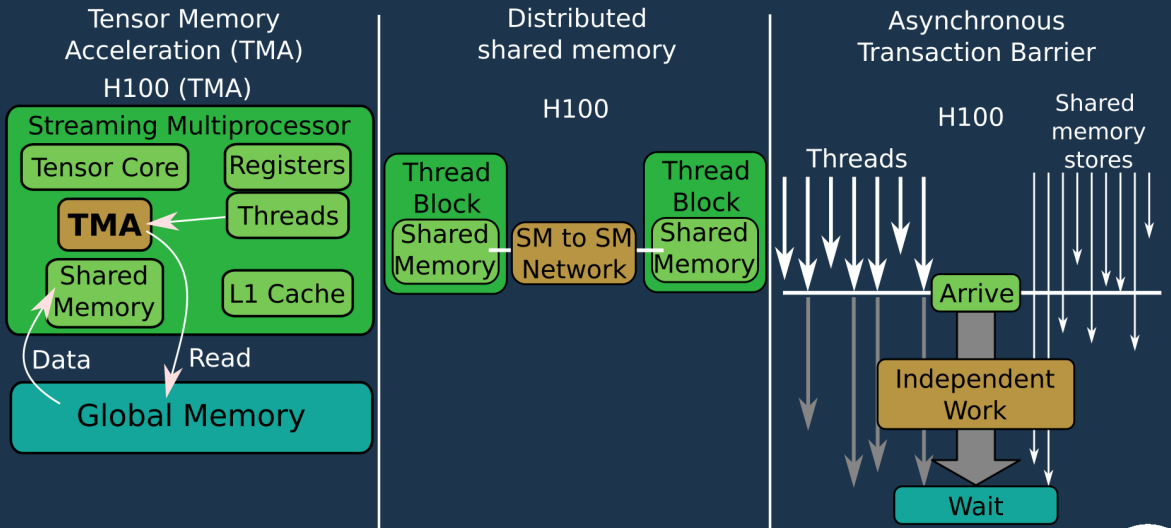

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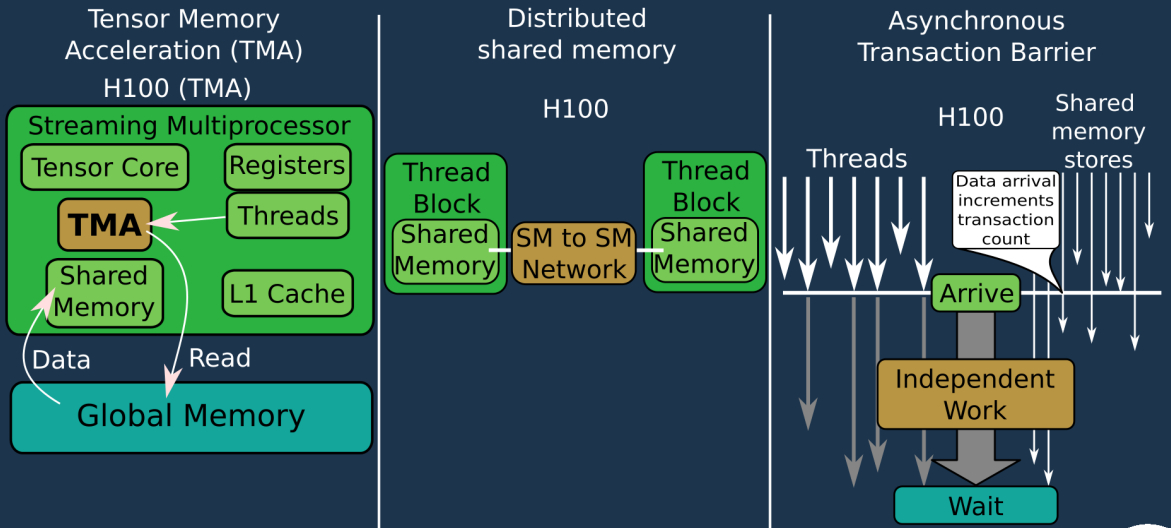

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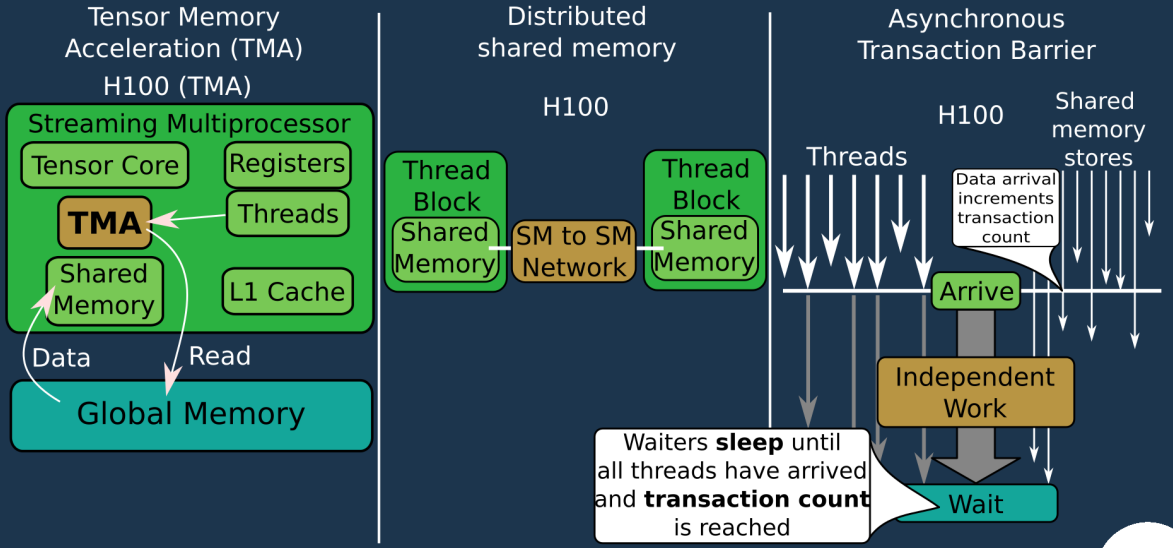

New intrinsic functions

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Dynamic Programming Acceleration (DPX) : recursive algorithms

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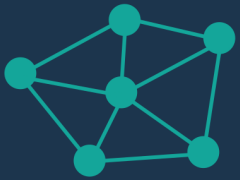
Floyd-Warshall Algorithm

Route optimization



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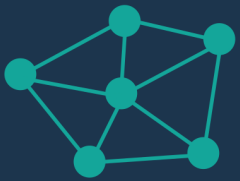
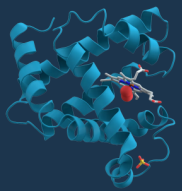


Smith-Waterman and **Needleman-Wunsch** Algorithm

Pattern Matching

- DNA sequence alignment
- Protein classification
- Protein folding



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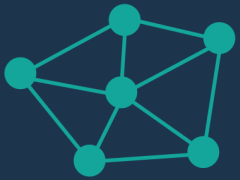

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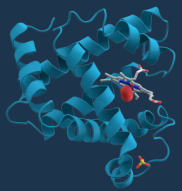
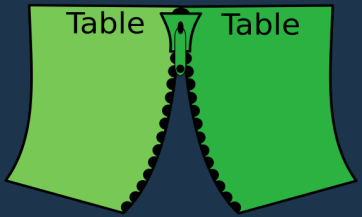


SQL Query optimisation

Join in optimal order



NVLink/NVSwitch acceleration

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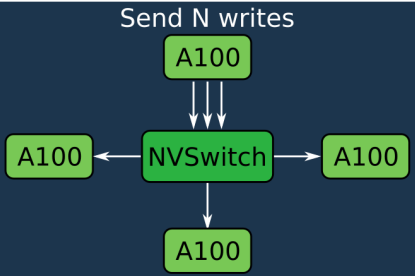
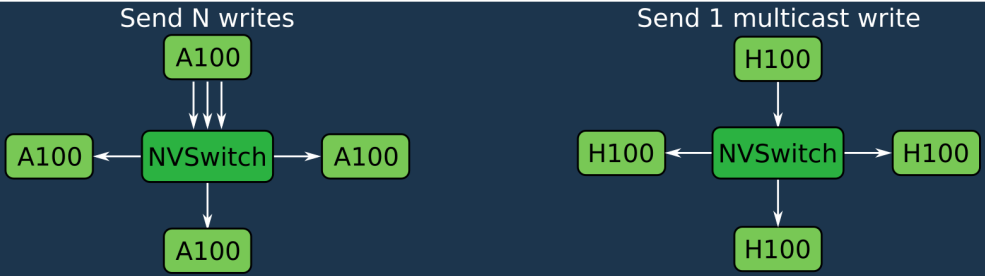


NVLink/NVSwitch acceleration



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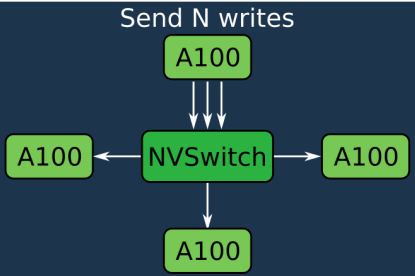

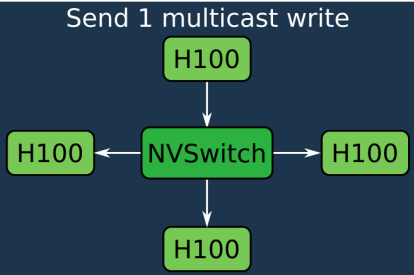

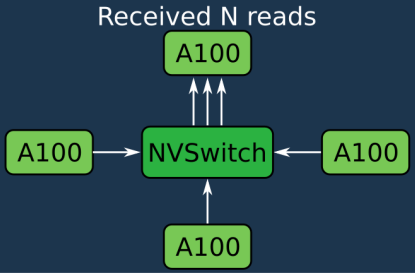

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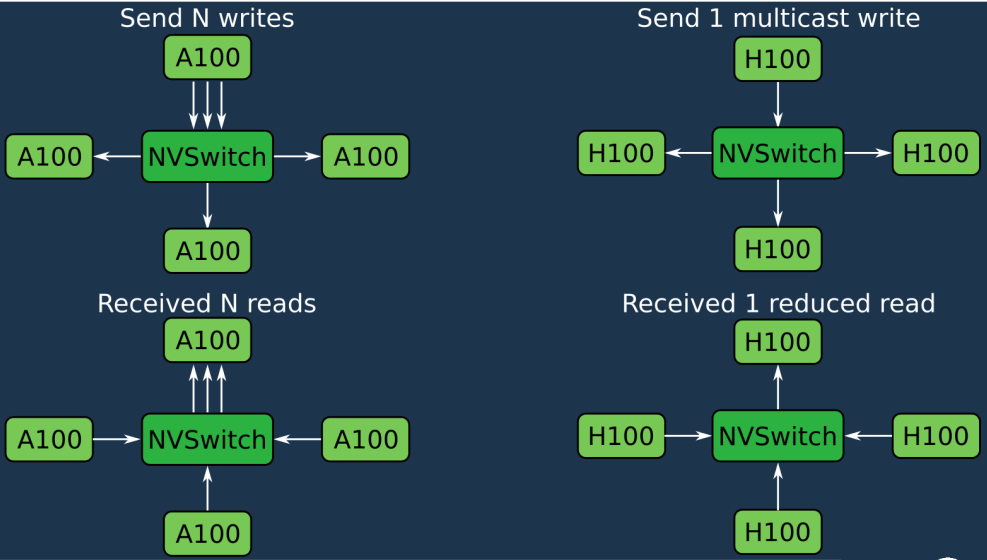

Thread block cluster

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A100 (108 SMs)

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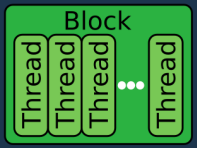

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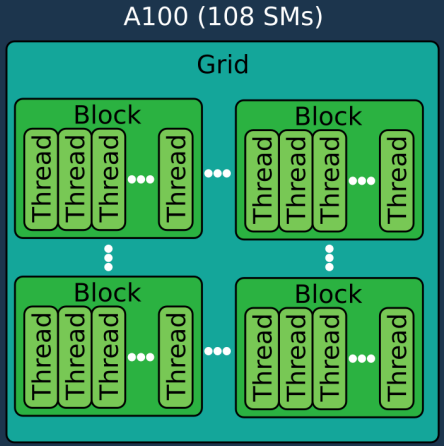

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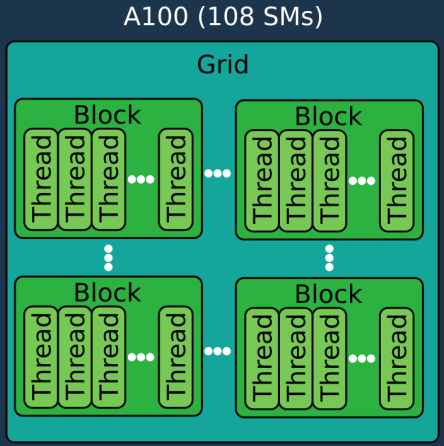

1 Block ~ 1 SM < 1% A100

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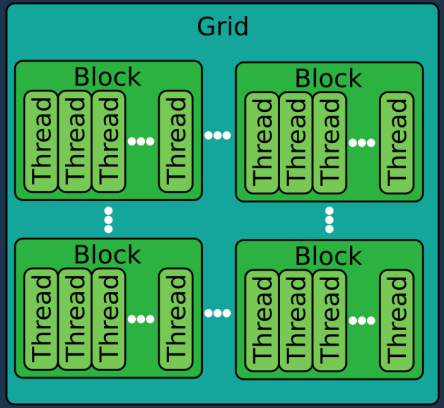

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H100 (132 SMs)

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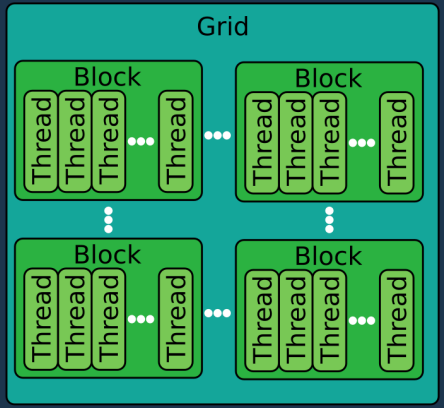

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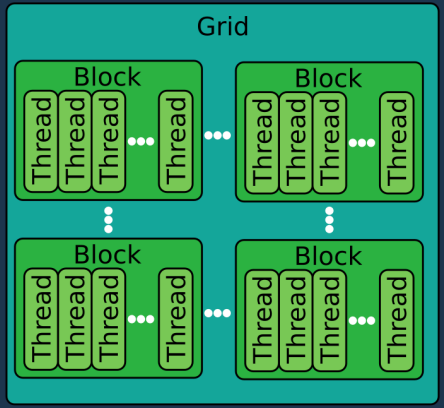

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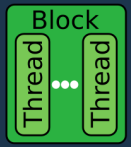

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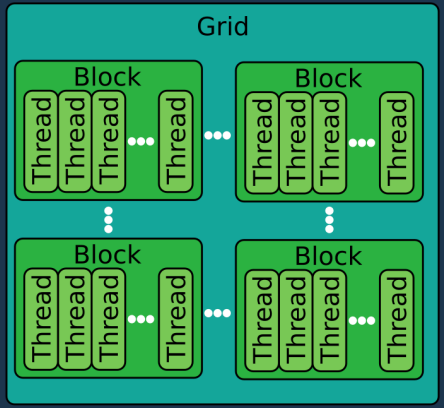

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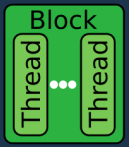

1 Block ~ 1 SM < 0.8 % H100

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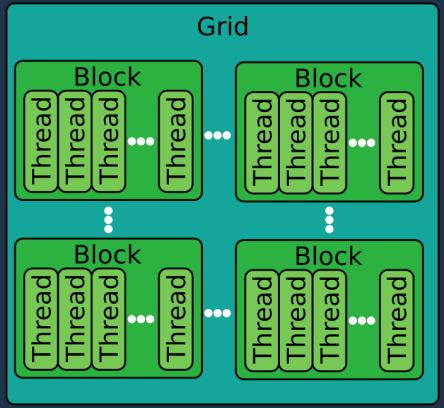

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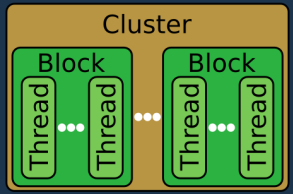

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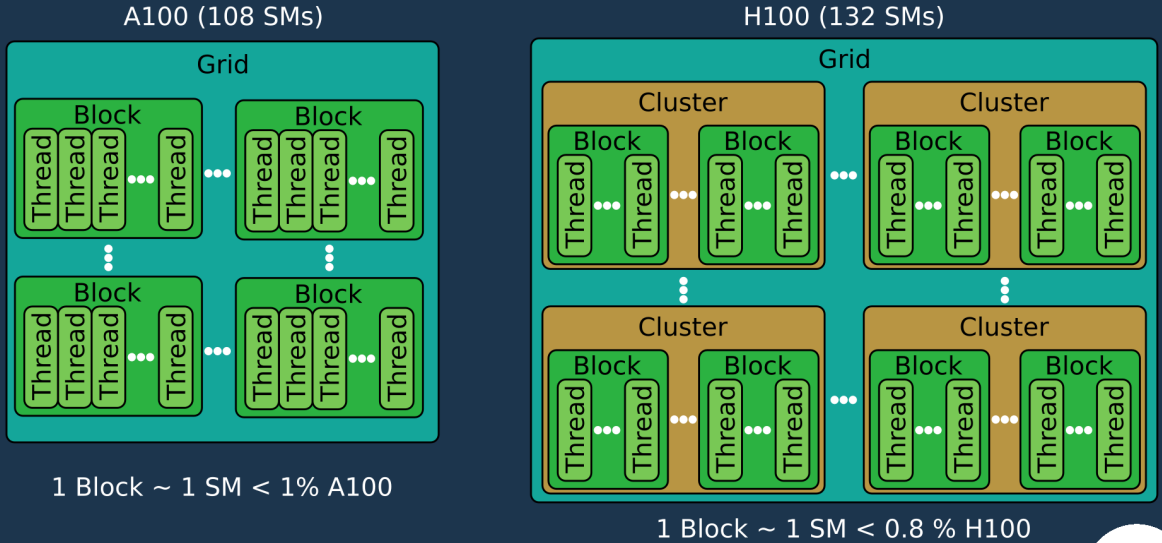
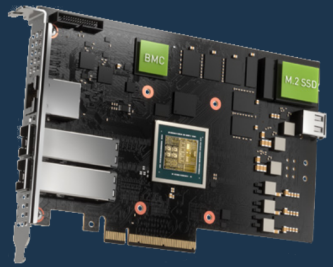


Bluefield 3

DPU : Data Processing Unit



Bluefield 3 DPU – 2x 200Gb/s
FHHL form factor

Bluefield 3

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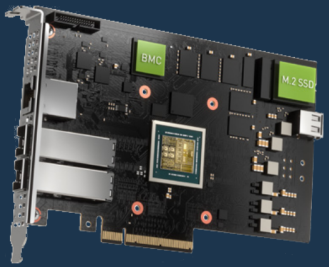

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1, 2, 4 ports with up to 400Gb/s connectivity
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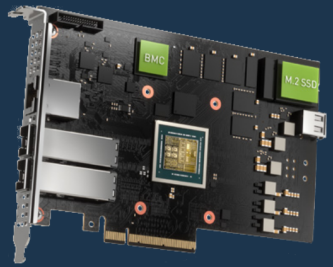

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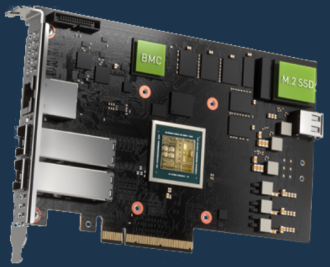

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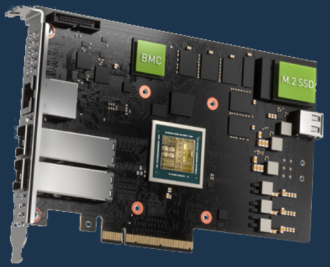

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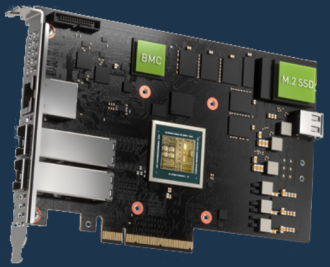

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Form factors: HHHL, FHHL

DGX H100 / DGX POD H100

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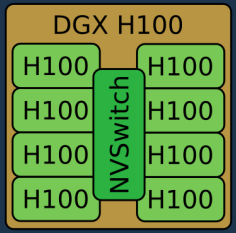

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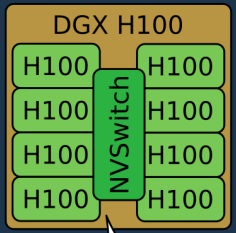

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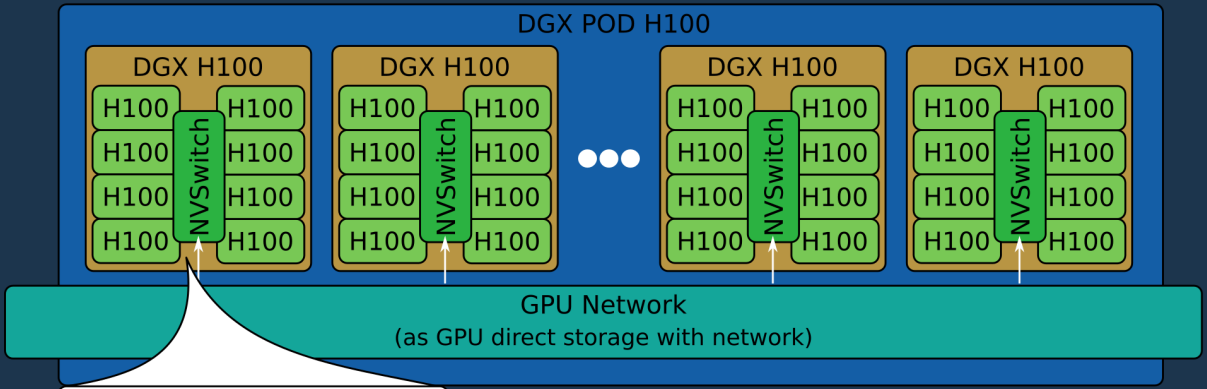

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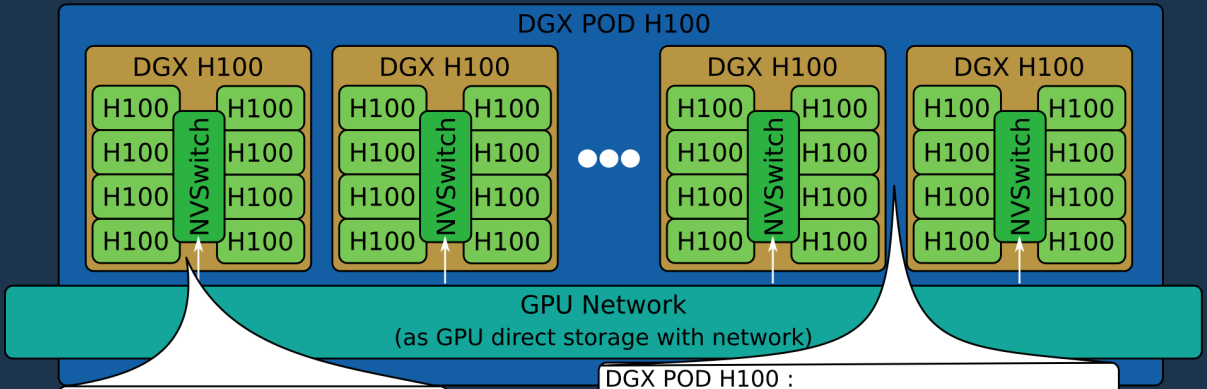

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- 1 EFlop (AI performance)
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- 70 TB/s memory Bandwidth
- 192 TFlops of Sharp in-Network compute

Grace architecture 2023

Grace Supership

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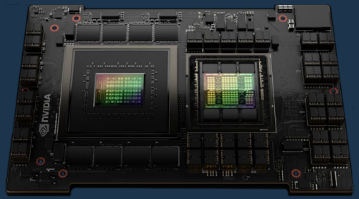
Grace Supership



Grace Hopper

Grace architecture 2023

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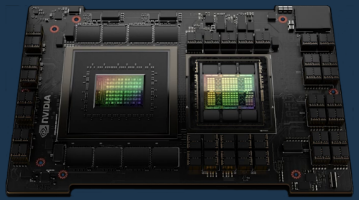
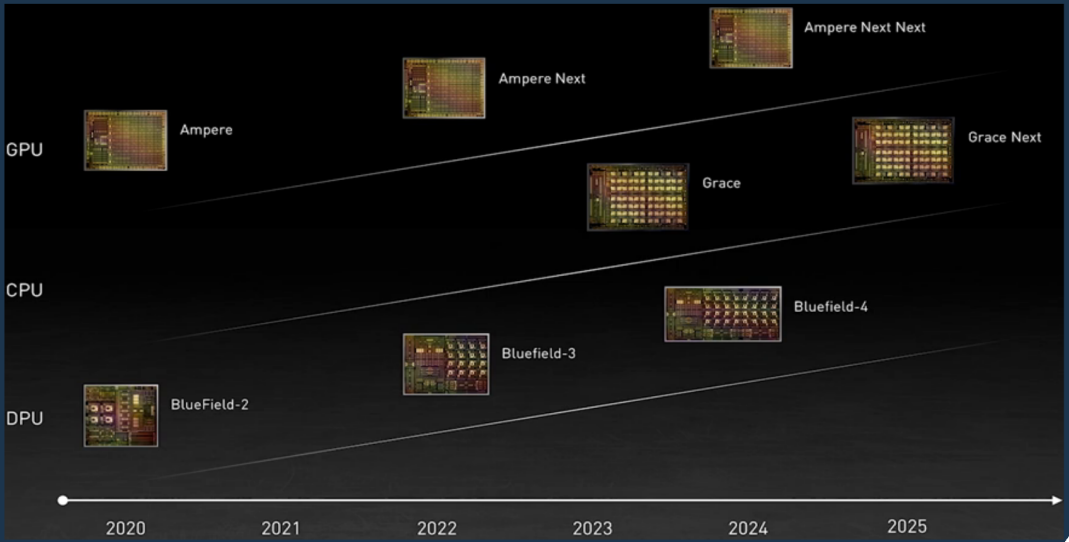


Grace Hopper

1906 - 1992

Grace architecture 2023

NVidia roadmap



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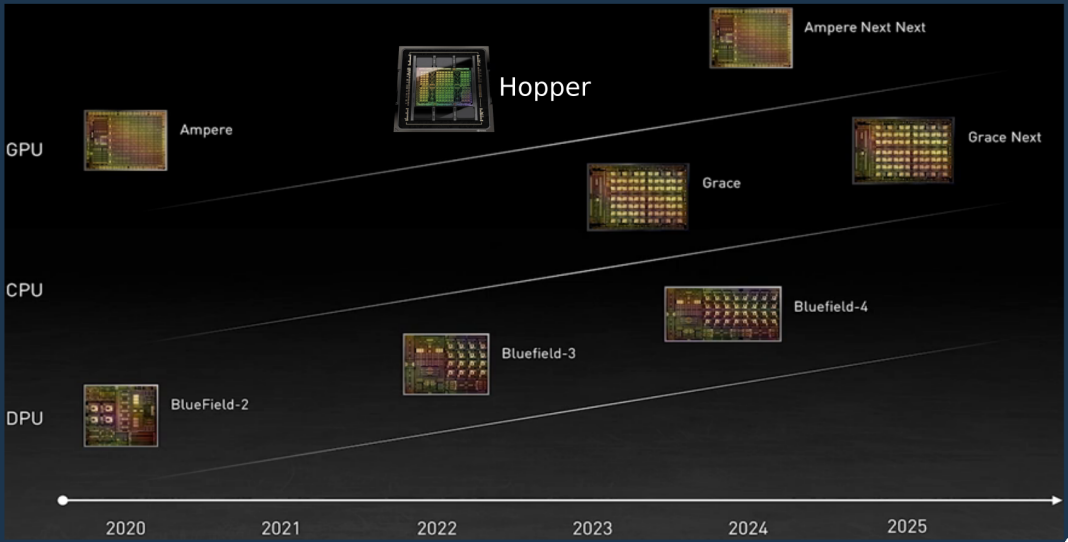

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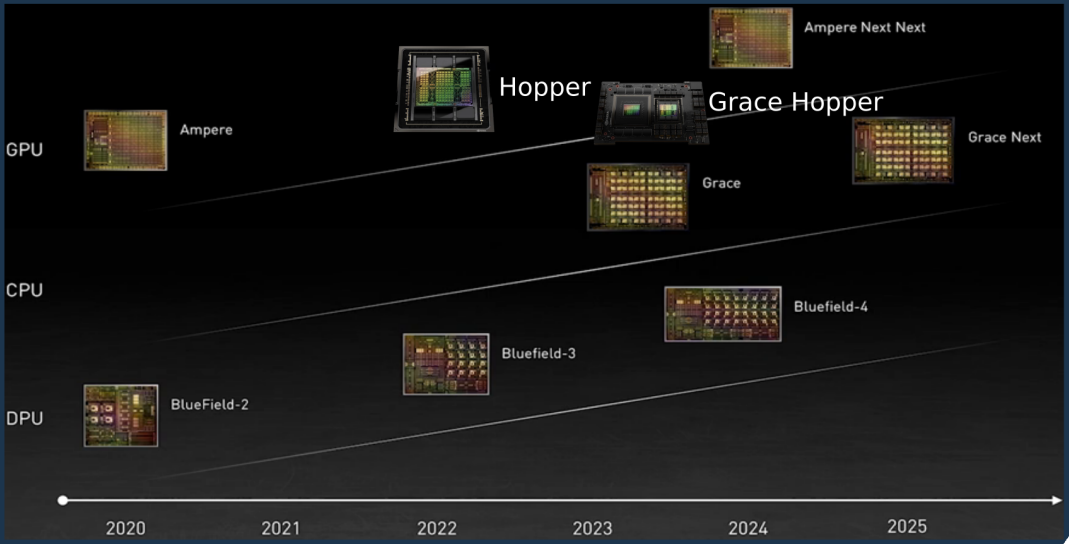

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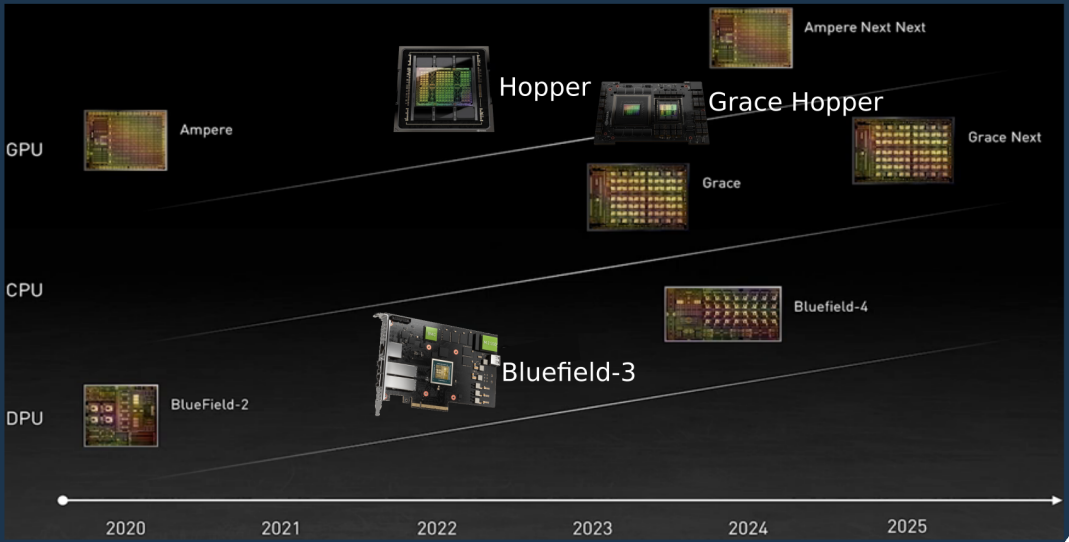

The Fermat Architecture

Fermat "Storage Attached Computing"

- Storage : **Flash**
- Computing : **ARM + FPGA**

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Extract & Label atmospheric and river feature from **8 TB** Timed Raw **NOAA Satellite**

Dell - Xeon Server :
- **2** Intel Xeon Gold 6240 @ 2.6 GHz
- **18** cores, **36** threads, 24.75 MB cache each
- **384 GB** DDR4 @ 2933 MHz
- Storage **RAID 5**, **16 x 7.67 TB** SSD
- OS : CentOS Linux release 7.6.1810

Fermat :
- **9** FPGAs
- **192 GB** DDR4 DRAM
- **8 TB** NAND Flash

Time to complete : **44 minutes**

Time to complete : **22 seconds (118x)**

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NVC++

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- Module but no cuda call

NVFortran

Uses **nvTENSOR**

Tensor Core available

Do Concurent :
- No function call
- Reduction not available yet

Compilers news

NVC++

C++17 :
- Combine **std::transform** and **std::reduce** in the same call

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- Parallelism Thread concurency

C++23 :

- Range based parallel algorithm (mdspan, mdarray)
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C++2X :

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Autodetection **GPU**

128 bits integers supported since version 11.6

Link Time Optimization (LTO)

Parallel compilation for different compute capabilities (-d -thread)

Implementation detail (-d -v) (ex: a+b)

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Fortran Forever :
- Modern Fortran >= **F18**

Link Time Optimization

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Sources

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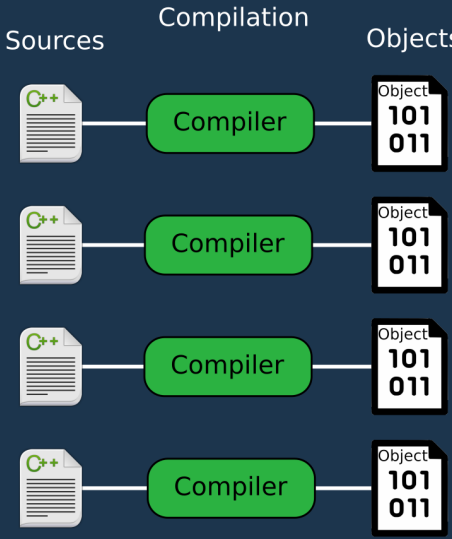

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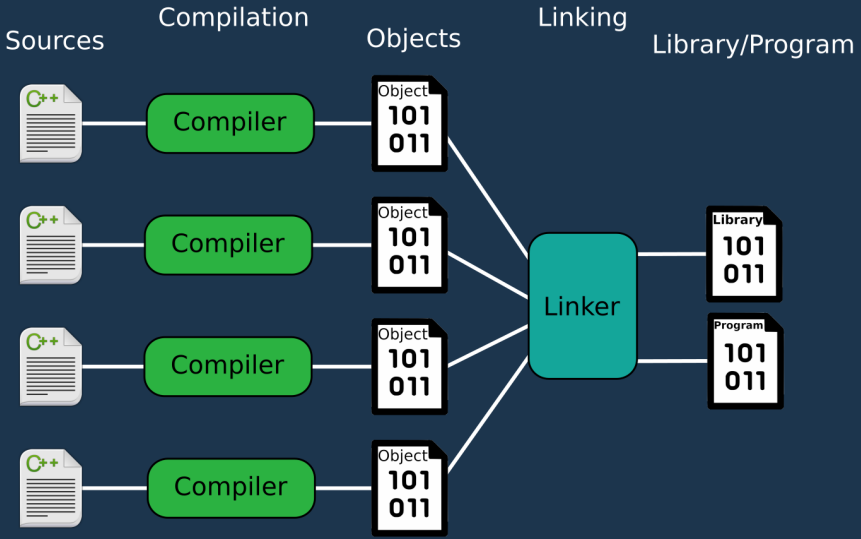

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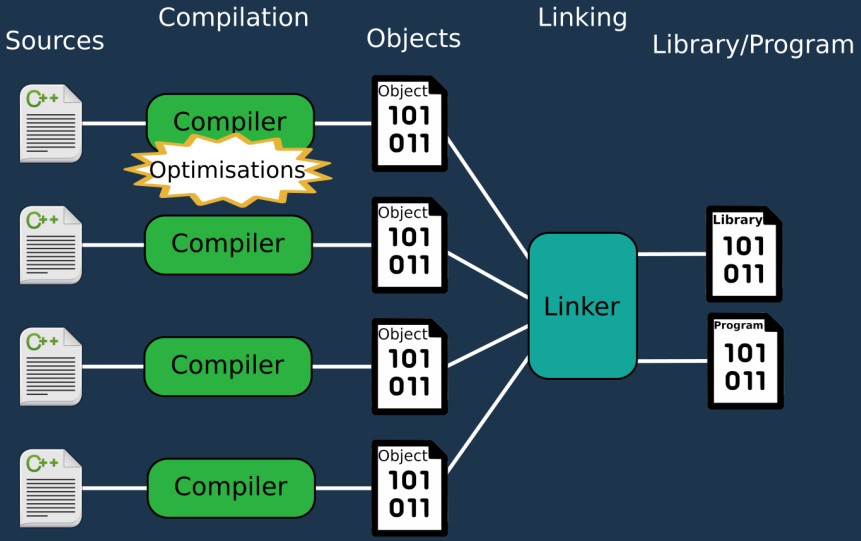

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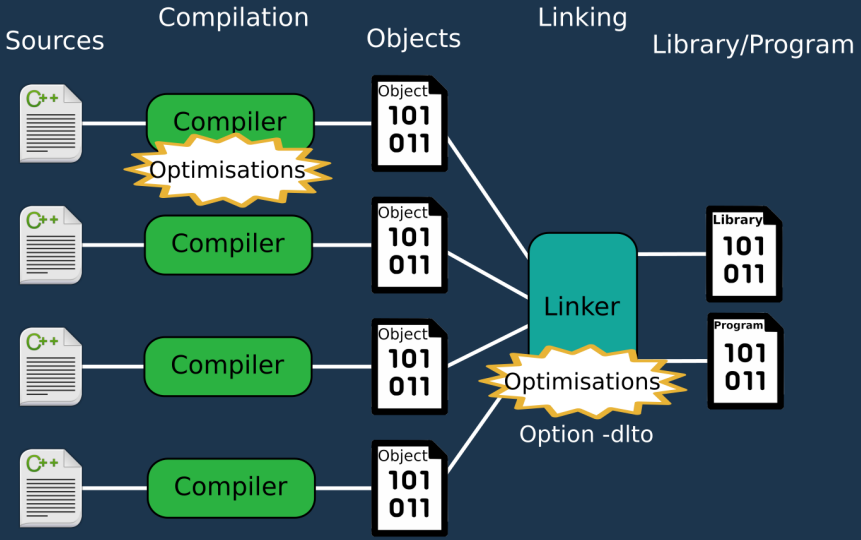

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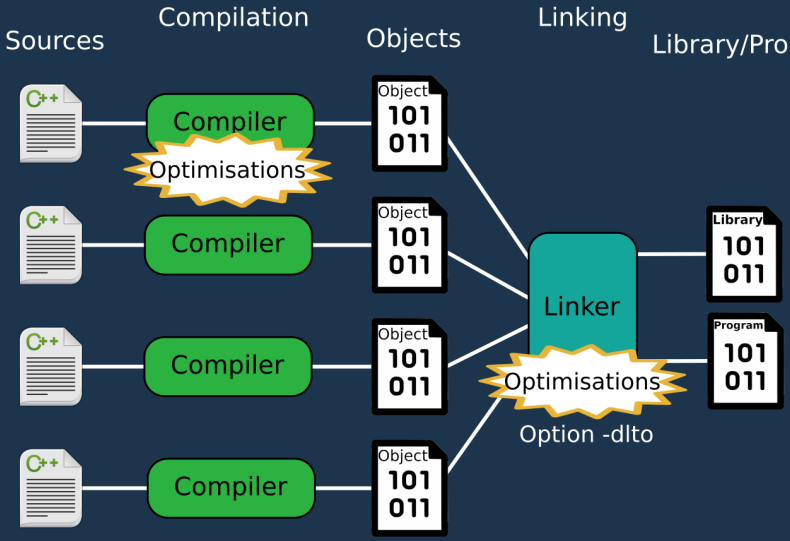

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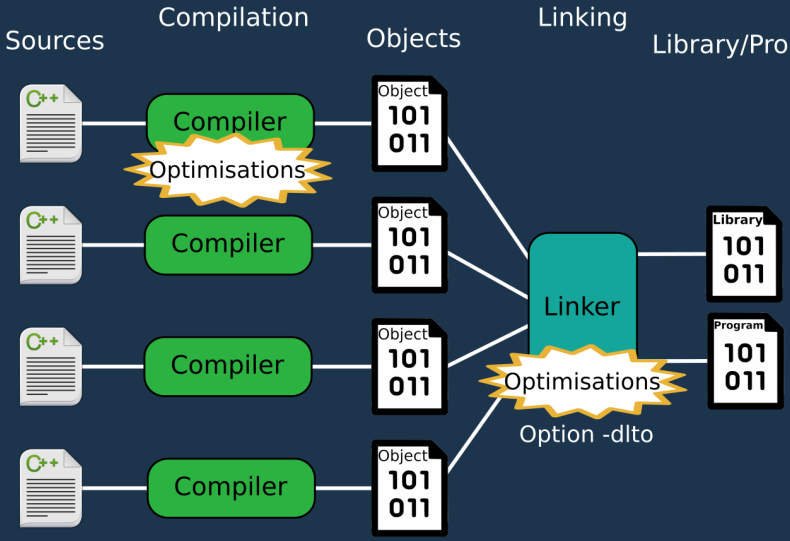

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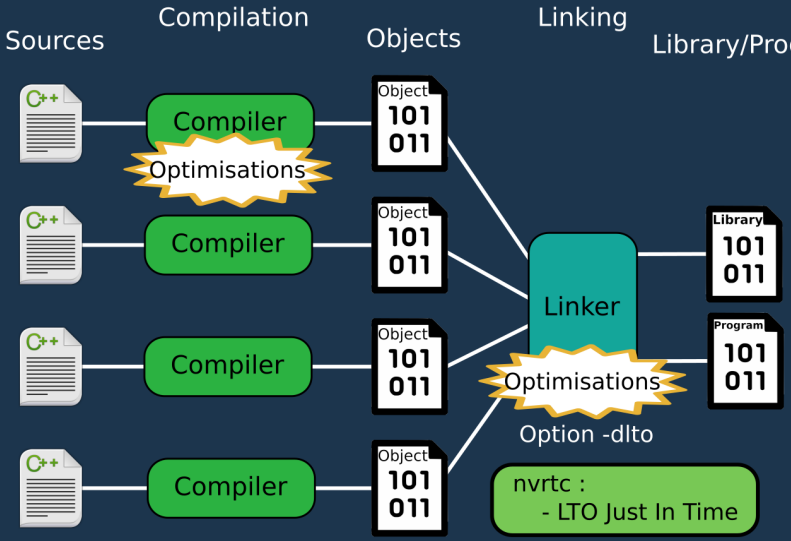

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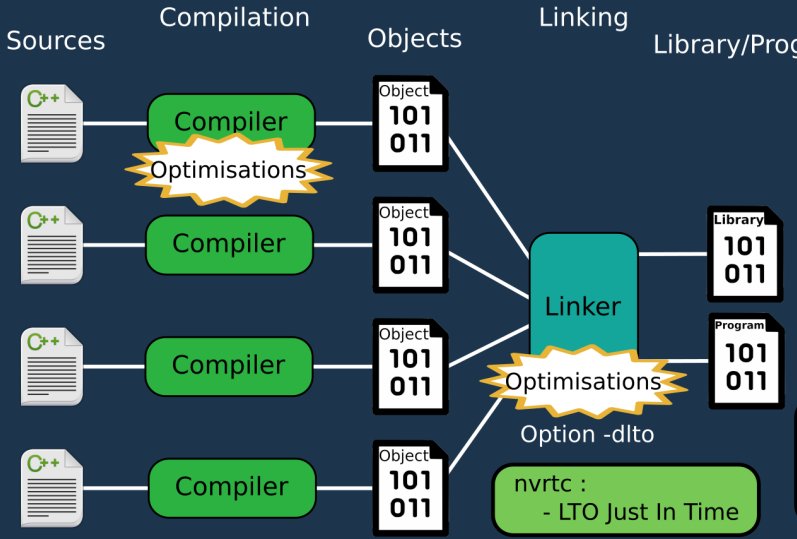

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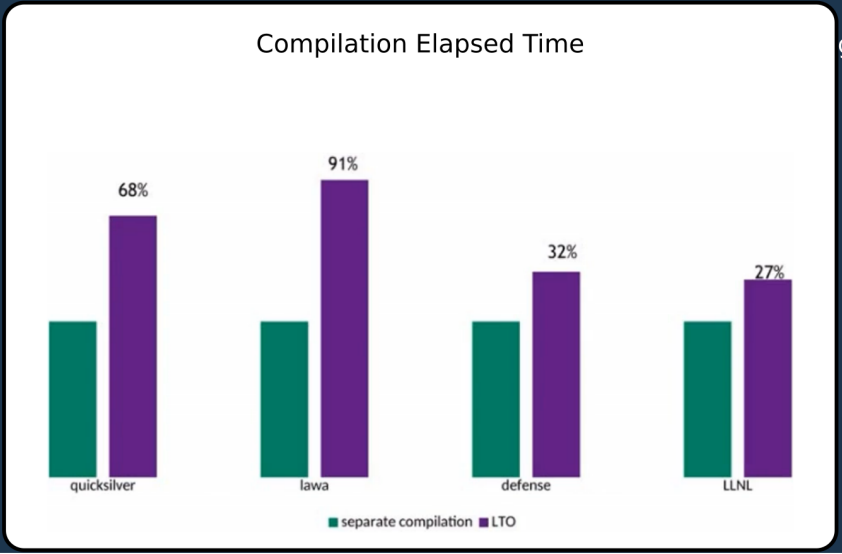

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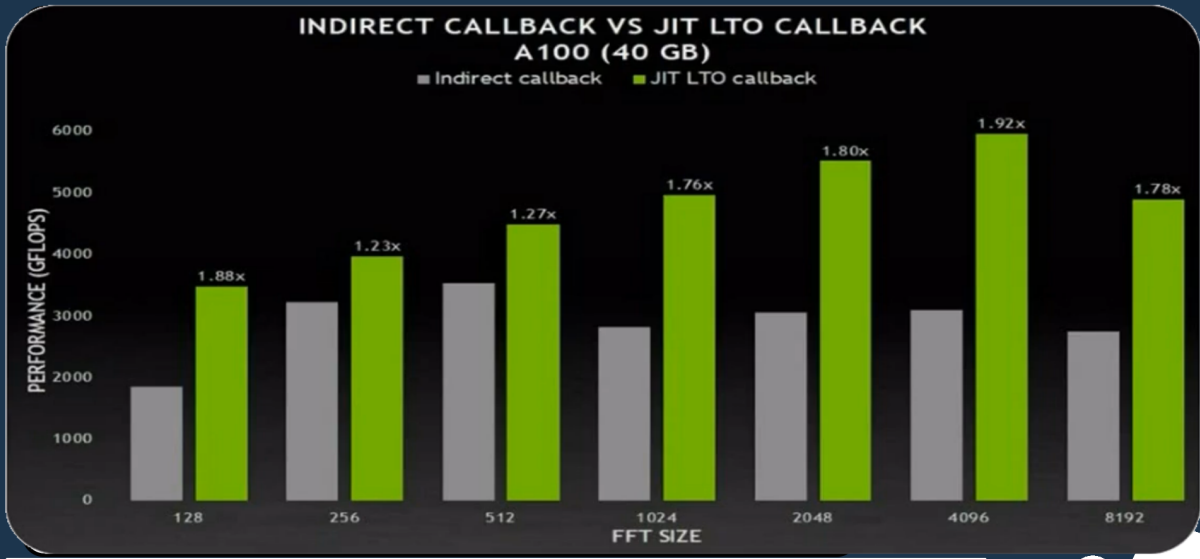

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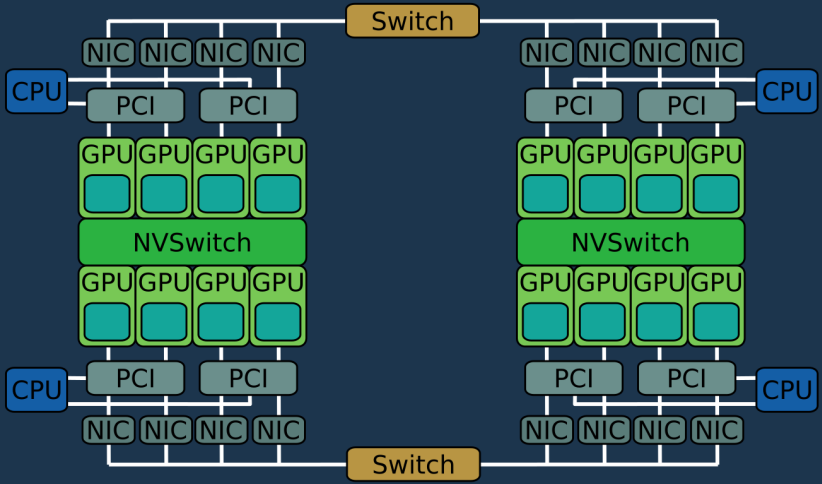

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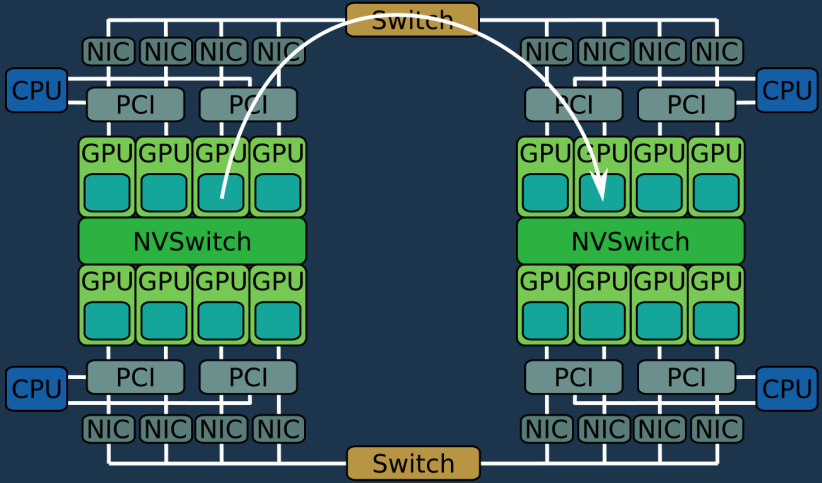

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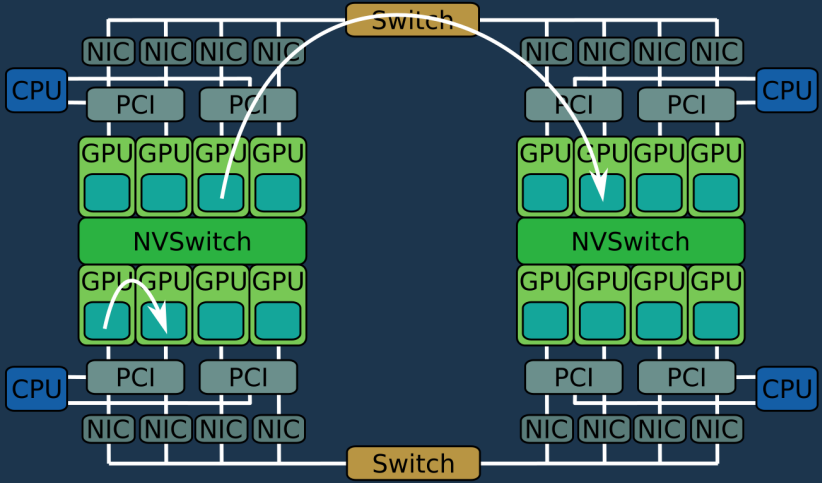

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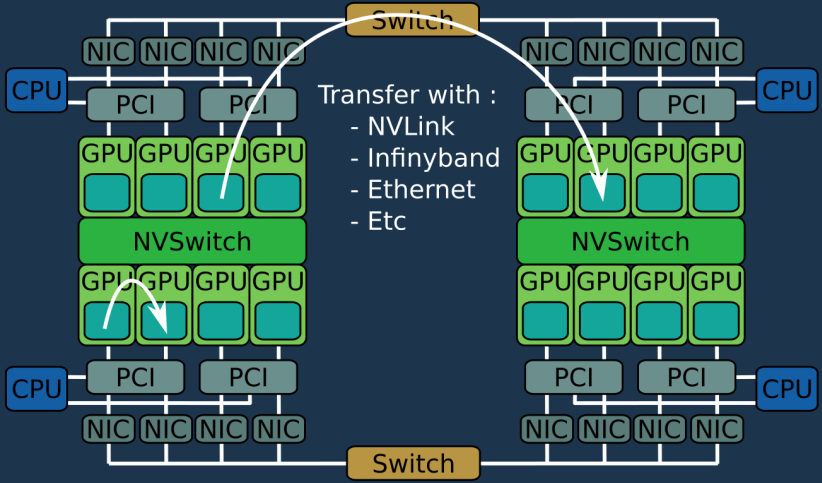

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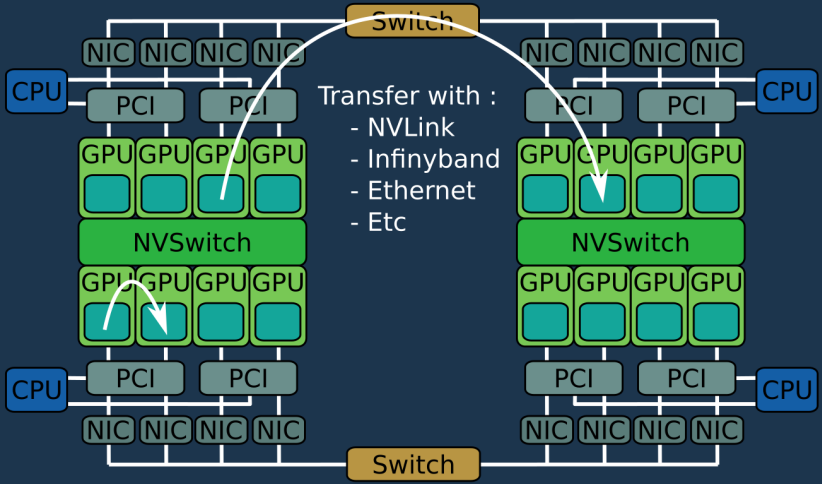
Based on OpenShmem



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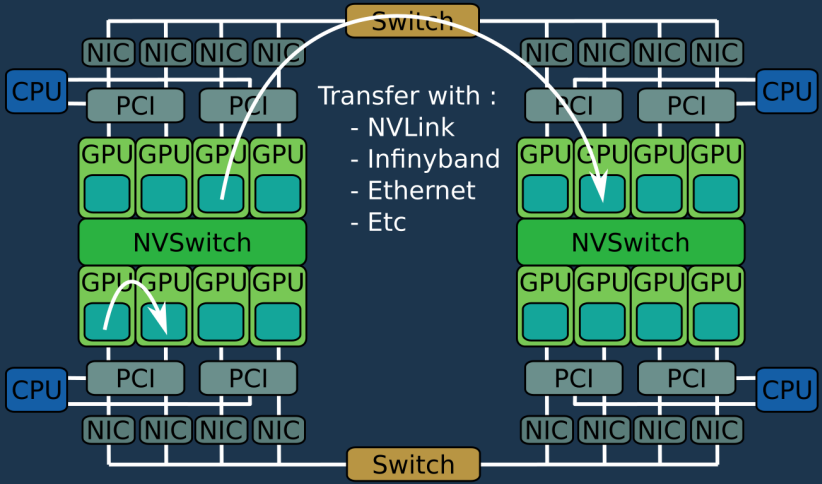
Scalable point to point communication



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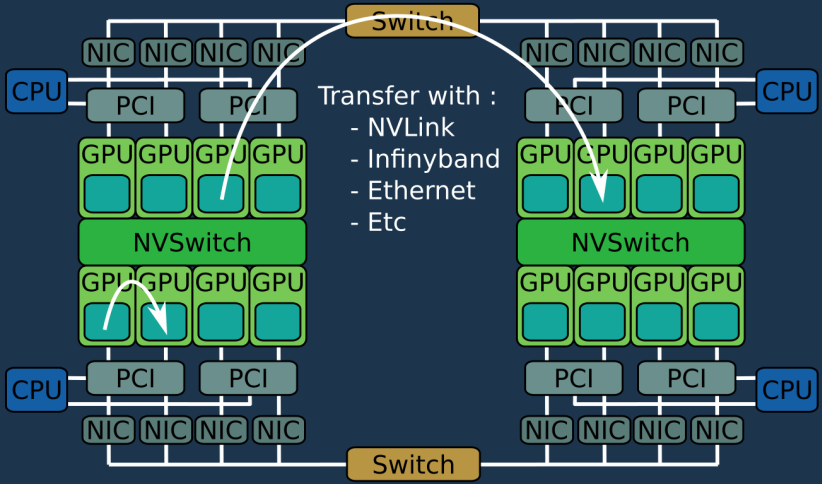

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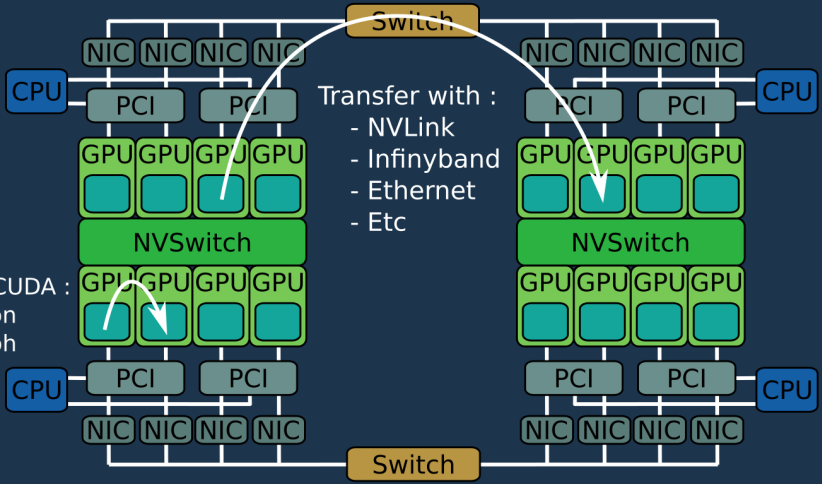

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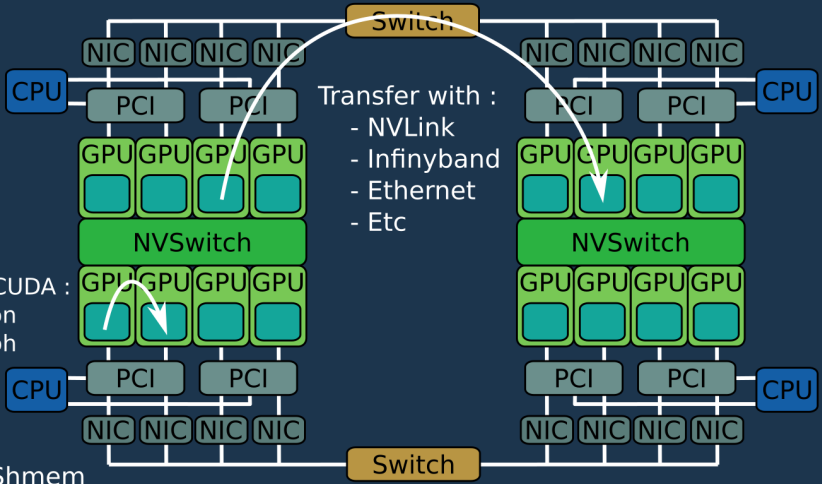

MagnumIO is based on NVShmem

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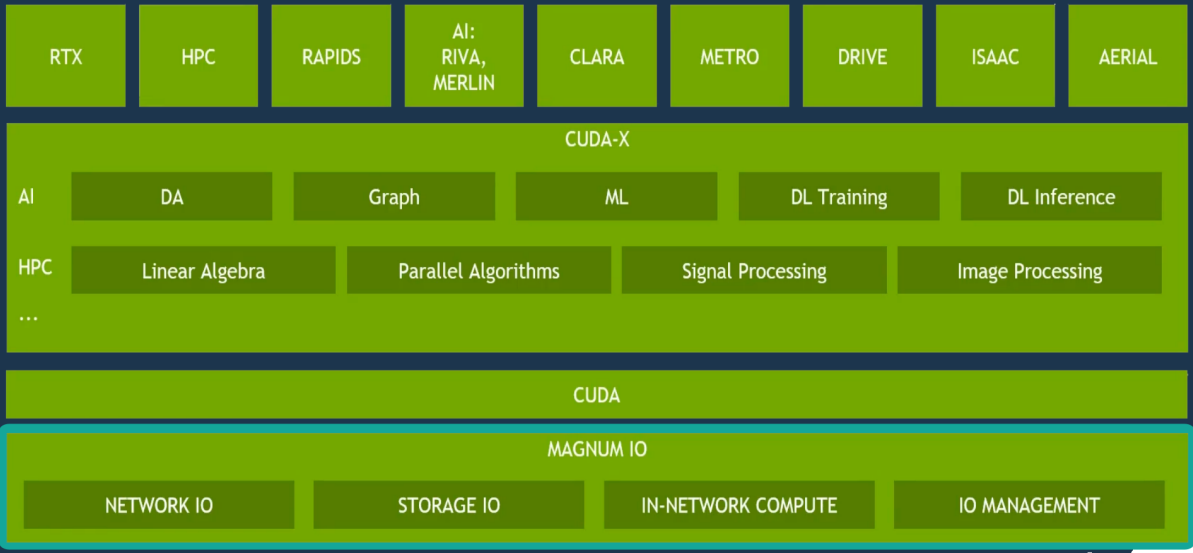

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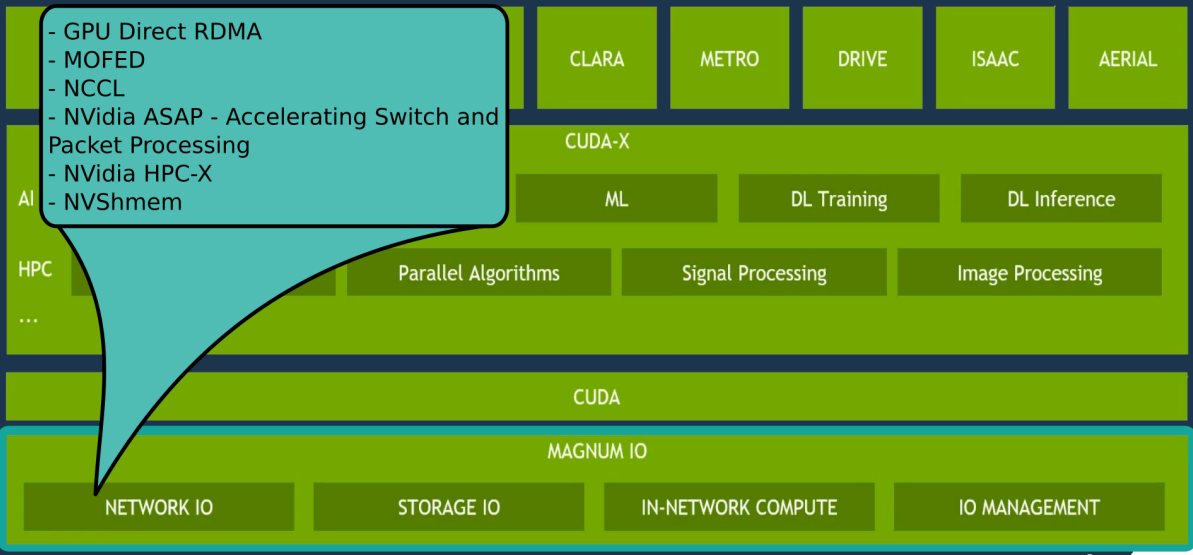

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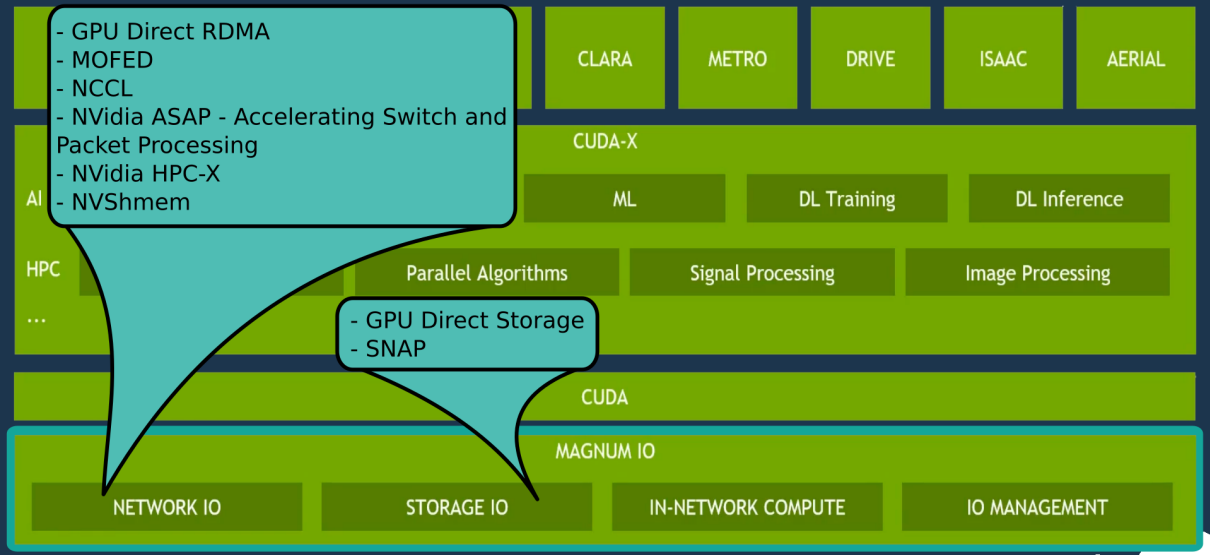

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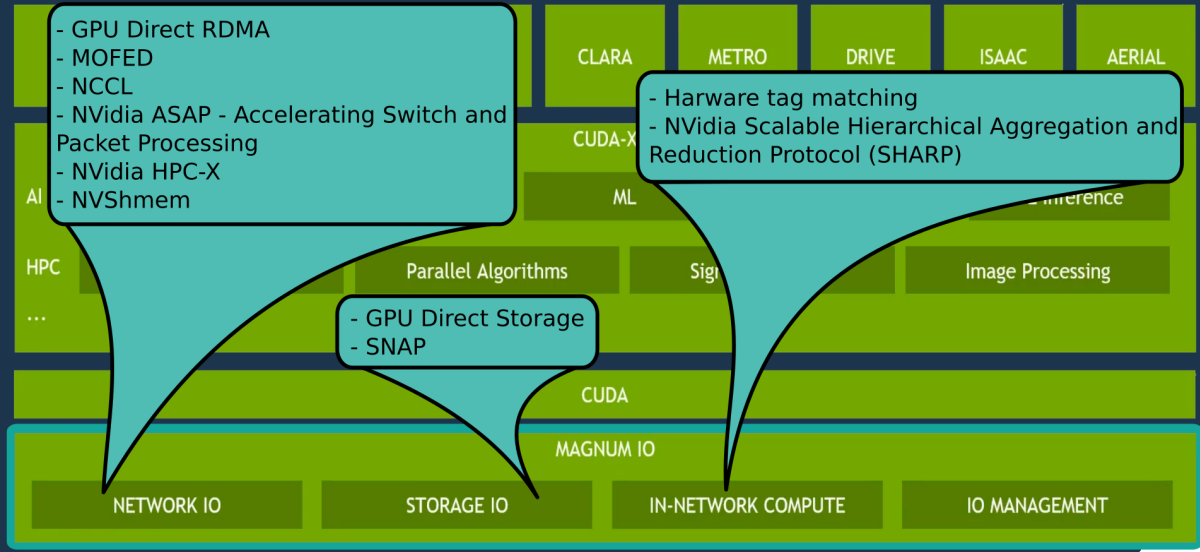

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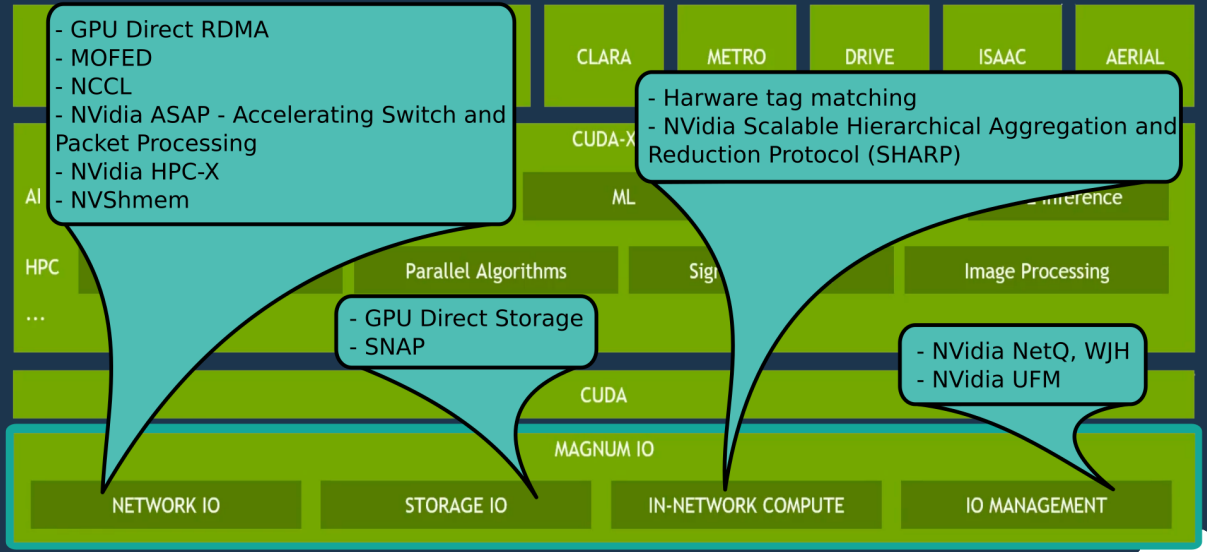

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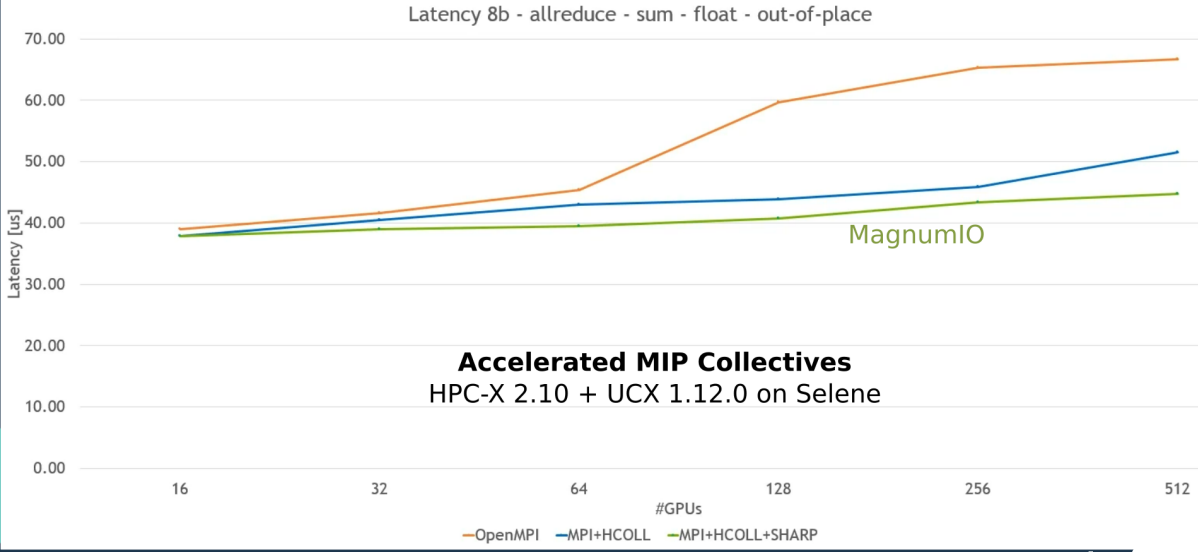

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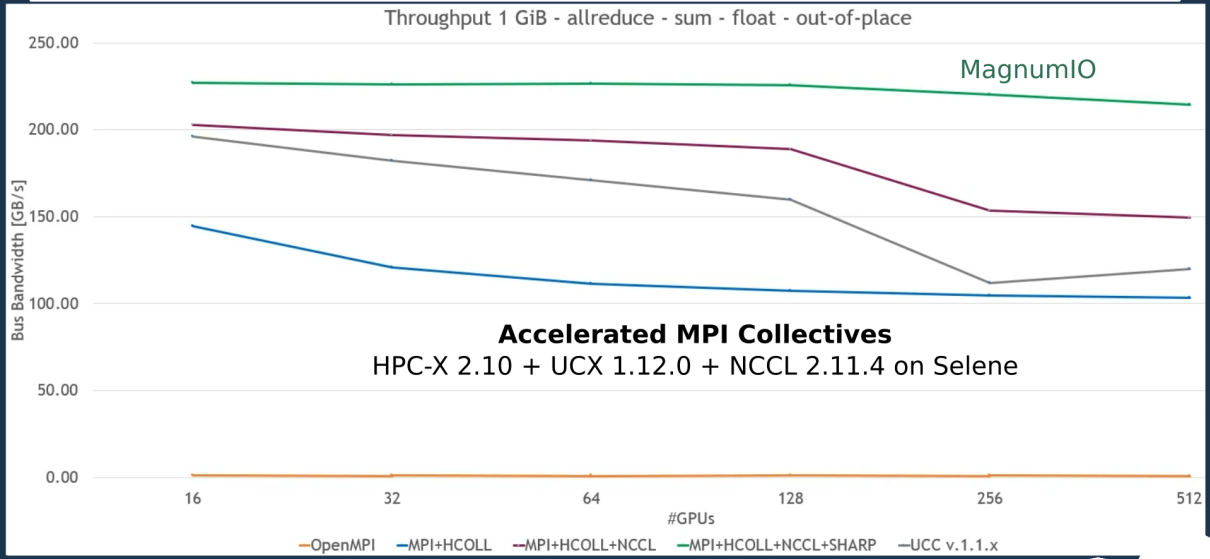

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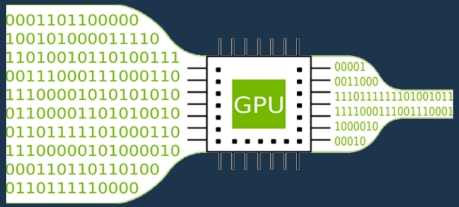
C/C++ standard calls



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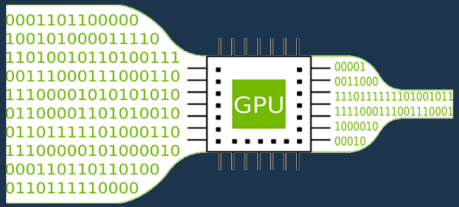

Release 2.2 :

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- High Level API simplified
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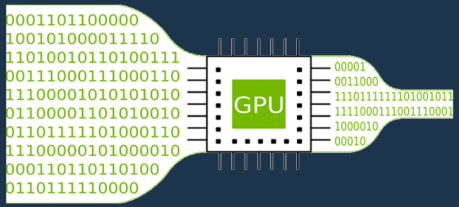

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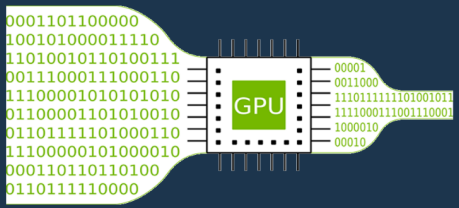

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News in future release 2.3 : 

- Add **Zstd** decompression
- Add **BitShuffle** (**float** compression)

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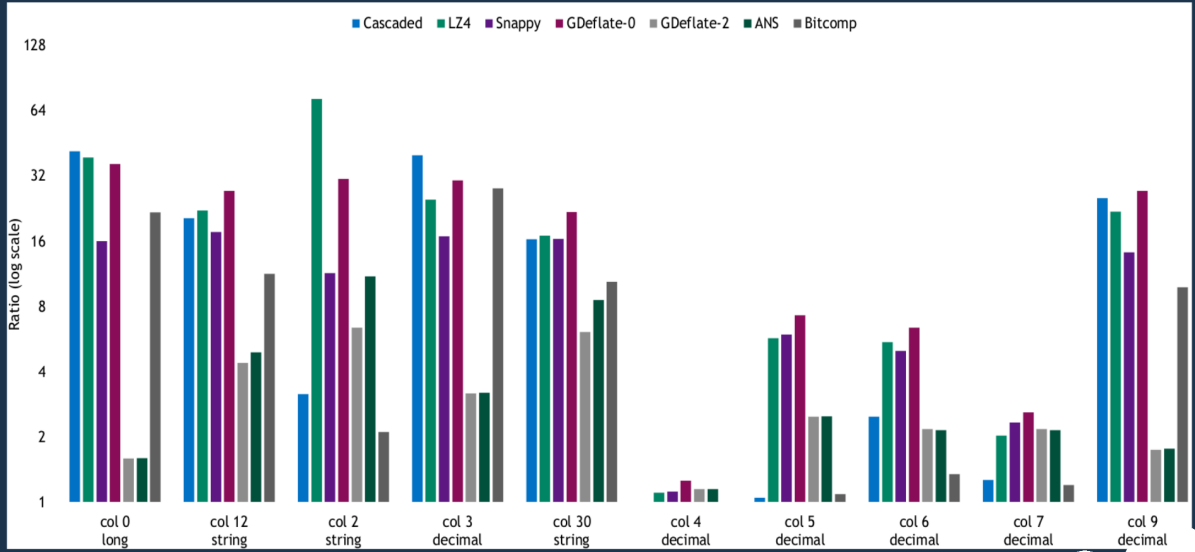

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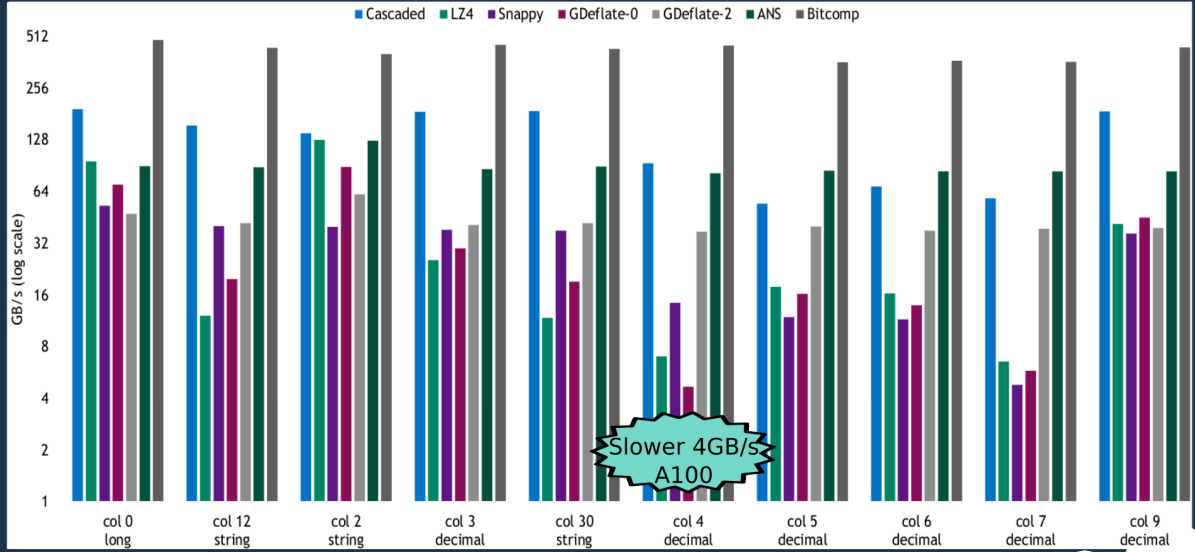

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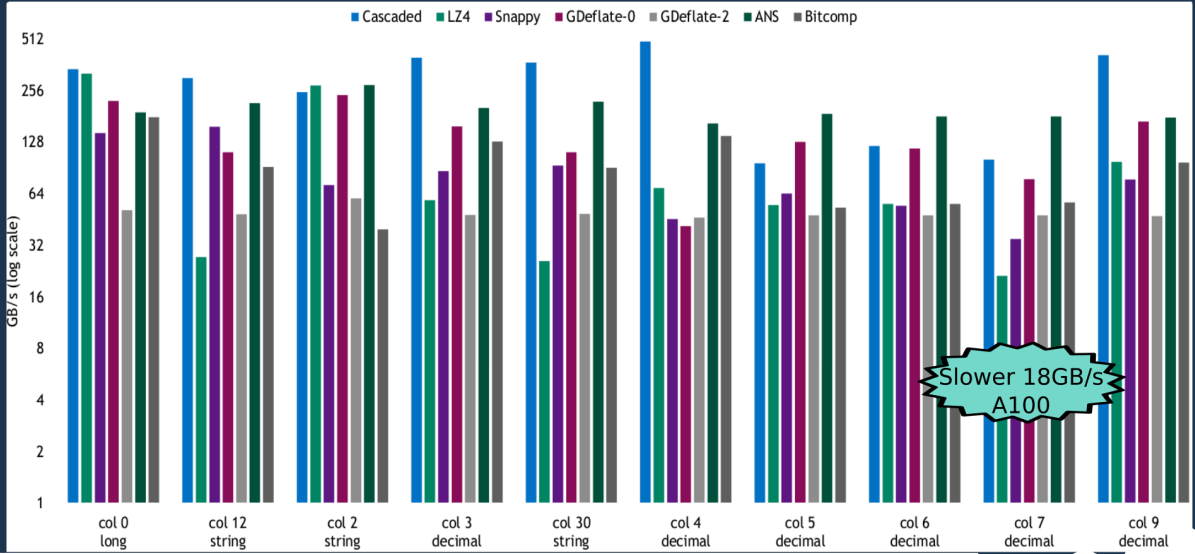

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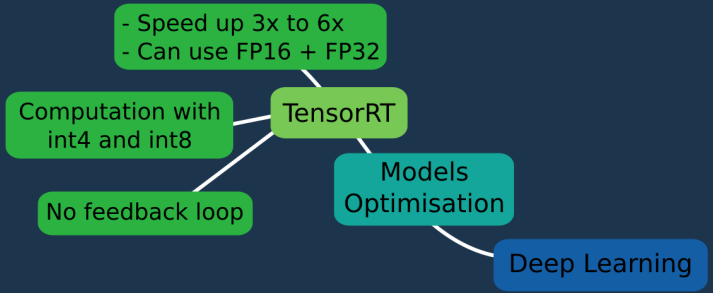

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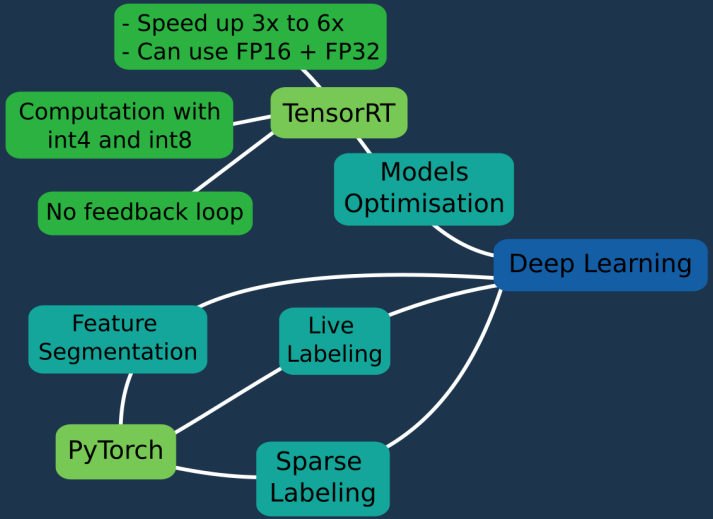

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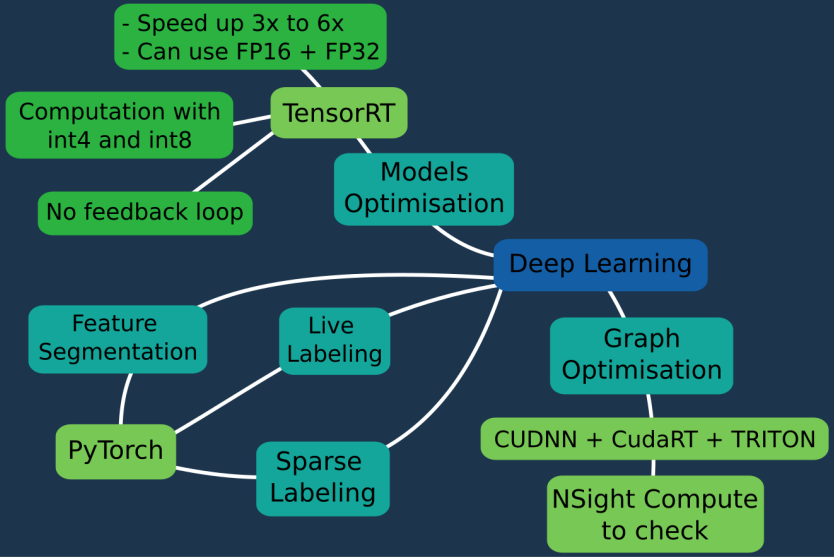

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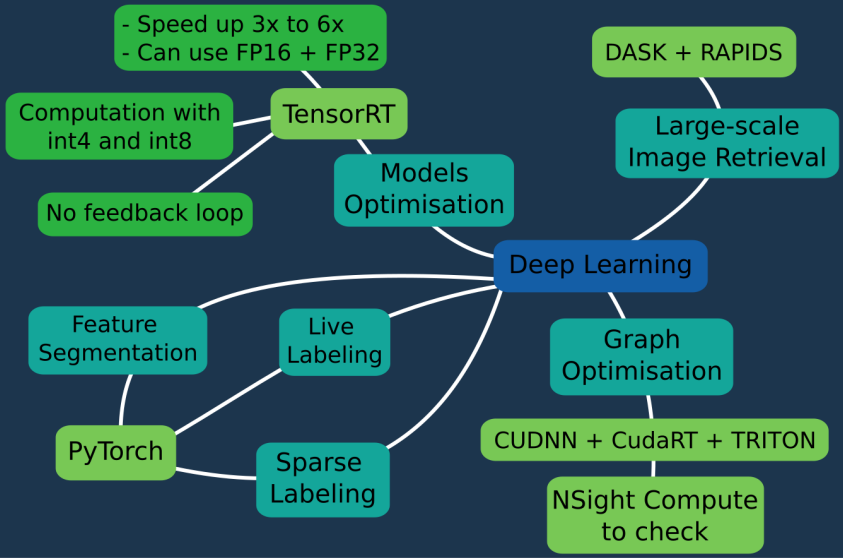

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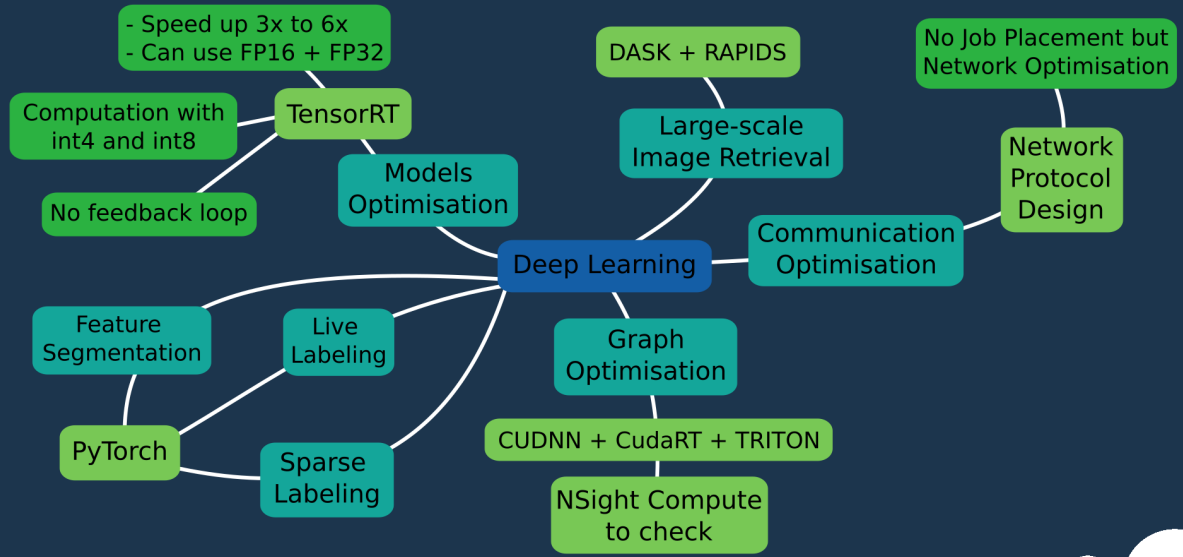

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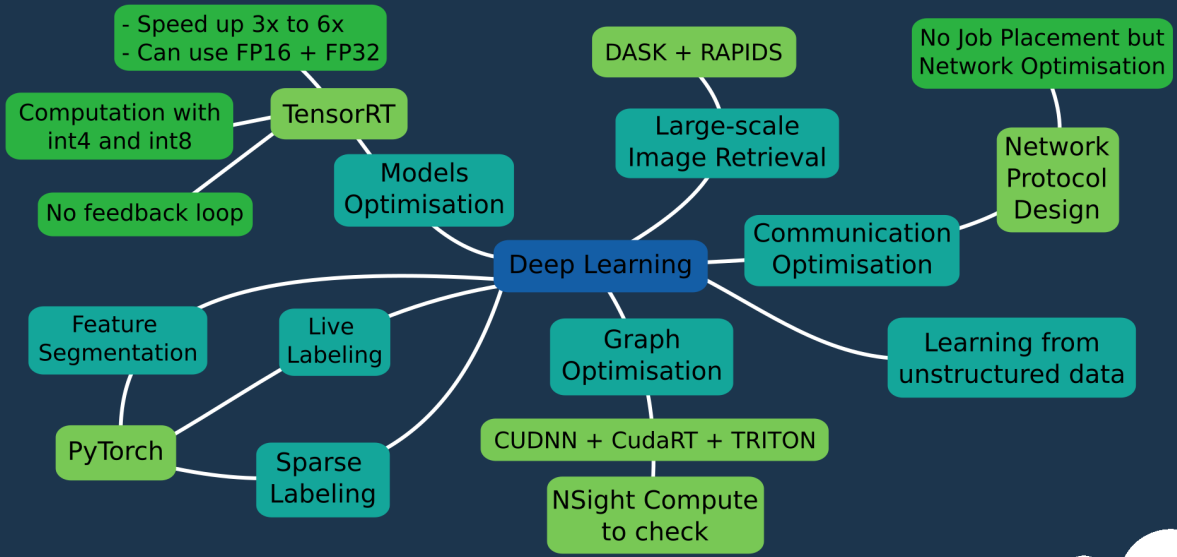

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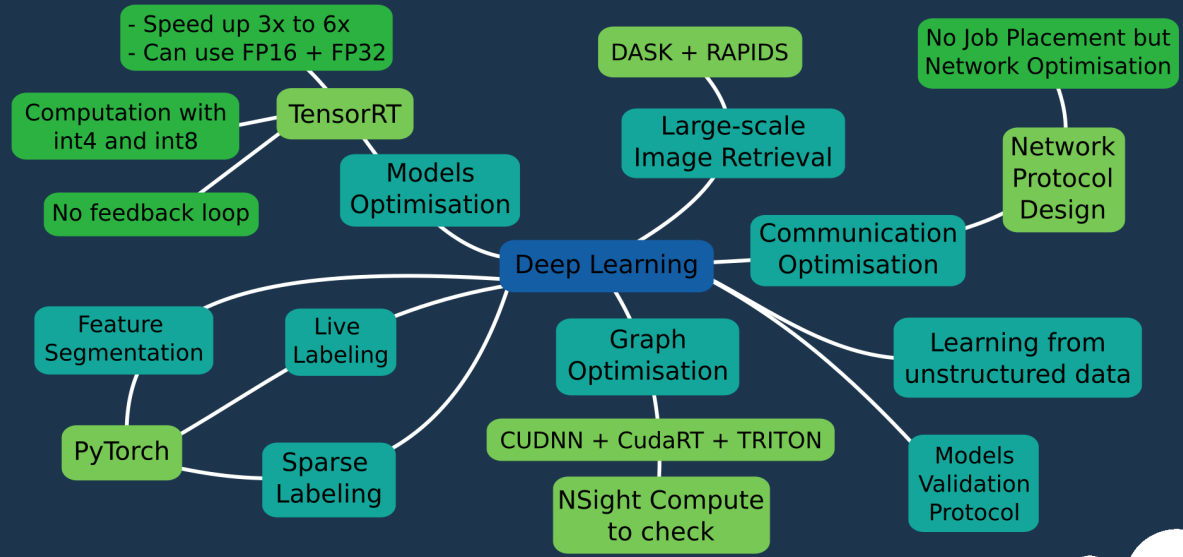

Link to a big summary

GTC 2022 notes from Reprises website

Sébastien Gignoux : l'architecture Fermat (see 11h-11h15 of first day)