Status CE65V2_xx chip

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CE65V2_xx (1.5mm x 1.5mm)

Versatile exploratory chip using matrix of pixels (48 col x 24 row) output is multiplexed to one analogue channel (matrix rolling shutter readout mode):

- ✓ share common pads structure, carrier and proxy boards
- ✓ 4 power domains: 3.3V analogue, 1.2 analogue, 3.3 digital, 1.2 digital
- ✓ 3.3 analog and 1.2 analog share same ground AVSS
- ✓ 3.3 digital and 1.2 digital share same ground DVSS
- ✓ one column reserved for precise charge collecting diode capacitance measurements

Power:

- digital (3.3V IO/1.2V CORE): DVDD33, DVDD12,DVSS
- analogue (3.3V): AVDD33, AVSS
- analogue (1.2V): AVDD12, AVSS

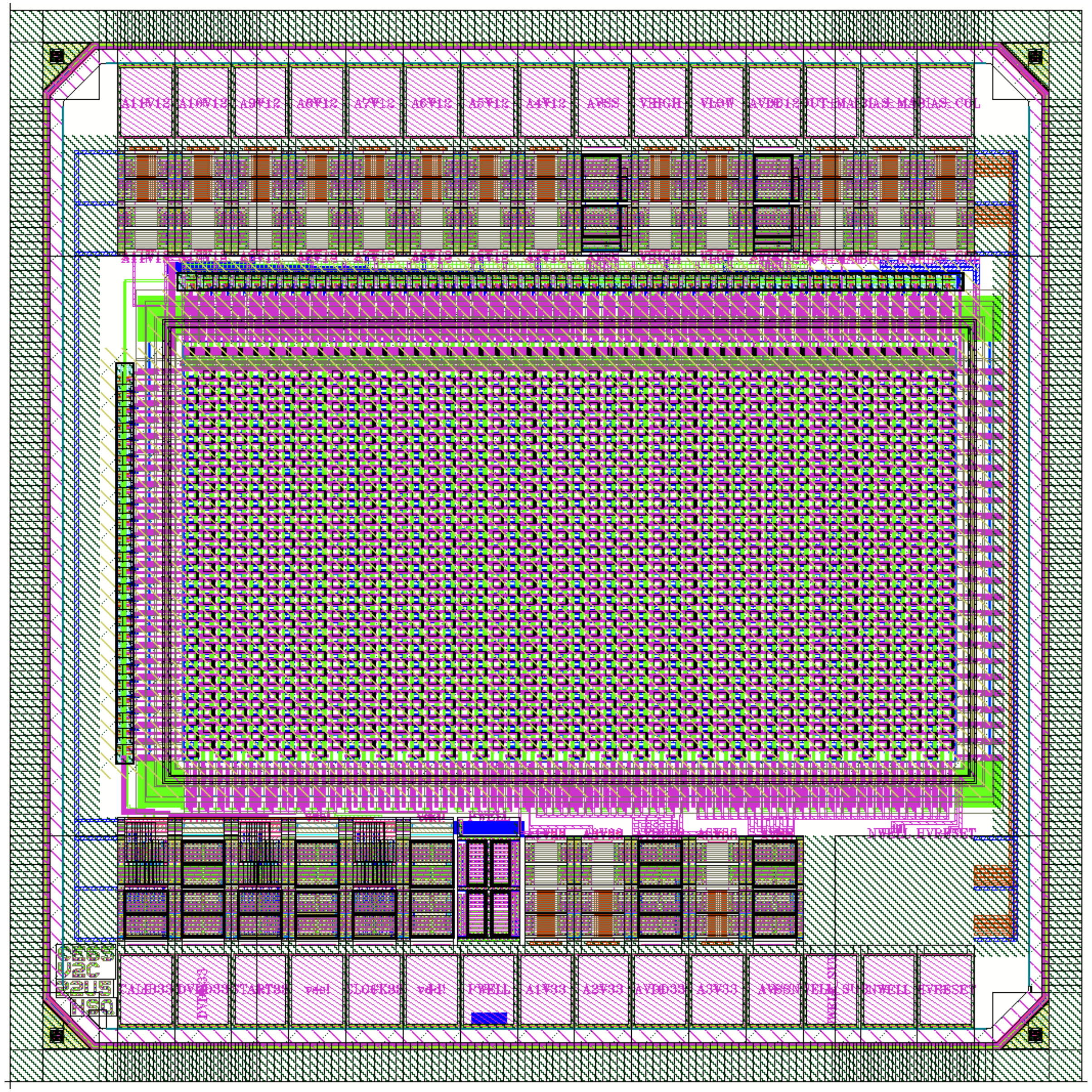
3 digital input pulses (3.3V): clock, start, calib

4 unprotected pads: HV, NWELL ,NWELLSUB, PWELL

Output is in 1.2V analogue domain
2 calibration voltages: VHIGH, VLOW
2 biases for output buffer

11 biases for pixel front-end:

- 8 X 1.2 analogue biases
- 3 x 3.3 analogue biases



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Different modifications / chips of CE65V2_xx / design status

Modification	Purpose	Pitch, um	Comment	N	status
CE65V2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (AC pixel from CE65 is implemented)	15, 18, 22.5, 18_{hexsq}, 22.5_{hexsq}	For lab and beam test, charge collection node, techno, optimization	5	DRC, LVS are OK for all chips Need finalize filling and define splits (3?)
CE65V2_A_xx	Precise measurements of multiplexed analogue or digital output of pixel FE ("_A_"): pulse duration, gain, FPN, noise, RTS..	18 (or 22.5)	For lab only, possibility to explore waveform with oscilloscope: FE optimization/tuning.	1 (existing FE from MOSS) + versions?..	If that chips is relevant for tests and not redundant to other chips: need to define which FE (or versions) for precise measurements