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Analog design in deep submicron technologies: Is it that bad?

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Even though deep-submicron technologies have been around since a couple of decades now, research groups have preferred to keep working with more mature technologies due to various reasons: performance, reliability, price, internal IP availability, etc. Unfortunately, the market pushes foundries to shut older nodes manufacturing down, forcing research groups to switch to newer nodes. Such change may look intimidating due to the huge differences in performance: supply voltages approach sub-1 V, transistors tend to behave differently, design tools may have changed, layout design turn even more demanding, etc. In this presentation, we first review the main differences in transistors performance in deep-submicron technologies. Then, we take a look at the different design strategies that have been proposed for novel technology nodes, both for transistor sizing and circuit design for lower supply voltages. Layout characteristics and design in deep-submicron technologies have also suffered several changes that are sometimes underrepresented in the literature. For this reason, we will also review the considerations to take into account while layouting our circuits in such novel technologies.

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