Time Synchronization Schemes for the Hyper-Kamiokande experiment

Context

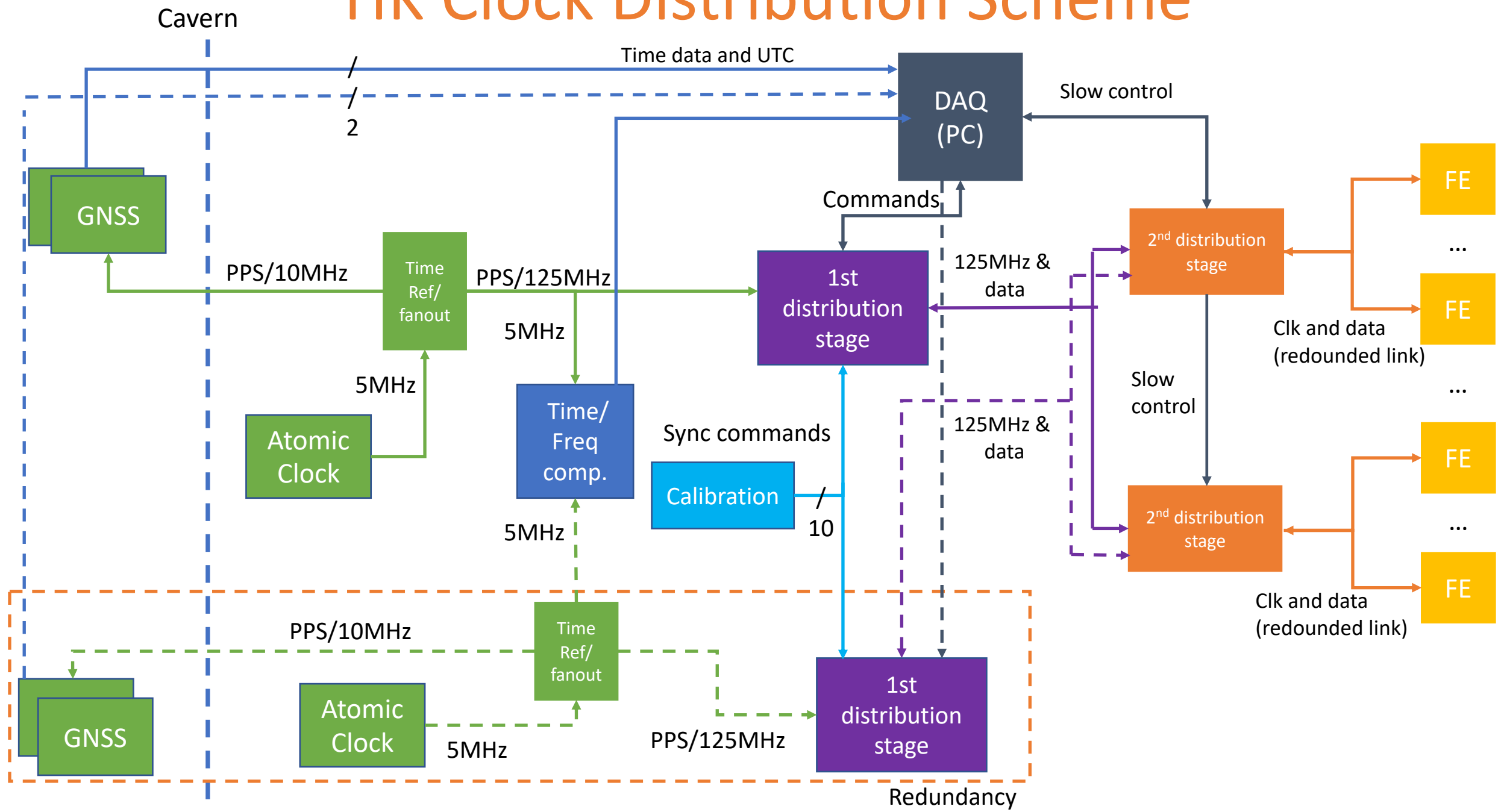
LPNHE, CEA and INFN have joint forces to design a full time distribution scheme that will be submitted to the international collaboration this spring. If approved the group will be in charge of the construction and commissioning. Together with the LLR digitizer it will give IN2P3 a central role in HK!

The proposal envisions to provide a system that fulfil the needs of both HK far and intermediate detector. Possible synergies can be found with the future T2K upgrades (when integrated in HK).

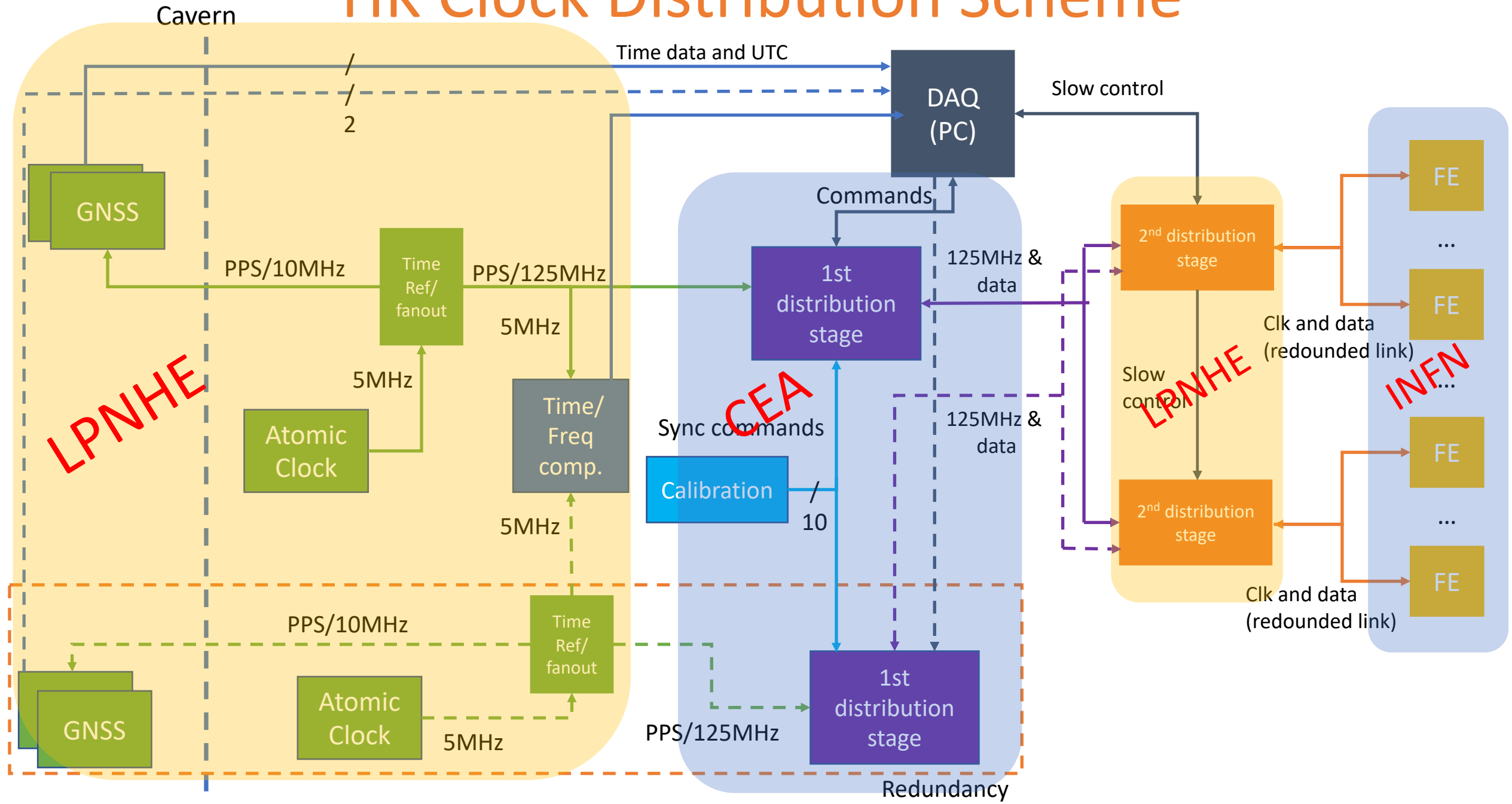
To conceive this proposal, an intense and fruitful R&D campaign is being carried out. Its results will be available for other IN2P3 experiments. This group believes that the time distribution system is a strategic assets for future experiments due to the constant size increase of particle detectors.

This program has already created synergies across CNRS institutes thanks to a very fruitful collaboration with the SYRTE lab (Observatorie de Paris).

HK Clock Distribution Scheme



HK Clock Distribution Scheme



Clock Generation & UTC - Connections

- The local time is generated (by a precise atomic clock) in the form of 5MHz in synch to each other (HK local time).
- The time reference point custom board receives the frequency, generate a local PPS and distribute them to the GNSSs and the first distribution stage. It has extra ports to compare the main and spare base cadence.
- GNSSs use the input cadence to sync the outputs and have a reference frequency more stable than the internal oscillator

Clock Generation & UTC - Connections

- 2 GNSSs receivers (connected to the same antenna) get information from the satellites and measure the time distance between the local PPS and UTC.
- The result of this measure is sent to DAQ and used to transform the local tag to UTC
- The DAQ monitors the status of the GNSSs and select which one to use

Clock Generation & UTC - Redundancy

- The full chain (atomic clock, GNSSs (x2), and first distribution stage) is replicated for redundancy
- Having a total of 4 GNSS receivers will allow the DAQ to identify if one is malfunctioning
- The time distance between the 2 chains will be constantly measured and the result sent to DAQ. This info will be used in case of switch from one chain to the other

Clock Generation & UTC - Reliability

- Scheduled interventions on components will be performed to reduce the risk of failures
- In case of PHM, the atomic clock “physics package” will be replaced within 10 years (at productor’s site in CH). In case of rubidium the clock will be changed.
- A third atomic clock will be available at far detector site and periodically turned on. It will serve as cold spare used if the main or the hot spare needs maintenance
- All the atomic clocks will be measured against the so-called travelling station every 3 / 4 years.
- The GNSS receivers will be changed before the end of life.
- The maintenance cost needs to be included in the budget request

Time Base and UTC Characterization

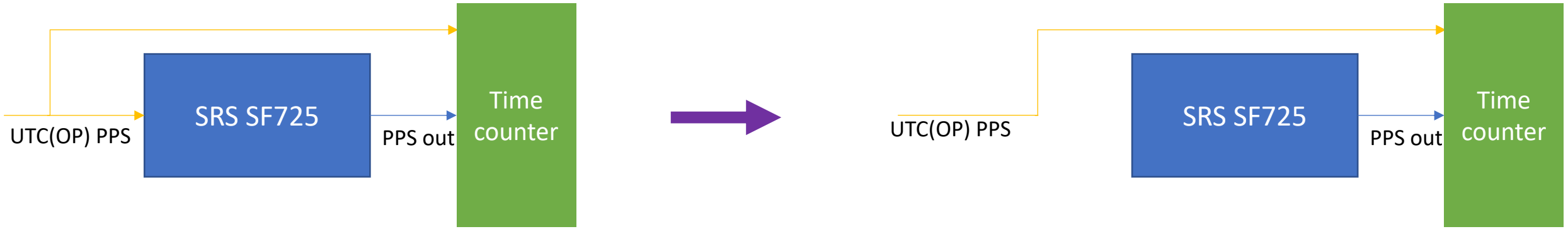
All the main chain components have been purchased and an extensive test campaign has been performed (many thanks to SYRTE!!)

- Atomic clock: rubidium SRS SF725 and passive hydrogen maser T4 science PHMaser 1008 (to be delivered in March).
- GNSS: Septentrio PolaRx5 and multi-constellation antenna
- Time comparator: Keysight 53230A

SRS FS 725 Rubidium Clock Characterization Setup

The rubidium clock was tested against the French definition of UTC: UTC(OP) using a time interval error measurement instrument.

After a warmup period of few hours the clock was synchronized with the UTC(OP) via the PPS input port. The UTC(OP) PPS was used as SF725 input until the PPS in and out were aligned then the atomic clock was configured in free running mode

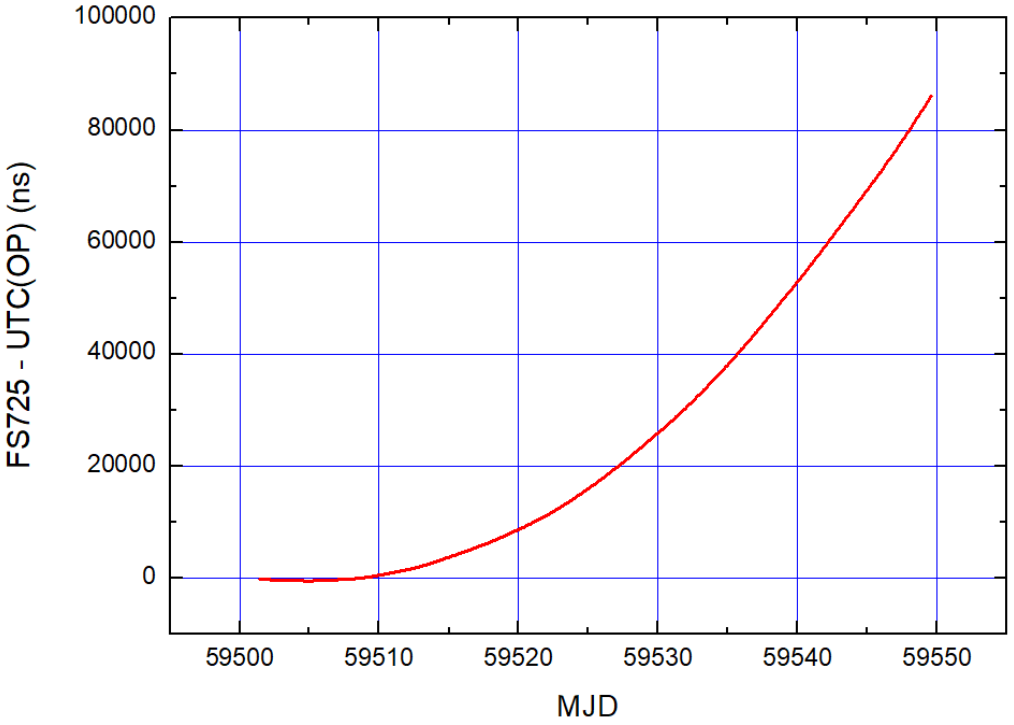


Steered mode

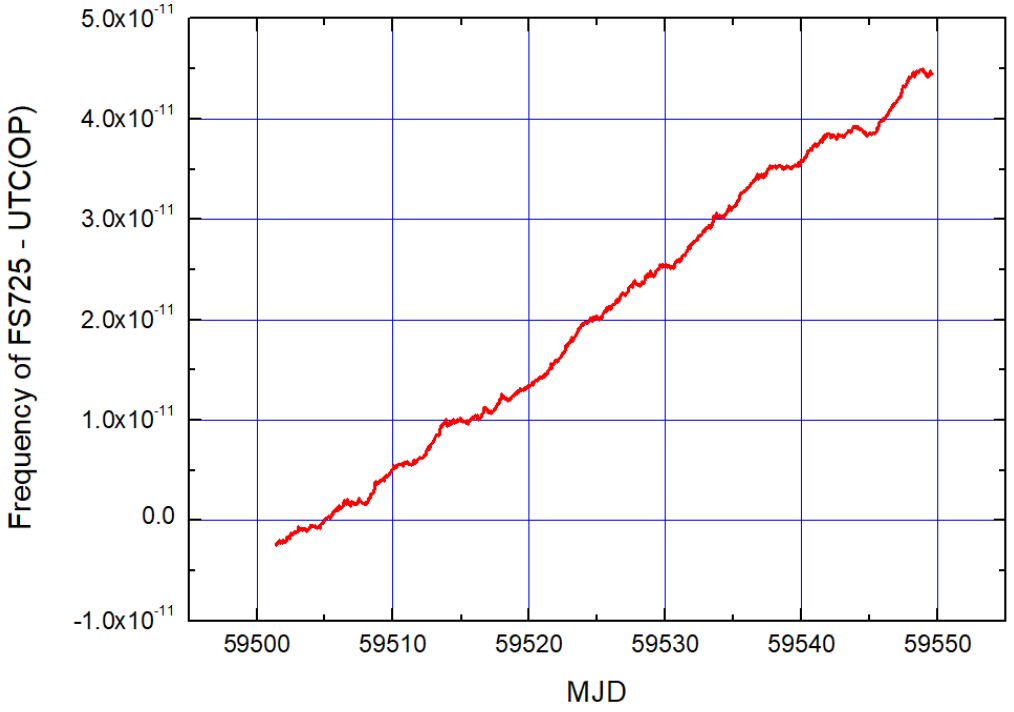
Free-running mode

SRS FS 725 Rubidium Clock Drift Measure

In free running mode the clock shows a constant frequency drift of 10^{-12}/day that reached a total of 4.5^{-11} after 50 day of test.



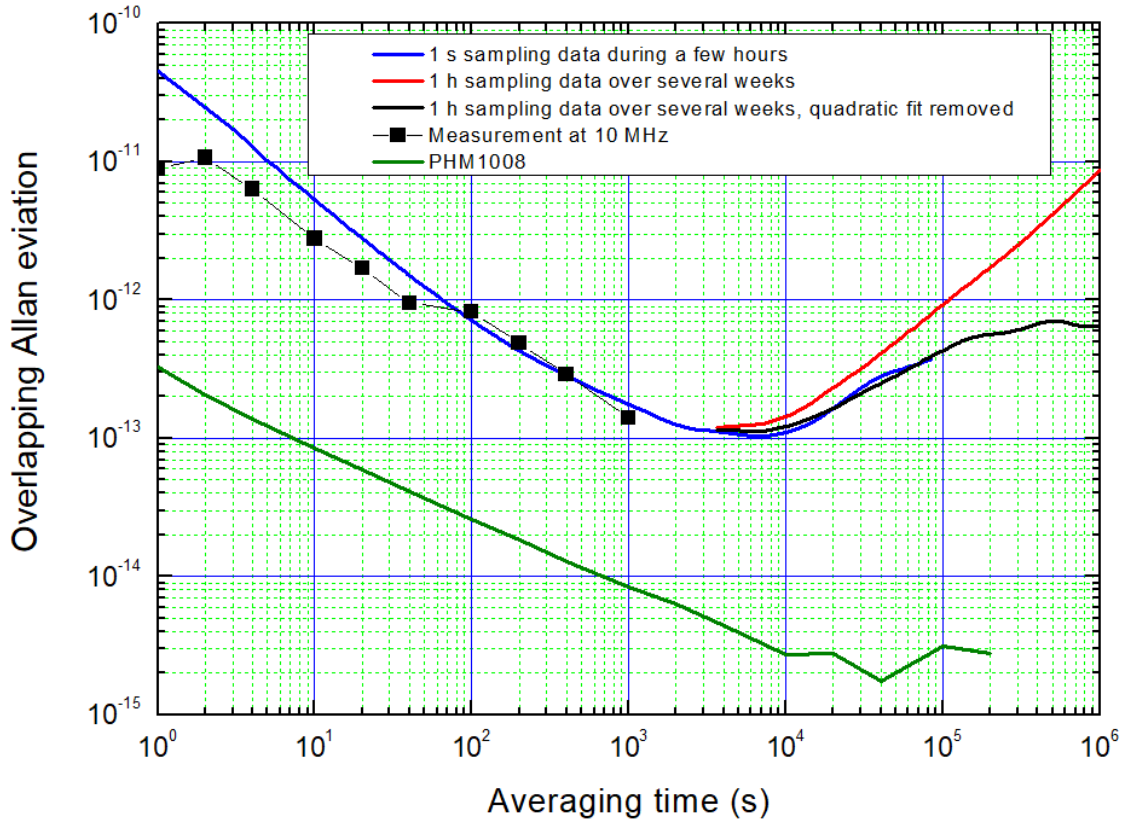
Phase comparison



Frequency comparison

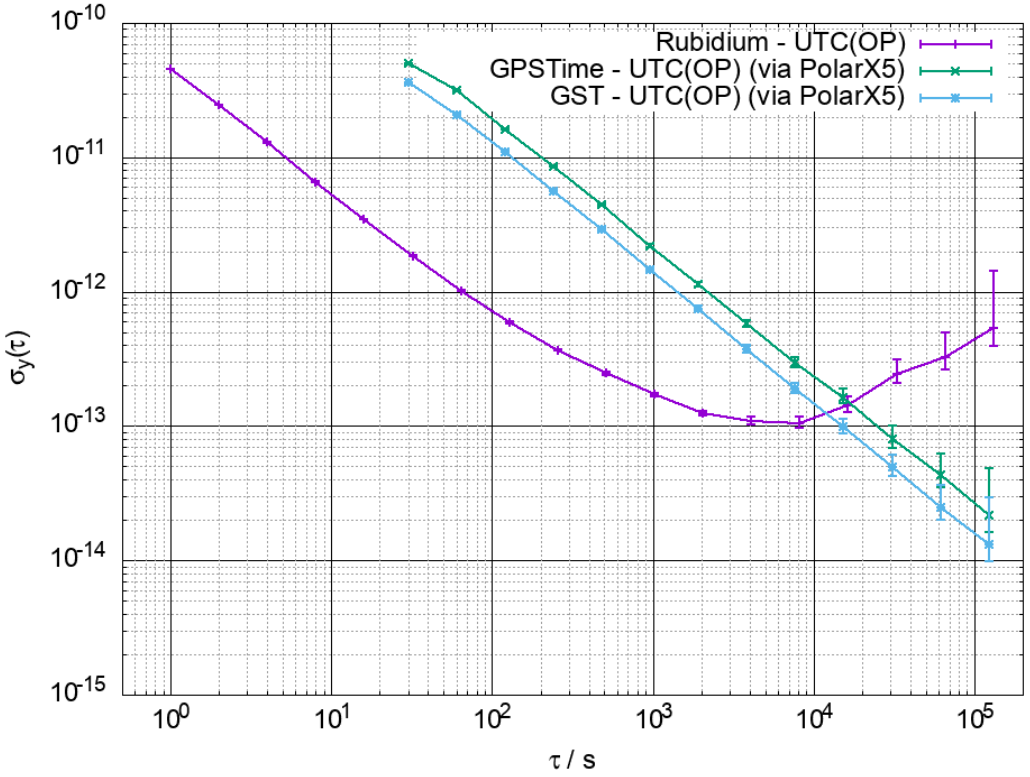
SRS FS 725 Rubidium Clock Stability Analysis

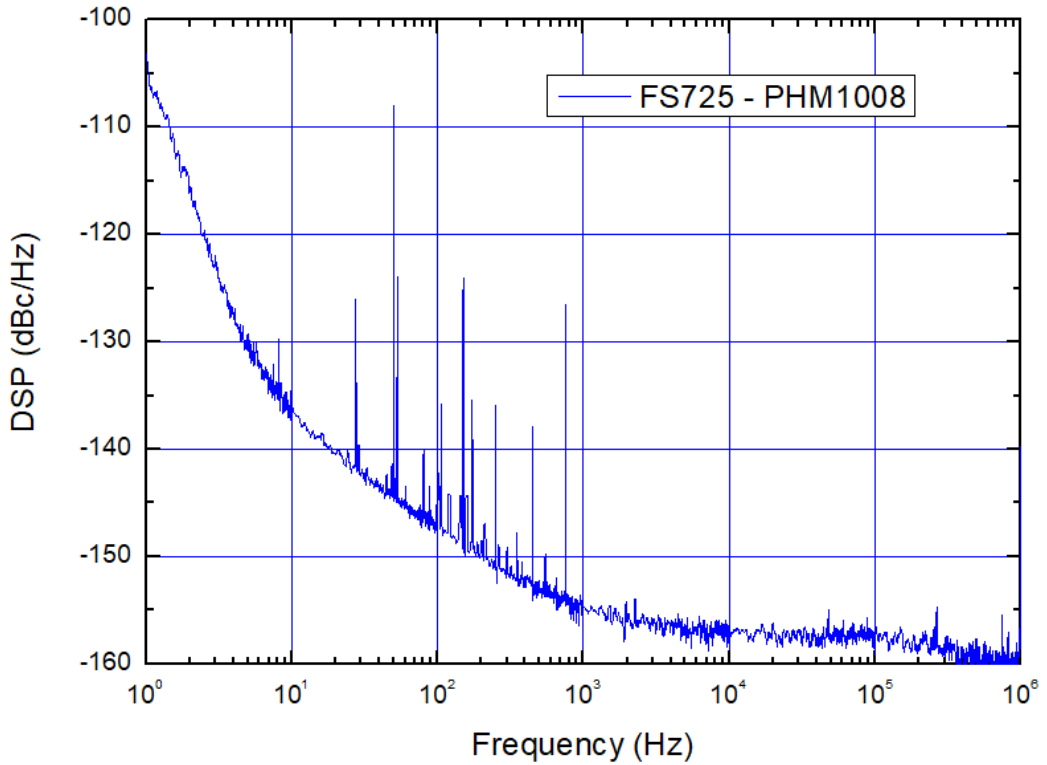
The clock short term stability was measured on intervals of 1 s during few hours. It averaged at $4 \times 10^{-11}\ \tau^{-1}$ and went down to 10^{-13} (white noise) before the drift become evident after 1000 s. The results are compared with a PHM clock



SRS FS 725 Rubidium Clock Stability Analysis and Jitter

The drift comparison against the UTC(OP) gives an idea of the drift correction frequency. The green and blue lines on the plot are the UTC representation of GPS and Galileo via GNSS receiver. The phase noise of the rubidium is also reported





Septentrio PolaRx5TR calibration

Our receiver (RINEX name: LPN1) was calibrated against one at Observatoire de Paris (OP73) in turn calibrated against a travelling station from Bureau International de Poids et de Mesures (BIPM, responsible of defining UTC). OP73 is then a so-called level 1 receiver and LPN1 has been calibrated as a level 2.

The receiver internal delays were measured for both GPS and Galileo constellations.

The combined uncertainty of the LPN1 station hardware delays calibration is 4 ns. This is the conventional uncertainty applied after a “direct calibration” in the TAI system.

Septentrio PolaRx5TR calibration

The two tables correspond to GPS (P1 and P2 codes) and Galileo (E1 and E2a) codes.

Receiver	Reference	MJD of Measurement	REFDLY	CABDLY	P1 DLY	TDEV	P2 DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	29.500	NC	26.300	NC
LPN1	OP73	59508 – 59514	88.3	127.1	25.832	0.024	22.871	0.022

Receiver	Reference	MJD of Measurement	REFDLY	CABDLY	E1 DLY	TDEV	E5a DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	31.700	NC	31.300	NC
LPN1	OP73	59508 – 59514	88.3	127.1	28.242	0.040	25.431	0.034

The values will be configured in the receiver and a correction will be applied to the UTC time. Mixing the two constellations' data will be done to provide the UTC time.

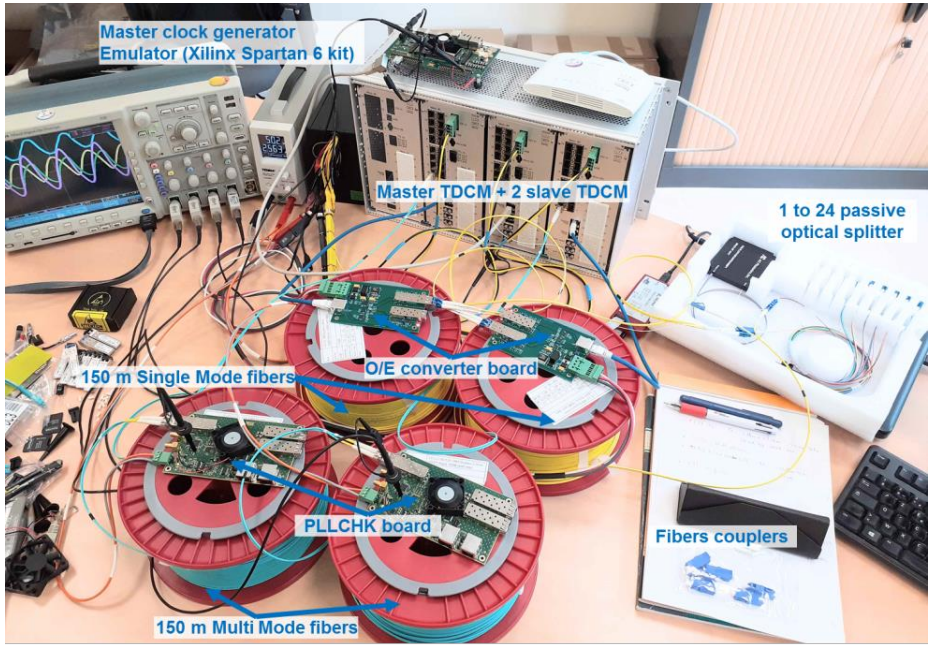
First distribution stage

- The system has two parts:
  - The time reference/fanout board transforms the base clock to FE ref clock and provides cadences for all the elements
  - The first distribution stage broadcast the clock and sync command to the second stage.

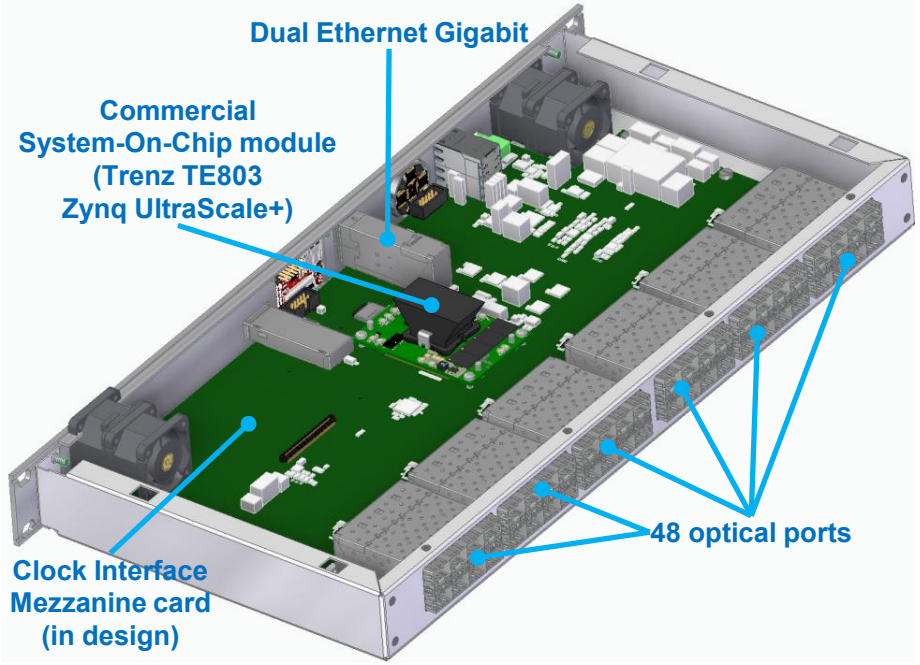
- The system will be replicated two times for redundancy

- The CEA group has designed a first prototype which is on fab now. The tests should start this week.

R&D ACTIVITIES AT IRFU ON CLOCK DISTRIBUTION FOR HYPER KAMIOKANDE



Setup for the evaluation of concepts



48-port clock distributor prototype

R&D activities

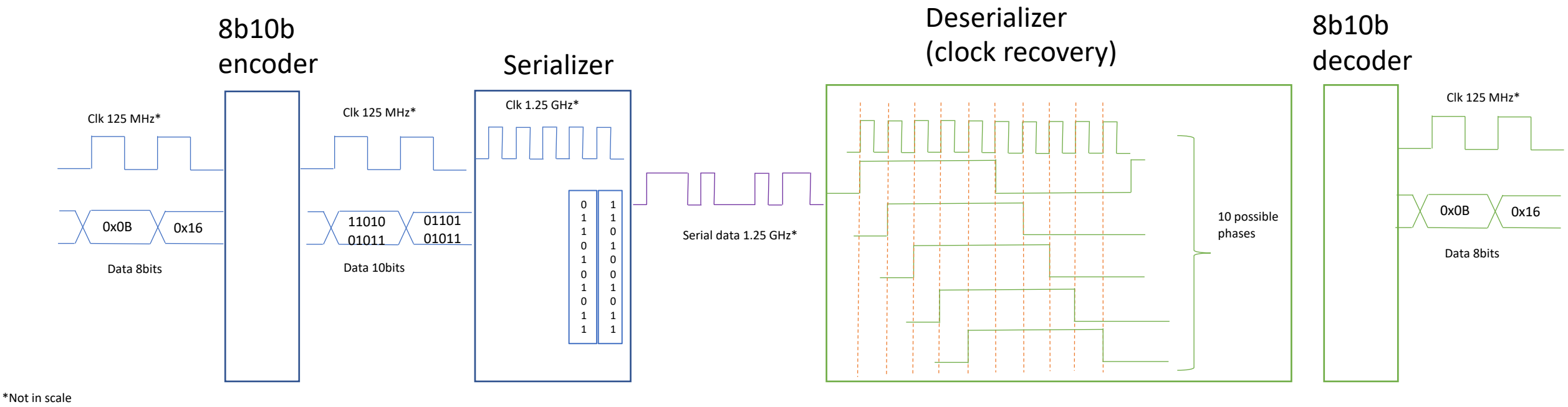
- Evaluation of components (e.g. passive optical splitters, commercial PLL) and techniques (e.g. clock modulation) for clock distribution. Based on hardware from T2K upgrade and other elements
- Design of a 48-port clock distributor aiming at HK specifications. Imminent delivery of first prototype

→ Collaboration Lpnhe / INFN / Irfu on proposal of clock distribution system for HK.
Work sharing: Clock Generation & 2nd Stage Clock Distribution (Lpnhe),
1st Stage Clock Distribution (Irfu), Front-end Clock Receiver (INFN)

Second Distribution Stage

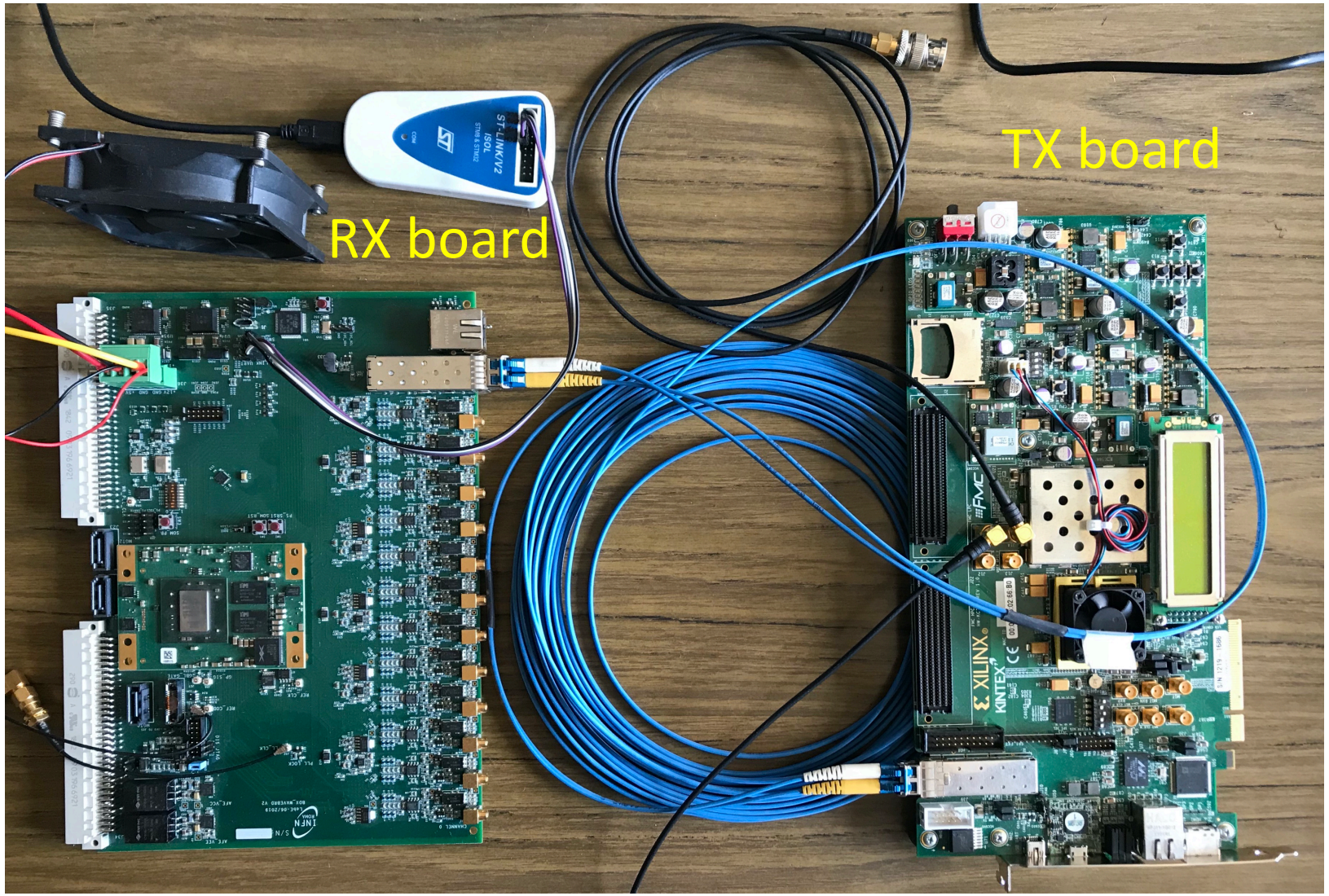
Clock embedded into data

The link from the second distribution stage is based on the clock and data revery concept. The clock, time information and payload data are sent on the same fiber encapsulated in a protocol



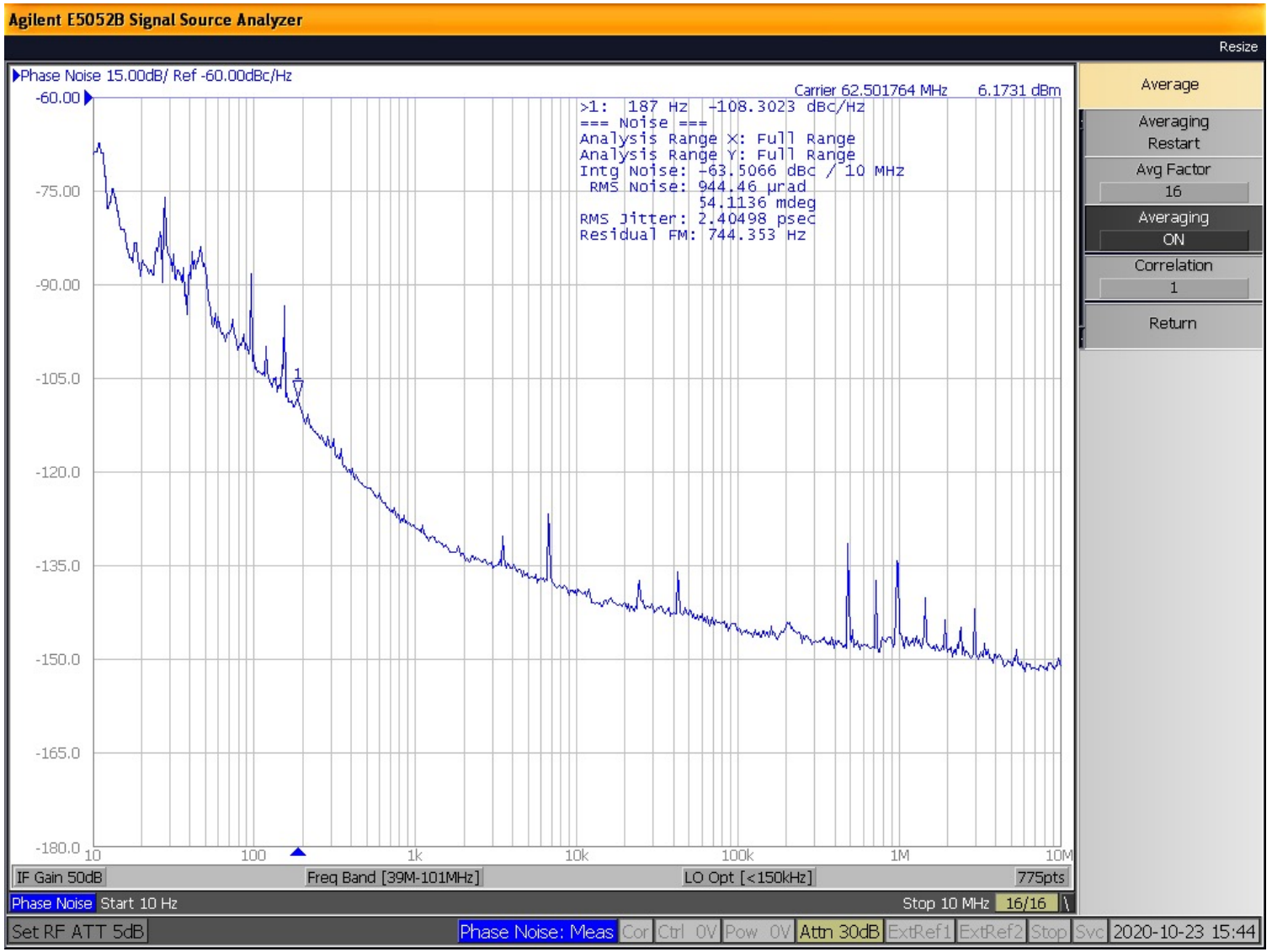
When the link's lock is established, the reconstructed clock is generated in phase with the master clock.

Jitter Test



The Clock and data recovery concept has been tested on existing boards. The results are well within the experiment’s requirements

RX clock Time Interval Error (jitter)



The received clock is sent to the jitter cleaner PLL SI5345 and its output is measured

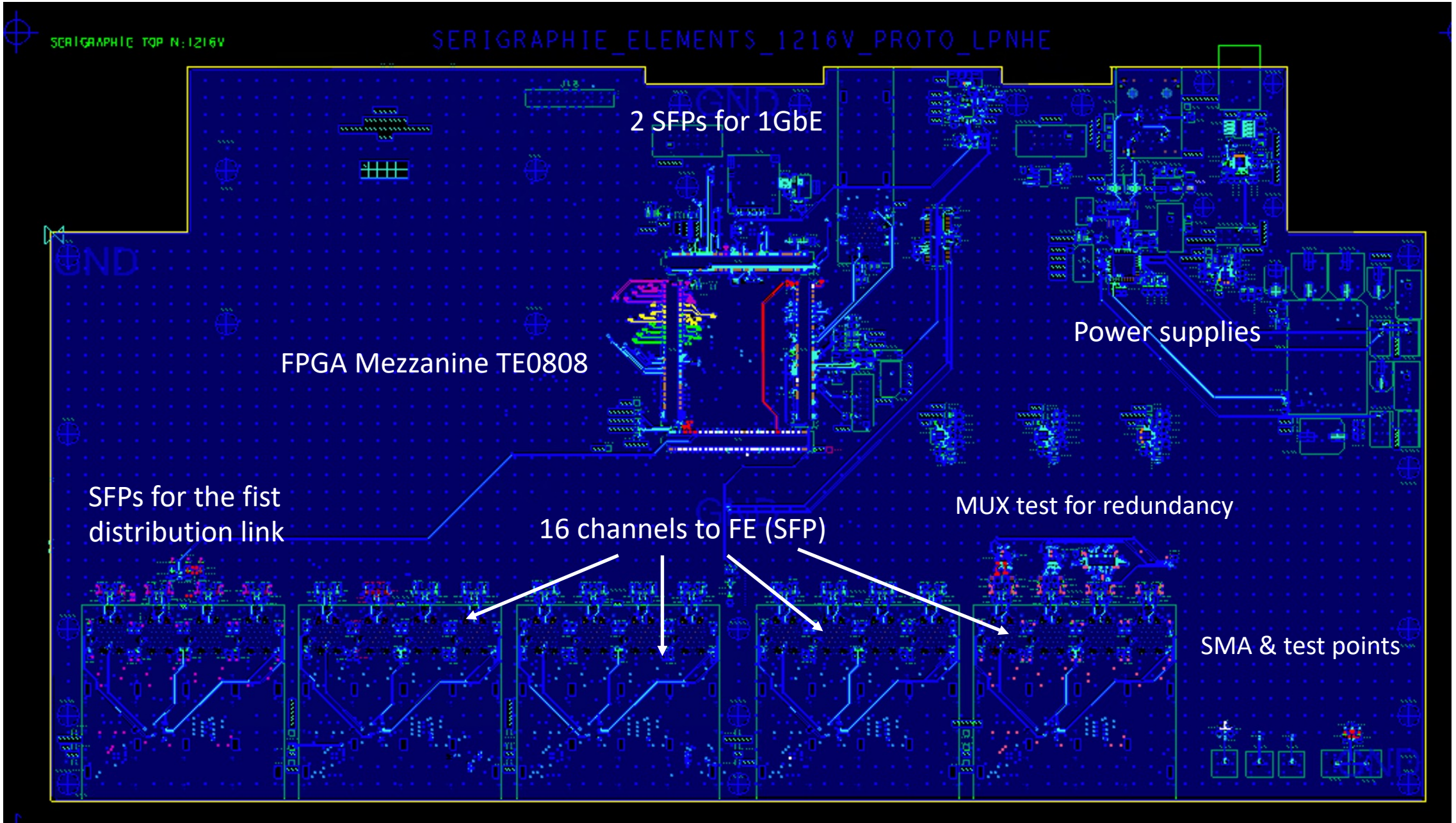
RMS noise 2.4 ps

The experiment's requirment is 100 ps

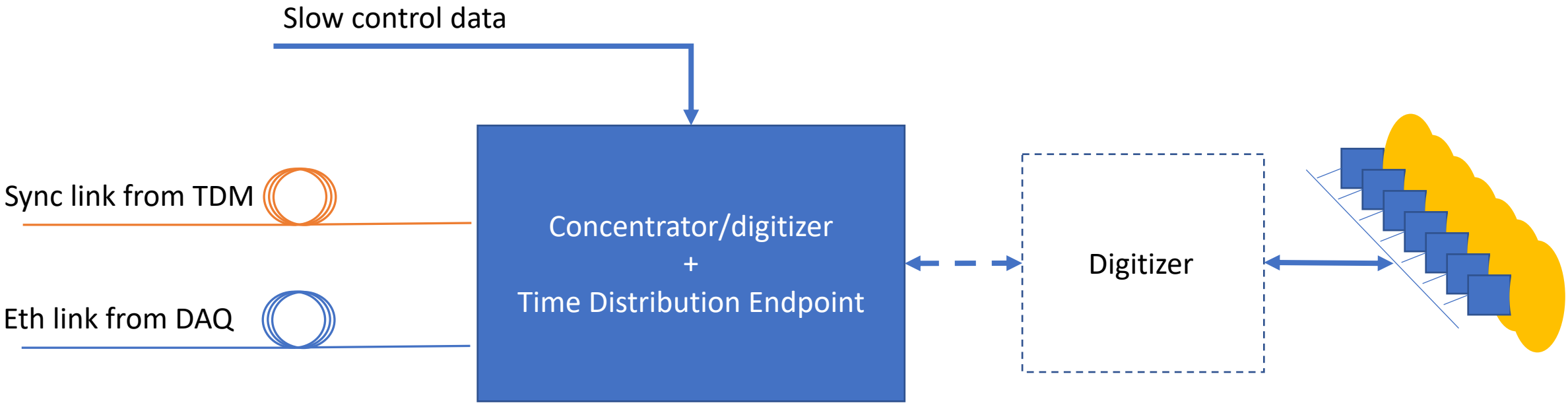
Second distribution stage

- The board design has been derived from the first stage distributor. Same design with same modifications (few weeks of work). Good synergy!
- An Ethernet DAQ link is used for the non-sync commands.
- Link redundancy on the board (2 optical transceivers).
- Synchronous and deterministic link on both directions.
- The board is in fab right now.
- Firmware development has started on EVB very similar to the final design.

Second Stage Distributor



Time distribution Endpoint (TDE)



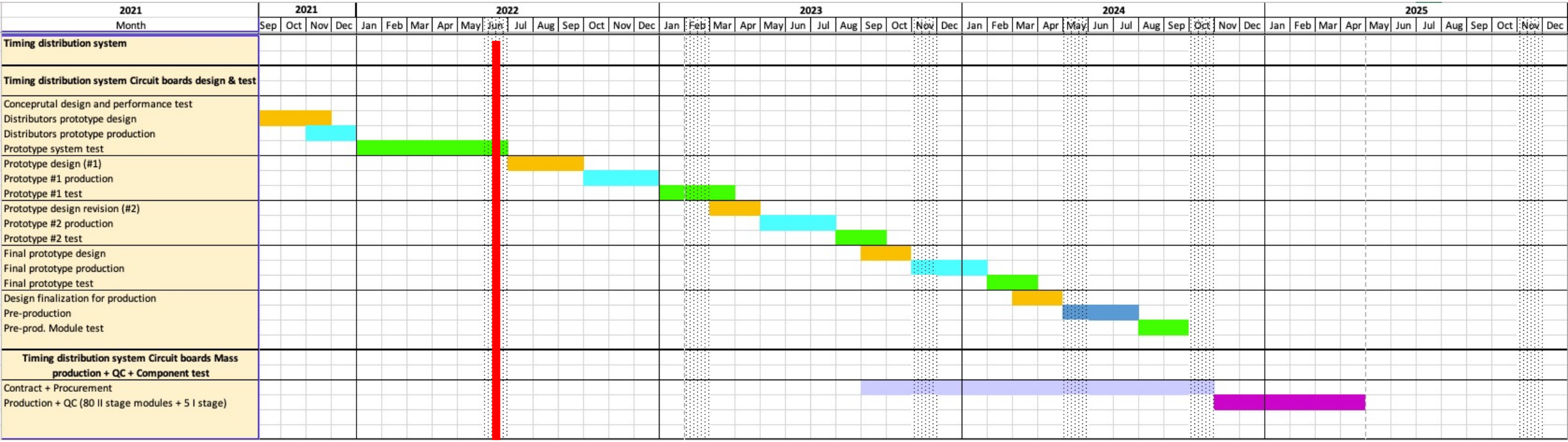
The time distribution endpoint is embedded in the concentrator board inside the FE. Our group provides know-how, firmware IPs, SFPs lasers and PLL and give full support for this integration.

We look forward to start testing our system with the HKROC board prototype.

Short Term Schedule

Task	% complete	Nov-21				Dec-21				Jan-22				Feb-22				Mar-22				Apr-22			
		w1	w2	w3	w4	w1	w2	w3	w4	w1	w2	w3	w4	w1	w2	w3	w4	w1	w2	w3	w4	w1	w2	w3	w4
Specification Document	99%																								
Time Base Generation																									
Hardware	100%																								
Standalone Hardware Test	90%																								
First Stage Time Distribution																									
Hardware Main board design/procurement	100%																								
Hardware Main fab	100%																								
Hardware mezzanine design	100%																								
Hardware mezzanine fab	80%																								
Firwmare design	10%																								
Standalone Test	0%																								
Second Stage Distribution																									
Hardware design	100%																								
Hardware procurement/fab	20%																								
Firmware design	70%																								
Test	70%																								
Time Distribution Endpoint																									
Hardware components procurement	100%																								
Firmware IP	90%																								
Test	90%																								

Long Term Schedule



R&D review and technologies selection

Summary

- A great synergy and collaboration has been established with CEA, INFN and SYRTE (not part of the project)
- The full time distribution scheme has been designed.
- Test and characterization campaigns on different subsystems have been carried out.
- First prototypes have been designed and are fabricated now.
- The technical note (including precise cost estimation) for the final review is being prepared
- We believe that the acquired know-how could represent a strategic asset for the IN2P3.

We look forward to share our material with the IN2P3 management to prepare the financial proposal for the final commitment

Cost Estimation

	total number of PMTs	PMT per FE	Total number of FE (Time distribution nodes)	Number of nodes per distributor	Number of distributors	Distributor cost per unit	Total istributor's cost
outer detector	13 300	72	185	16	12	4 000	48 000
Inner detector	20 000	24	833	16	53	4 000	212 000
MultiPMT	2 000	12	167	16	11	4 000	44 000
		total FE	1 185		76		
Total distributor's cost	304 000						
Atomic Clock cost	5 000				First Distribution Stage		
Number of AC	3				distribution Board cost	5 000	
GNSS recevier	13 000		quote septentrio		Number of Boards	4	
Antenna + cable	4 000		quote septentrio		Fanout board	2000	
Number of GNSS	4				Number of Boards	€2,00	
Number of antennas	2				Total First stage cost	€24 000,00	
Total clk ref cost	75 000						
White rabbit switches	5 000						
Grand total clock rference	80 000				Time Distribution EP		
Slow Control switch	2 000				SFP cost	20	
					Number of SFPs	2	
Total cost	386 000				PLL cost	15	
Contigency	20%				Number of PLLs	1	
					WR circuit cost	0	
Total Gen&second stage	463 200						
					Total costvper FE	55	
Total all included	€528 361,72				Grand Total cost	€65 159,72	