Gateware: serial link and heater Specification

- Serial links
  - Requirements
  - Conceptual view
- Heater
  - Definition

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Serial links : requirements

Goal : Test serial links for debug and qualification of PCIe400

PCIe400 has

- 48 bidir links for front-end : up to 25 Gbits/s
- 2 bidir links for TFC : up to 10 Gbits/s
- Benefit from links symmetry to test on loopbacks (internal/external)

Verification at different steps of development maturity

- Debug : recognize a fixed pattern
- Functional : measure a bit error rate (BER)
- Qualify : measure BER + eye diagram
- Acceptance : measure a BER with high logic occupancy

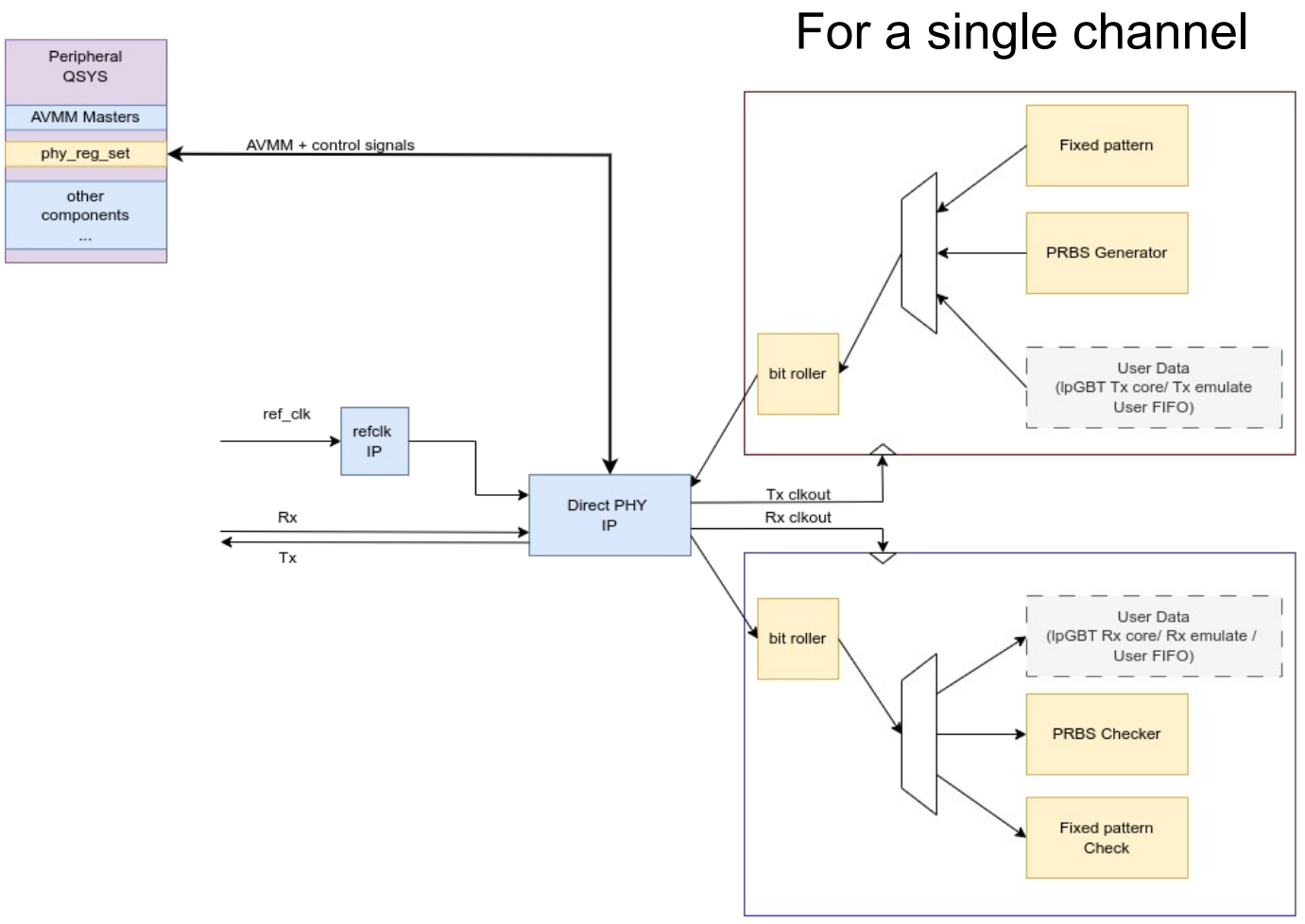
Design should be configurable

- Active channels
- Datarates (10 or 25Gbits/s)
- FPGA logic occupancy

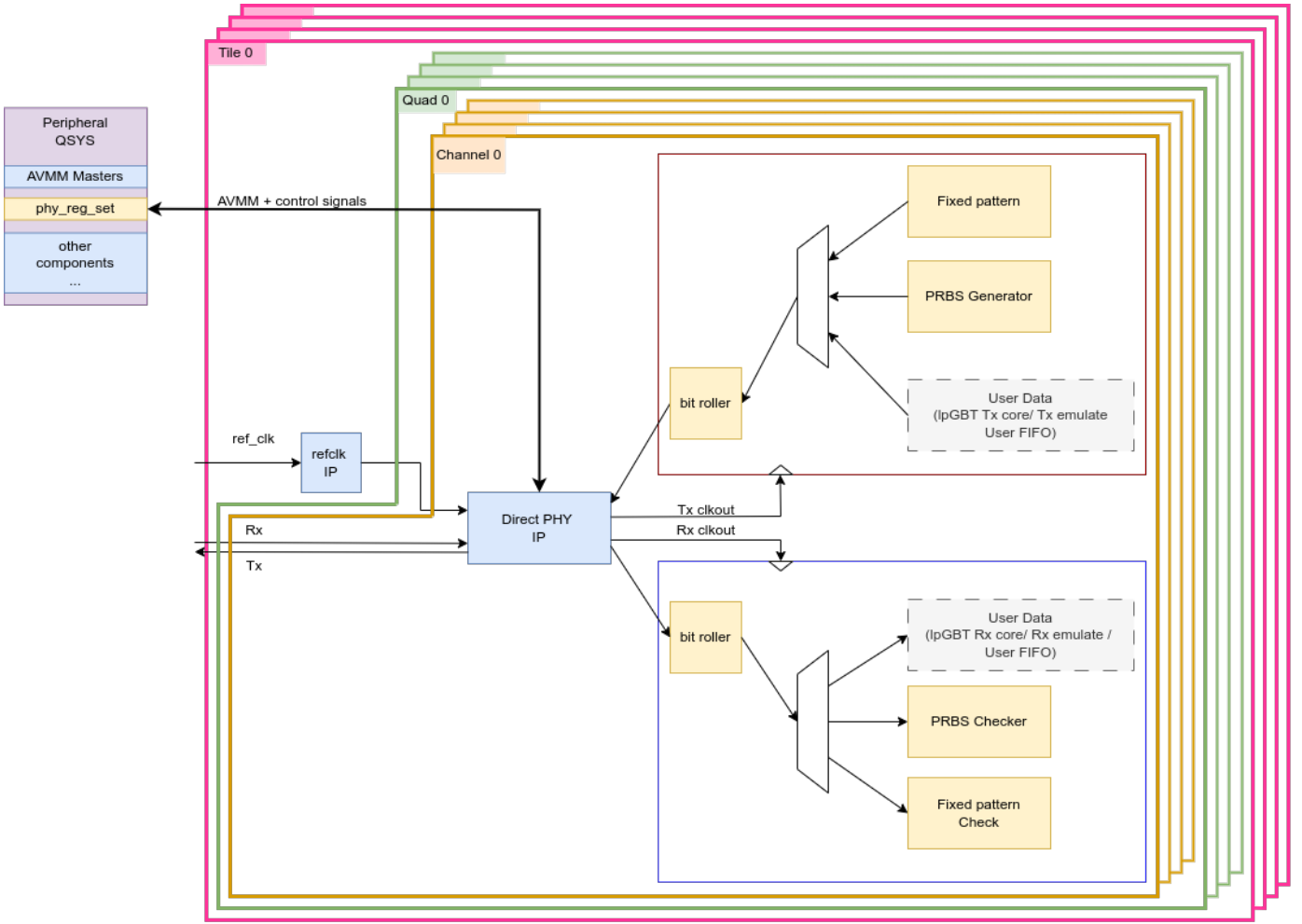
Design should be integrated to the LLI to benefit from all developped tools aside

***Deliberately not mentionned : PCIe and QSFP112 high speed serial links interfaces**

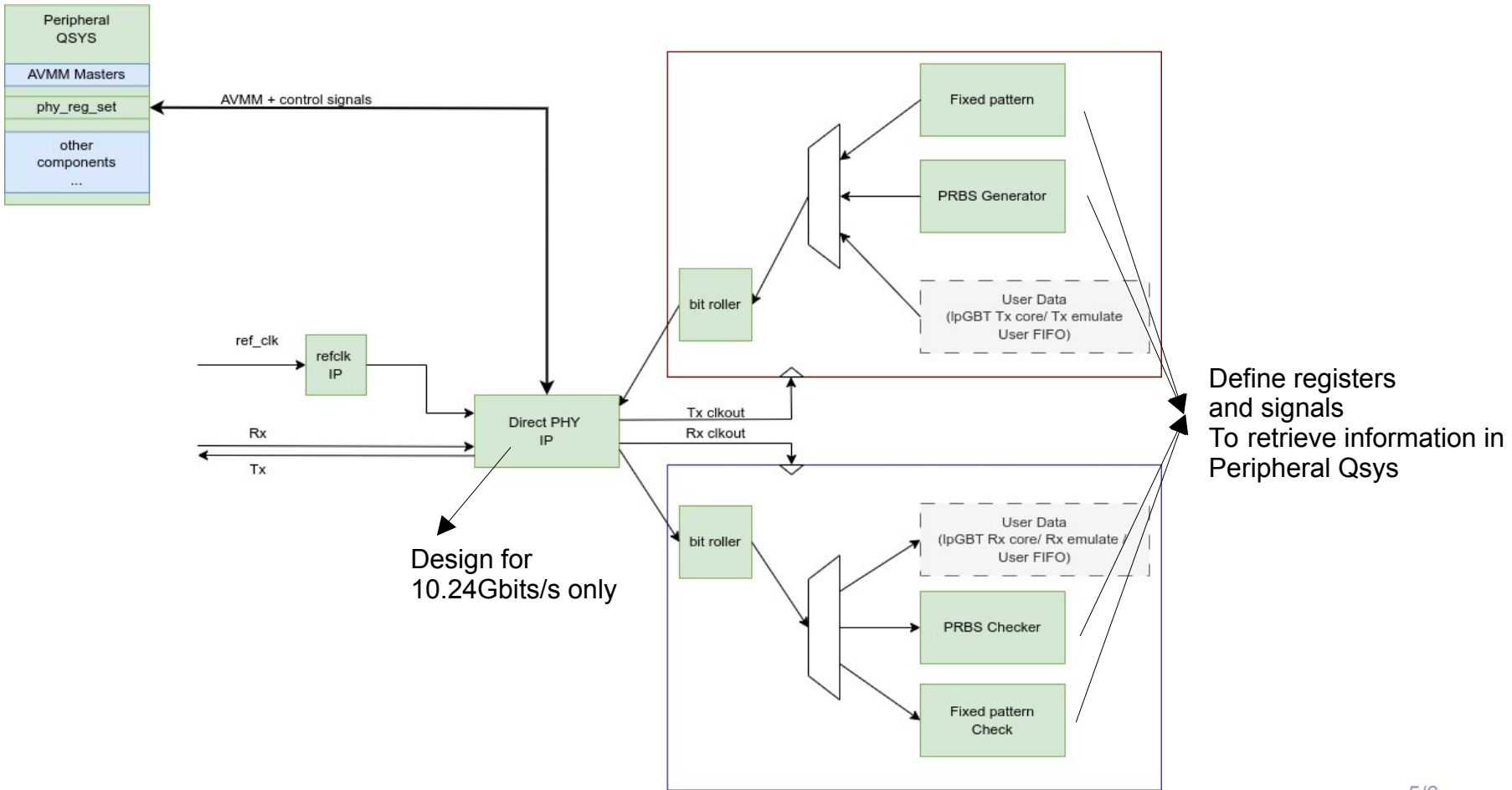
Serial links : conceptual view



Serial links : conceptual view



Serial links : existing developments



Heater : Definition

Shift register to generate logic occupancy

- Seed is randomly generated for each blocks
- Fed by a frequency configurable clock

Design can be reused from PCIe40