Test lli-pcie400
branch qsys_i2c_pcie_XP

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Setup

Tests sur les 2 devkit Agilex sur marupgrade15

- devkit I PCIe DK-DEV-AGI027RBES
- Devkit F PCIe DK-DEV-AGF014E2ES

Firmware :

- commit 67aa307C (qsys_i2c_pcie_XP) « Move mm_bridge_0.ip to source/peripherals folder. »

Améliorations apportées par Paolo, Xavier

- Ajout d'un IP JTAG to AVMM sur le BAR0 1 et 2
- Ajout d'un module pour récupérer le Serial Number du FPGA sur un registre spécifique accessible du AVMM
- Ajout du nom de la carte et un identifiant du BAR sur 2 registres spécifiques accessible du AVMM
- Ajout de l'ensemble des controlleurs de périphériques module « peripherals » branché sur le BAR2

Vérification des interfaces PCIe

8 interfaces PCIe visibles après programmation et reboot

```
$lspci | grep CERN

21:00.0 Communication controller: CERN/ECP/EDU Device ce40 (rev 01) → PCIe40
22:00.0 Communication controller: CERN/ECP/EDU Device ce40 (rev 01) → PCIe40
23:00.0 Communication controller: CERN/ECP/EDU Device ce80 (rev 01) → devkit F
24:00.0 Communication controller: CERN/ECP/EDU Device ce80 (rev 01) → devkit F
a1:00.0 Communication controller: CERN/ECP/EDU Device cecd (rev 01) → devkit I
a2:00.0 Communication controller: CERN/ECP/EDU Device cecd (rev 01) → devkit I
c1:00.0 Communication controller: CERN/ECP/EDU Device ce40 (rev 01) → PCIe40
c2:00.0 Communication controller: CERN/ECP/EDU Device ce40 (rev 01) → PCIe40
```

Affichage du Serial Number sur les devkit Agilex

```
$pcie40_id -e

Interface: 0
  FPGA: 00-54-01-90-28-A3-FE-0A
  Link: 0 (21:00.0)
  EEPROM: {"cn": "FEDD", "dt": "2019-10-08", "io": "24/0", "pn": "p40_fv22b20713", "serial_number_p40": "18-02411 - 0711"}
Interface: 1
  FPGA: 00-54-01-90-28-A3-FE-0A
  Link: 1 (22:00.0)
Interface: 2
  FPGA: 05-00-A1-FB-8C-A6-09-34
  Link: 0 (23:00.0)
Interface: 3
  FPGA: 05-00-A1-FB-8C-A6-09-34
  Link: 1 (24:00.0)
Interface: 4
  FPGA: 00-54-00-02-28-92-00-08
  Link: 0 (C1:00.0)
EEPROM: {"serial_number_p40": "18-02407 - 0014", "dt": "2018-08-02", "pn": "p40_fv21pr014", "cn": "FEDD", "io": "48/48"}
Interface: 5
  FPGA: 00-54-00-02-28-92-00-08
  Link: 1 (C2:00.0)
Interface: 6
  FPGA: 23-D3-1E-20-EF-7E-B5-92
  Link: 0 (A1:00.0)
  EEPROM: error in p40_i2c_r8_str()
Interface: 7
  FPGA: 23-D3-1E-20-EF-7E-B5-92
  Link: 1 (A2:00.0)
```

Vérification des registres d'identification

```
$./pcie40_aji -c 2 -d 0
2) -0x00000001- AGI FPGA Development Kit [1-2.4.3]
 0) 034BB0DD   AGIB027R29A(.|B|R0|R1|R3)/..
   0) 0x30006E00 Signal Tap #0
   1) 0x00486E00 (110:9) #0
   2) 0x0C206E00 JTAG to Avalon-MM #0
   3) 0x0C206E01 JTAG to Avalon-MM #1
   4) 0x0C206E02 JTAG to Avalon-MM #2
   5) 0x0C206E03 JTAG PHY #3
```

Identification du BAR → registre 0x8000_0000 en ASCII

- **JTAG to Avalon-MM #0** $./pcie40_aji -c 2 -d 0 -n **2** -a 0x80000000 -r retourne 0x42415230 = `BAR0`
- **JTAG to Avalon-MM #1** $./pcie40_aji -c 2 -d 0 -n **3** -a 0x80000000 -r retourne 0x42415232 = `BAR2`
- **JTAG to Avalon-MM #2** $./pcie40_aji -c 2 -d 0 -n **4** -a 0x80000000 -r retourne 0xC001BEEF BAR1 inactif ?

Lecture du Serial Number → registre 0x8000_0020 (HI) et 0x8000_0010 (LOW)

- Exemple devkit I S/N : 23-D3-1E-20-EF-7E-B5-92
  - $./pcie40_aji -c 2 -d 0 -n 2 -a 0x80000020 -r retourne **0x23D31E20**
  - $./pcie40_aji -c 2 -d 0 -n 2 -a 0x80000010 -r retourne **0xEF7EB592**

Lecture du « Nom » de la carte → registre 0x8000_0040 (HI) et 0x8000_0030 (LOW)

- Comment définir le nom d'une carte ?

Vérification du module peripheral

Modification du driver libaji pour ajouter la lecture du registre « BAR_ID » 0x80000_0000 pour identifier le nœud JTAG-to-Avalon MM attaché au BAR2.

- Tous les tests AVMM passent sur le devkit F et I
- Tous les tests I2C passent sur le devkit I, manque les tests I2C sur devkit F

```
platform linux -- Python 3.9.18, pytest-8.2.0, pluggy-1.5.0 -- /pcie400/software/JL/p400/venv/bin/python
cachedir: .pytest_cache
rootdir: /pcie400/software/JL/p400/jtag_libaji/p400-rw-aji
configfile: pyproject.toml
collected 11 items

test_100_avmm.py::test_read_avmm_by_interface_101 PASSED
test_100_avmm.py::test_read_avmm_by_interface_id_102 PASSED
test_100_avmm.py::test_read_avmm_by_interface_port_103 PASSED
test_100_avmm.py::test_read_avmm_by_interface_name_104 PASSED
test_100_avmm.py::test_read_avmm_by_device_105 PASSED
test_100_avmm.py::test_read_avmm_by_device_name_106 PASSED
test_100_avmm.py::test_read_avmm_by_node_107 PASSED
test_100_avmm.py::test_read_avmm_speed_benchmark_108
-------------------------------------------------------------------------------------------------
INFO [test_100_avmm test_read_avmm_speed_benchmark_108] Time elapsed for 100 reads 3.105
PASSED
test_100_avmm.py::test_read_avmm_speed_benchmark_optimize_109
-------------------------------------------------------------------------------------------------
INFO [test_100_avmm test_read_avmm_speed_benchmark_optimize_109] Time elapsed for 100 reads 0.068
PASSED
test_100_avmm.py::test_write_avmm_111 PASSED
test_100_avmm.py::test_write_avmm_multi_112 PASSED
```

```
(venv) marupgrade15:tests langouet (main *) $pytest test_200_i2c.py --testbench devkit_i_m15.yml
=================================================================================================
platform linux -- Python 3.9.18, pytest-8.2.0, pluggy-1.5.0 -- /pcie400/software/JL/p400/venv/bin/python
cachedir: .pytest_cache
rootdir: /pcie400/software/JL/p400/jtag_libaji/p400-rw-aji
configfile: pyproject.toml
collected 6 items

test_200_i2c.py::test_read_i2c_single_201 PASSED
test_200_i2c.py::test_read_i2c_multi_202 PASSED
test_200_i2c.py::test_read_i2c_speed_benchmark_203
-------------------------------------------------------------------------------------------------
INFO [test_200_i2c test_read_i2c_speed_benchmark_203] Time elapsed for 100 reads 1.030
PASSED
test_200_i2c.py::test_read_i2c_speed_benchmark_optimize_204
-------------------------------------------------------------------------------------------------
INFO [test_200_i2c test_read_i2c_speed_benchmark_optimize_204] Time elapsed for 100 reads 0.588
PASSED
test_200_i2c.py::test_write_i2c_single_205 PASSED
test_200_i2c.py::test_write_i2c_multi_206 PASSED
```