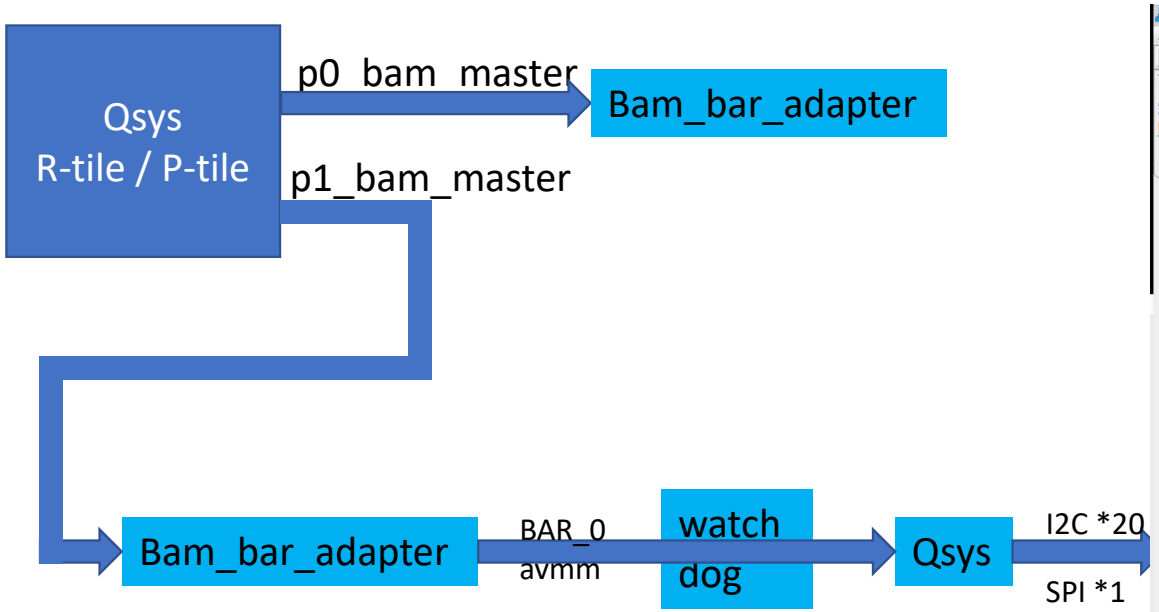
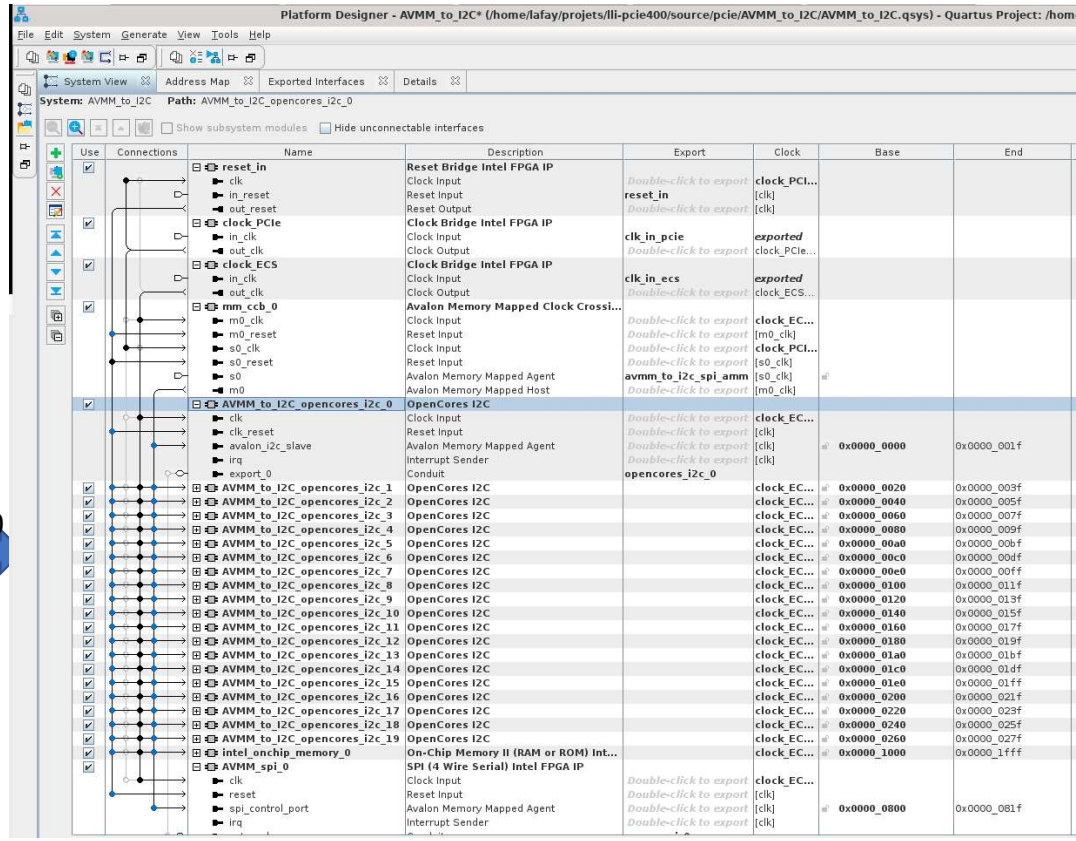
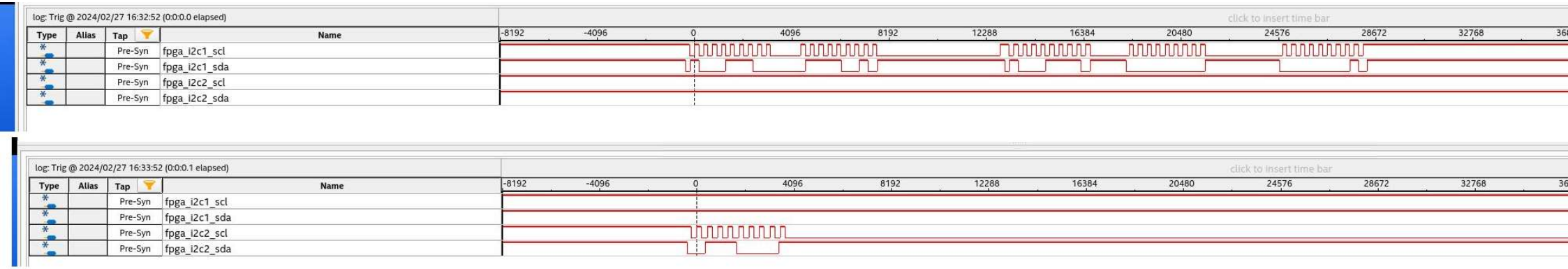
Instanciation Qsys pour piloter bus I2C et SPI à travers le PCIe


Qsys
R-tile / P-tile
p0_bam_master
p1_bam_master
Bam_bar_adapter
Bam_bar_adapter
BAR_0
avmm
watch
dog
Qsys
I2C *20
SPI *1


Platform Designer - AVMM_to_I2C* (/home/lafay/projets/lli-pcie400/source/pcie/AVMM_to_I2C/AVMM_to_I2C.qsys) - Quartus Project: /hom
File Edit System Generate View Tools Help
System View
Address Map
Exported Interfaces
Details
System: AVMM_to_I2C
Path: AVMM_to_I2C_opencores_i2c_0
Show subsystem modules
Hide unconnectable interfaces
Use
Connections
Name
Description
Export
Clock
Base
End
reset_in
Reset Bridge Intel FPGA IP
clk
Clock Input
in_reset
Reset Input
clock_PCIe
Clock Bridge Intel FPGA IP
clock_ECS
Clock Bridge Intel FPGA IP
mm_ccb_0
Avalon Memory Mapped Clock Crossi...
AVMM_to_I2C_opencores_i2c_0
OpenCores I2C
avalon_i2c_slave
0x0000_0000
0x0000_001f
AVMM_to_I2C_opencores_i2c_1
AVMM_to_I2C_opencores_i2c_2
AVMM_to_I2C_opencores_i2c_3
AVMM_to_I2C_opencores_i2c_4
AVMM_to_I2C_opencores_i2c_5
AVMM_to_I2C_opencores_i2c_6
AVMM_to_I2C_opencores_i2c_7
AVMM_to_I2C_opencores_i2c_8
AVMM_to_I2C_opencores_i2c_9
AVMM_to_I2C_opencores_i2c_10
AVMM_to_I2C_opencores_i2c_11
AVMM_to_I2C_opencores_i2c_12
AVMM_to_I2C_opencores_i2c_13
AVMM_to_I2C_opencores_i2c_14
AVMM_to_I2C_opencores_i2c_15
AVMM_to_I2C_opencores_i2c_16
AVMM_to_I2C_opencores_i2c_17
AVMM_to_I2C_opencores_i2c_18
AVMM_to_I2C_opencores_i2c_19
intel_onchip_memory_0
On-Chip Memory II (RAM or ROM) Int...
AVMM_spi_0
SPI (4 Wire Serial) Intel FPGA IP
spi_control_port
0x0000_0800
0x0000_081f


log: Trig @ 2024/02/27 16:32:52 (0:0:0.0 elapsed)
click to insert time bar
Type
Alias
Tap
Name
-8192
-4096
0
4096
8192
12288
16384
20480
24576
28672
32768
Pre-Syn
fpga_i2c1_scl
fpga_i2c1_sda
fpga_i2c2_scl
fpga_i2c2_sda
log: Trig @ 2024/02/27 16:33:52 (0:0:0.1 elapsed)
click to insert time bar

I2C devkit_I

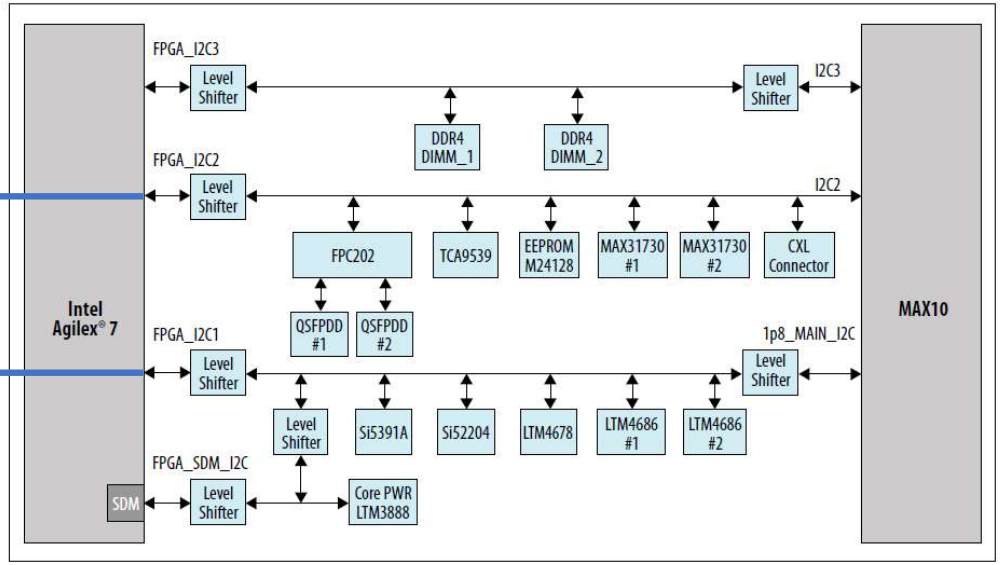
Table 9. I2C Device Address

Type	Bus	Address	Device
FPGA/Intel MAX 10 I2C Address	I2C1	0x74	Si5391
		0x6A	Si52204
		0x42	LTM4678/LTM4680
		0x45	LTM4686
		0x46	LTM4686
	I2C2	0x1E	FPC202
		0x57/0x5F	M24128
		0x38	MAX31730
		0x3A	MAX31730
		0xA0	QSFPDD_0
		0xA0	QSFPDD_1
		0x74	TCA9539
	I2C3	0xA1	DDR4_DIMM
		0xA0	DDR4_DIMM2
Intel MAX 10 I2C Address	AVS_I2C	0x47	LTC3888

OpenCore_I2C_1
0x0000 0020

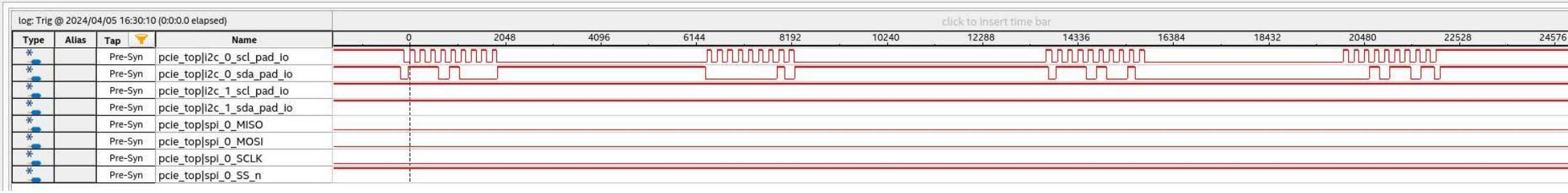
OpenCore_I2C_0
0x0000 0000

I2C Chain



- Communication avec le LTC3888 (via MAX10 ???) après programmation du FPGA ; la communication s'arrête après un certain nombre d'accès à l'I2C (> 100-200)

- La communication avec le LTC3888 semble perturber mes accès à l'I2C : des erreurs se peuvent se produire lors des premiers accès ; puis plus aucune erreur (coïncide avec l'arrêt de la communication avec le LTC3888)



I2C devkit_F

OpenCore_I2C_0
0x0000 0000

Figure 25. I²C Block Diagram

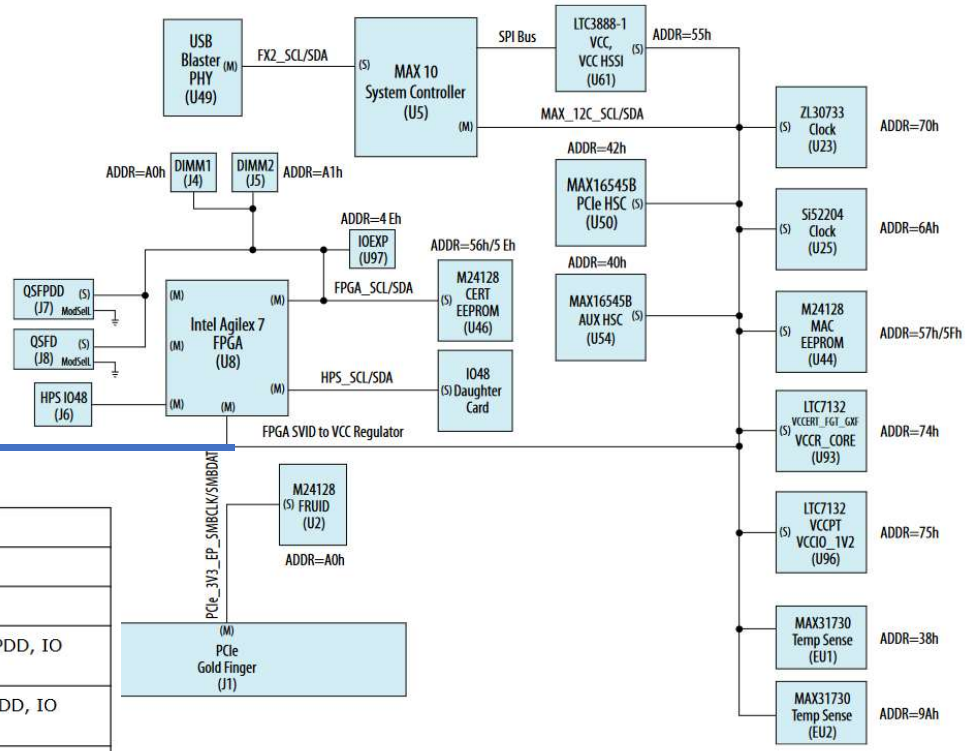


Table 38. FPGA I²C Signals

Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
FPGA_1V8_SVID_SCL	CG47	1.8 V open drain	Serial voltage ID I²C clock
FPGA_1V8_SVID_SDA	CB46	1.8 V open drain	Serial voltage ID I²C data
FPGA_1V2_SCL	K44	1.2 V open drain	FPGA I²C clock for DDR4 DIMMs, QSFP, QSFPDD, IO expander, and certificate EEPROM
FPGA_1V2_SDA	J43	1.2 V open drain	FPGA I²C data for DDR4 DIMMs, QSFP, QSFPDD, IO expander, and certificate EEPROM
HPS_SCL	N3	1.8 V open drain	HPS I/O48 daughter card I²C clock
HPS_SDA	L6	1.8 V open drain	HPS I/O48 daughter card I²C data

utilisation drivers

- i2c_bar0.prescale = p40_i2c_prescale(freq_avalon, freq_I2C);
- p40_i2c_open(interface,BAR,I2C_interface_Qsys,structurep40_I2C)
- p40_i2c_w8(structurep40_I2C,adresse_device,registre,data)
- int read = p40_i2c_r8 (structurep40_I2C,adresse_device,registre)
- p40_i2c_close(structurep40_I2C);

- Exemple : écrire 0x32 dans le registre page (0x01) du SI5391, et le relire
  - i2c_bar0.prescale = p40_i2c_prescale(40000000, 400000);
  - p40_i2c_open(3, 0, 0x00000000, &i2c_bar0);
  - p40_i2c_w8(&i2c_bar0, 0x74, 0x01, i);
  - int read = p40_i2c_r8(&i2c_bar0, 0x74, 0x01);
  - p40_i2c_close(&i2c_bar0);

Tests
devkit_i sur maruprage15 : /pcie400/gateware/XavierLAFAY/lhcb-daq40-software-devel-i2c/pcie40_i2c

- Boucle qui écrit et relis de 0 à 127 dans le registre de page ;
- boucle faite 1000 fois
- => pas d'erreur si pas de communication avec le LTC3888

```c
#include "i2c.h"

#define __STDC_FORMAT_MACROS
#include <inttypes.h> //PRIu64
#include <stdio.h>

int main()
{
  int i,nb_boucles;
  p40_i2c i2c_bar0 = {0};
//i2c_bar0.prescale = p40_i2c_prescale(freq_avalon, ?freq_i2c?);
  i2c_bar0.prescale = p40_i2c_prescale(40000000, 200000);

  p40_i2c_open(3, 0, 0x00000000, &i2c_bar0);


//int read = p40_i2c_r8(&i2c_bar0, adresse_composant_I2C, registre_composant);
  for (nb_boucles=0; nb_boucles<1000; nb_boucles++)
  {
    for (i=0; i<128; i++)
    {
      p40_i2c_w8(&i2c_bar0, 0x74, 0x01, i);
      int read = p40_i2c_r8(&i2c_bar0, 0x74, 0x01);
      if (i != read)
        printf("%i %x\n",i,read);
    }
    printf("boucle %i \n",nb_boucles);
  }
  p40_i2c_close(&i2c_bar0);
  return 0;
}
```