Dernières évolutions architecturales

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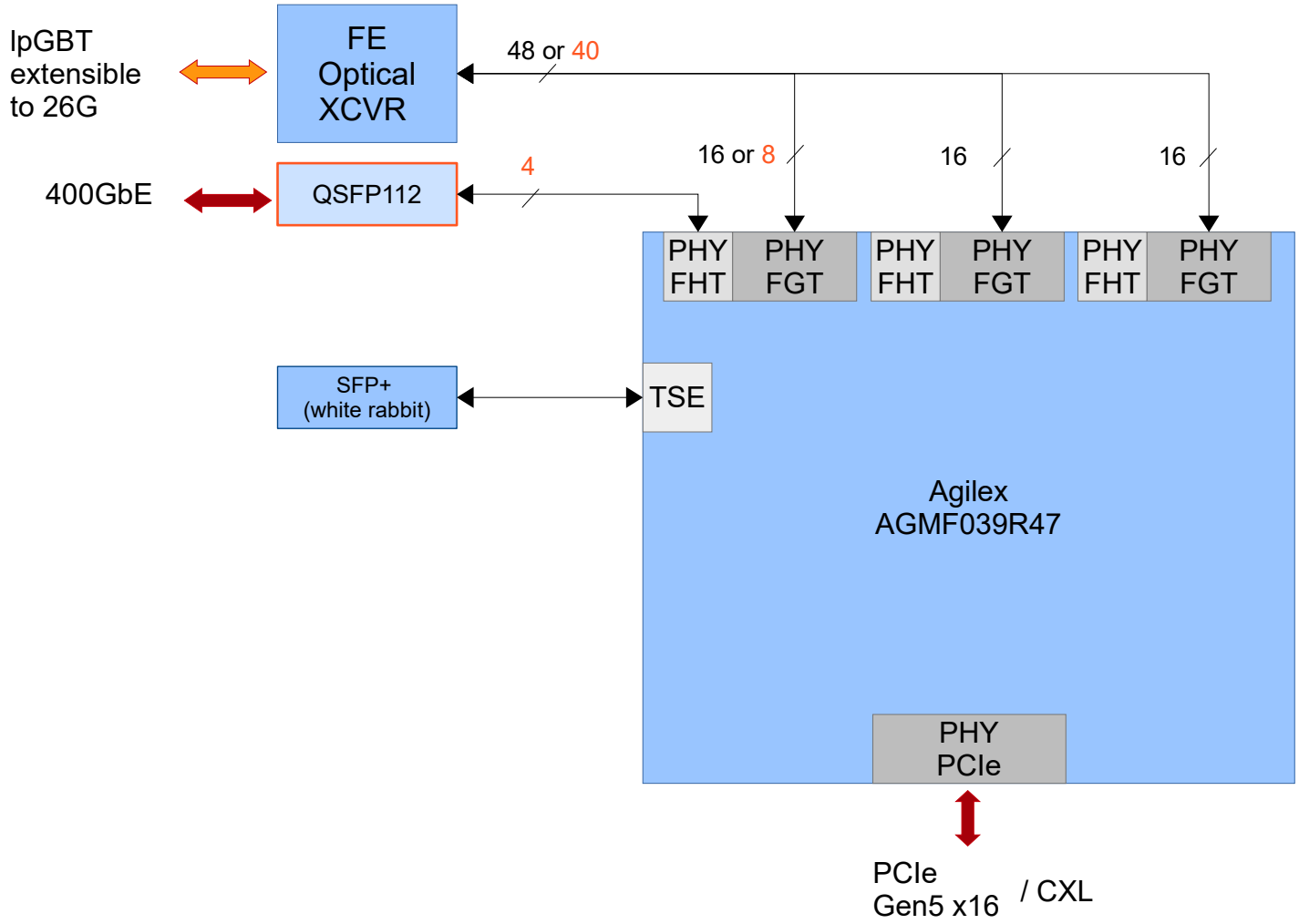
Résumé

- Implémentation des liens sériels TFC et WR
- Implémentation de l’arbre d’horloge

Serial links

Former serial link diagram



Missing dedicated link for fast control, white rabbit is only foreseen for clock distribution. Using lpGBT (point to point) links is possible but requires more PCIe400 on the overall system. TFC-PON has a ratio of 1 to 128.

TSE IP (ethernet over LVDS) leaves high speed serializer free but is limited to 1.6Gbps. White rabbit could evolve toward 10GbE.

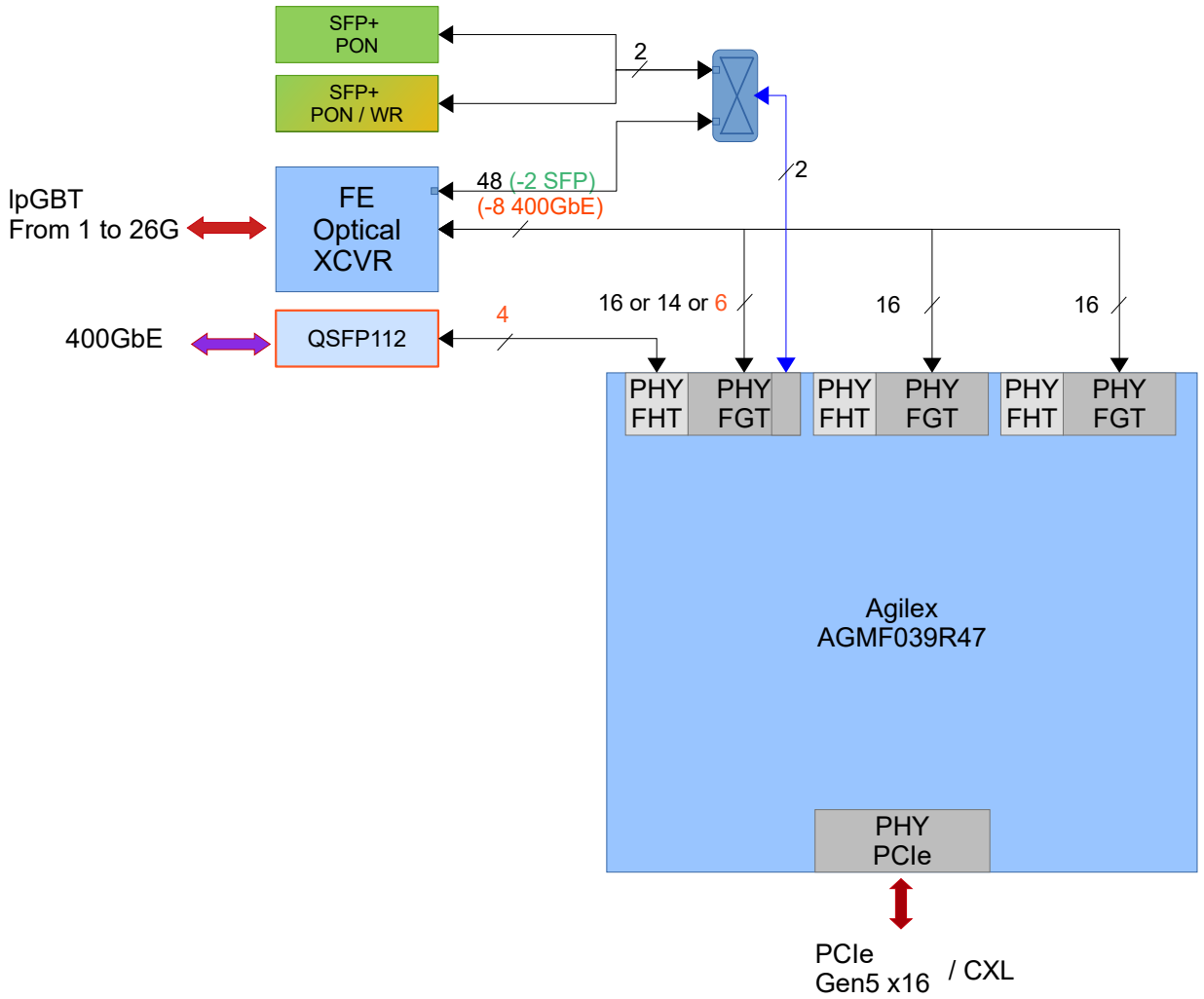
Proposition of serial link diagram

2 SFP+ cages wired to high speed serializer. SFP+ cage can accept a 1GbE optoelectronic XCVR (for WR) or a OLT/ONU PON optoelectronic XCVR.

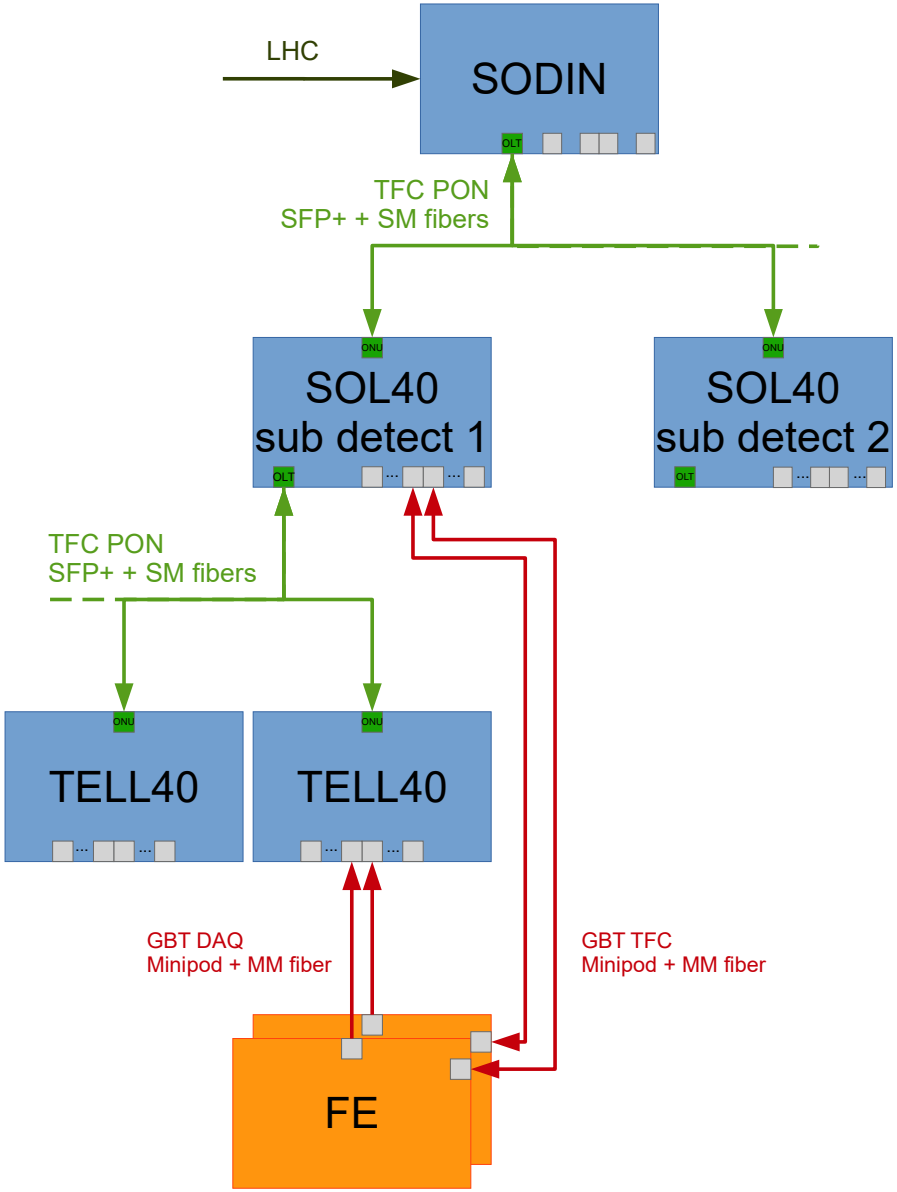
Number of bidir links available for FE :

Number of FE links	Use of SFP+	Use of 400GbE
48	✘	✘
46	✓	✓
40	✘	✓
38	✓	✓

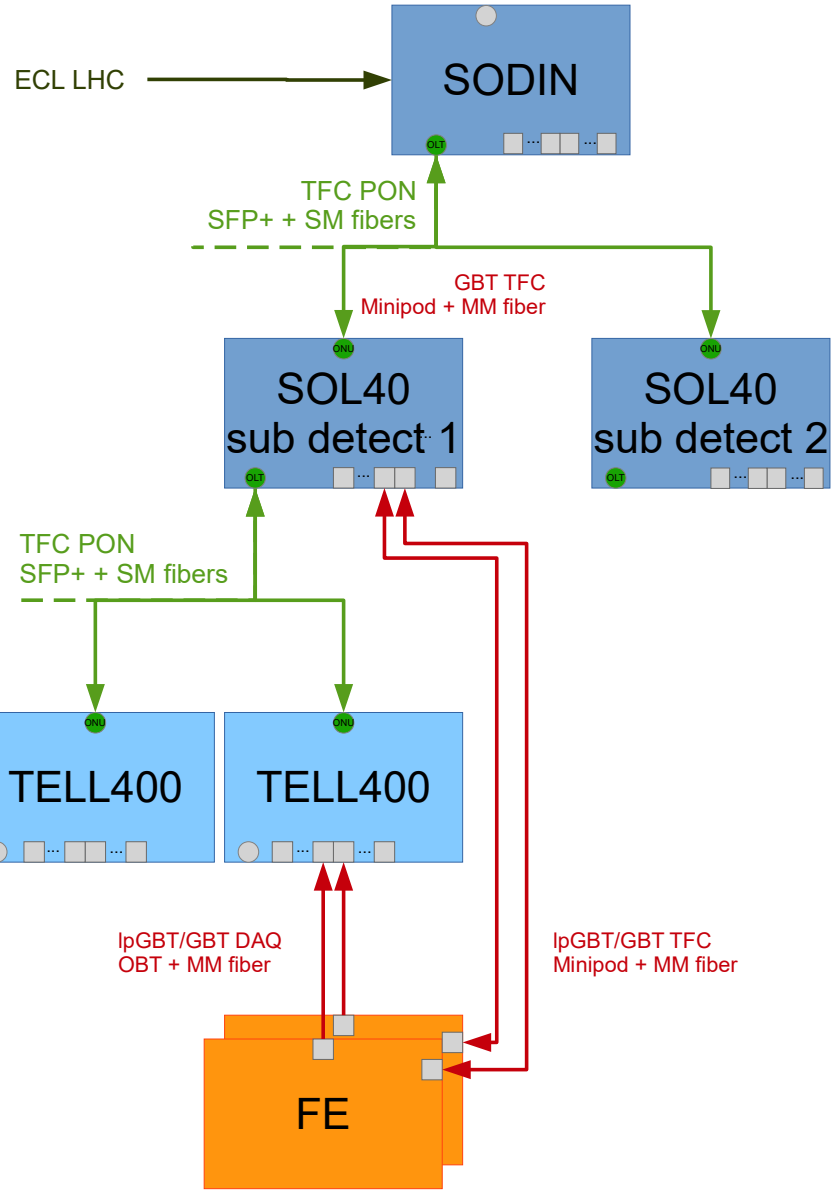
48 links still possible by adding a crossbar.
Using 400GbE makes 8 links unavailble for FE because of bandwidth limitation inside the FPGA.



Use case current system PCIe40



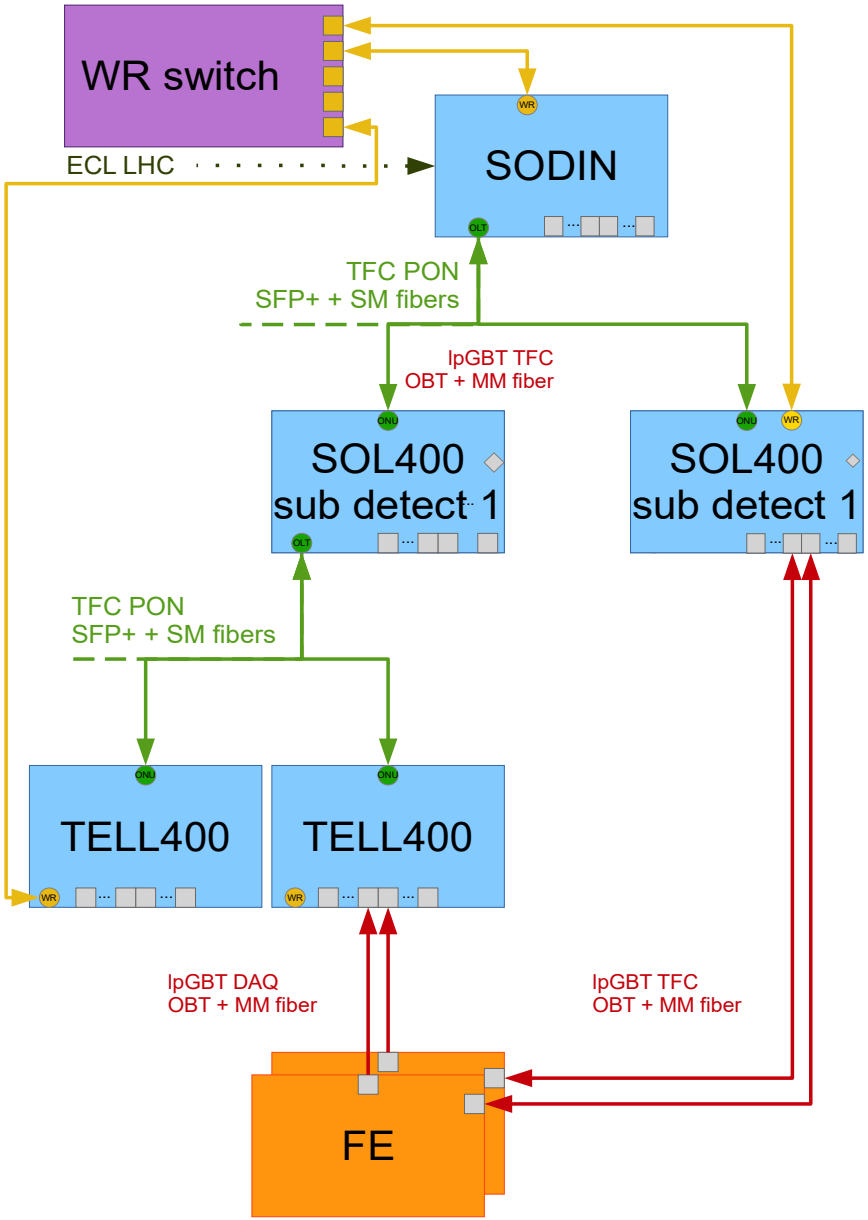
Use case : transition PCIe400 as TELL400



Use case : PCIe400 with WR

SOL400

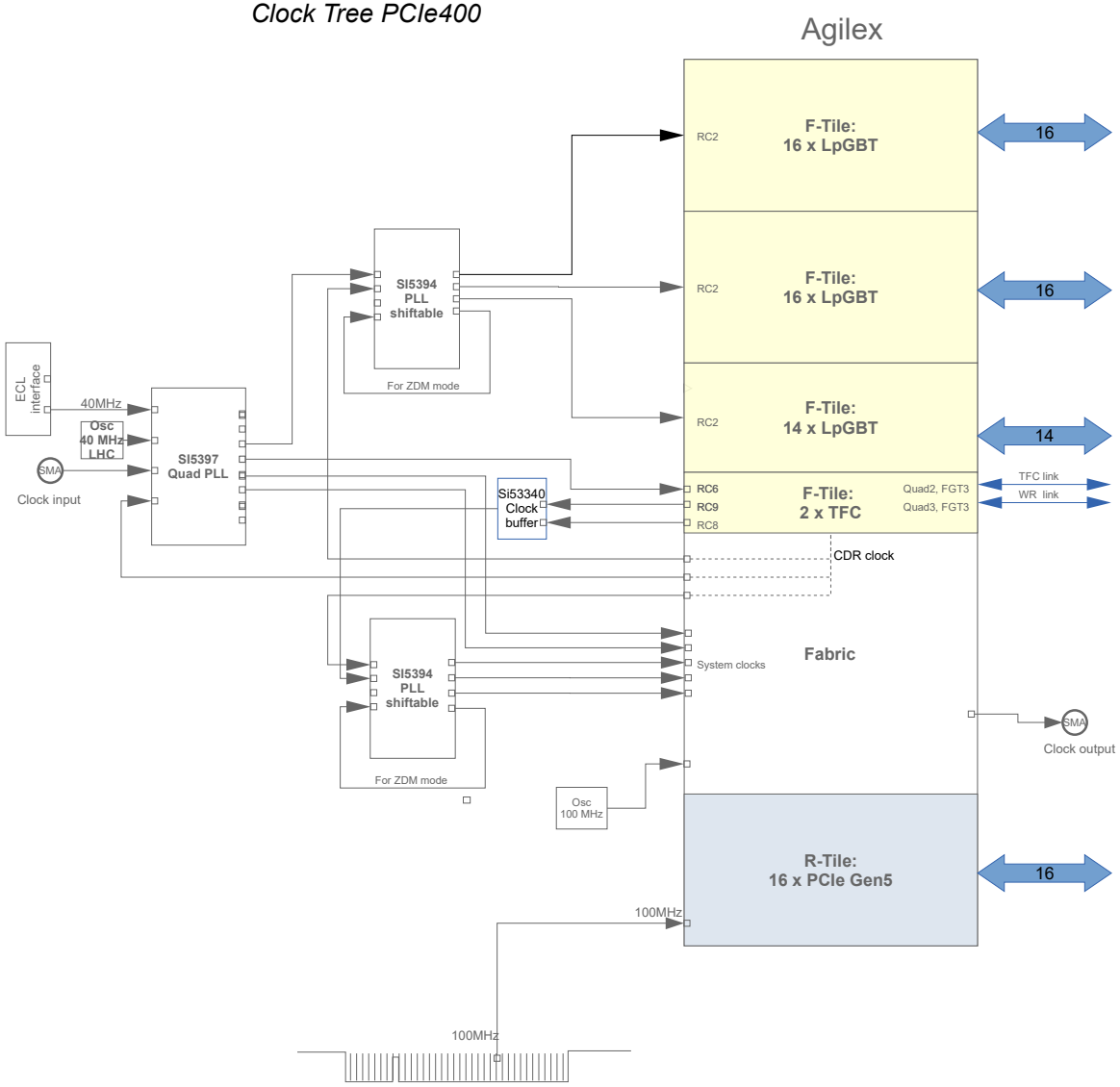
- To mitigate the fact that there is only 2 links for PON ONU, PON OLT and WR. More SOL400 are required to benefit from WR clock distribution for FE.



Clock tree

Former clock tree

Clock Tree PCIe400



Missing features

No FINC/FDEC on SI5394

Pin Name	Pin Number			Pin Type[1]	Function
	Si5395	Si5394	Si5392		
LOS0b	—	—	30	O	**Loss of Signal for IN0[3]** This pin indicate a loss of clock at the IN0 pin when low.
LOS1b	—	—	31	O	**Loss of Signal for IN1[3]** This pin indicate a loss of clock at the IN1 pin when low.
LOS2b	—	—	35	O	**Loss of Signal for IN2[3]** This pin indicate a loss of clock at the IN2 pin when low.
LOS3b	—	—	36	O	**Loss of Signal for IN3[3]** This pin indicate a loss of clock at the IN3 pin when low.
LOS_XAXBb	—	28	28	O	**Loss of Signal on XA/XB Pins[3]** This pin indicates a loss of signal at the XA/XB pins when low.
FINC	48	—	—	I	**Frequency Increment Pin[2]** This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.
FDEC	25	—	—	I	**Frequency Decrement Pin[2]** This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.

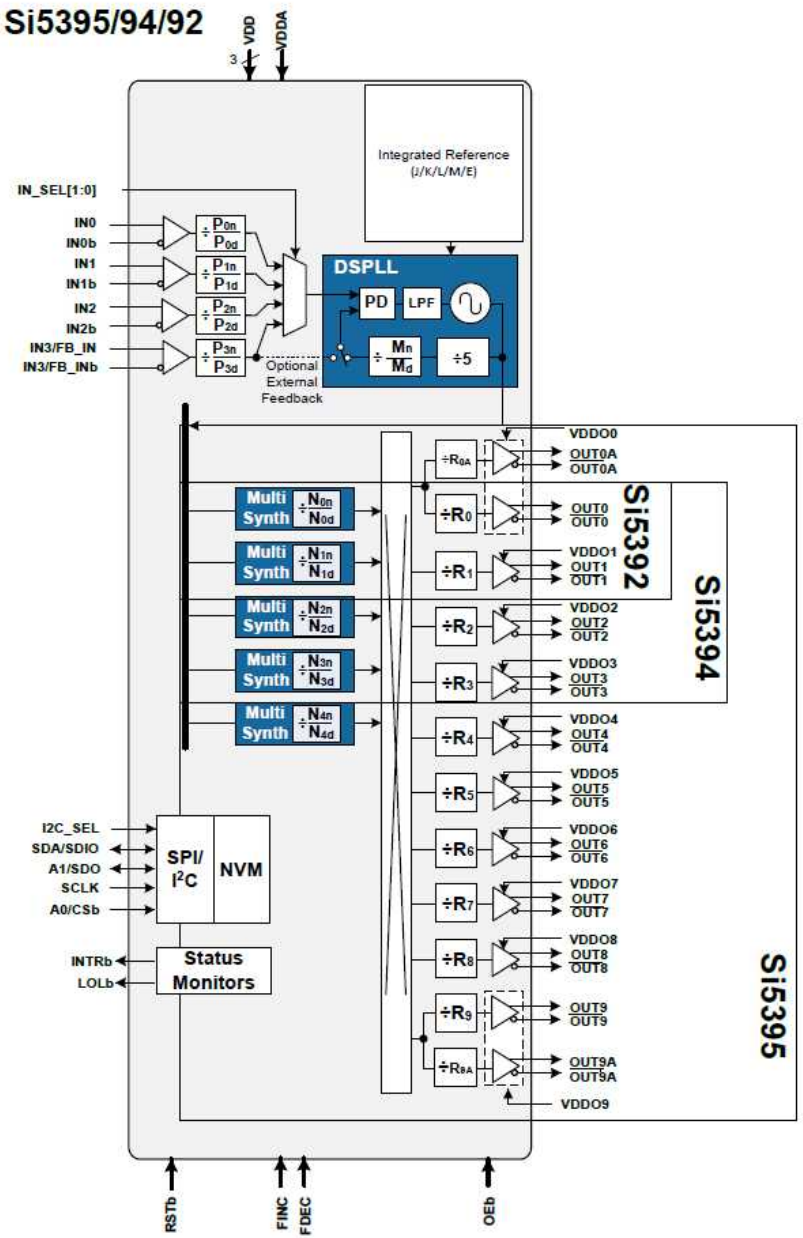
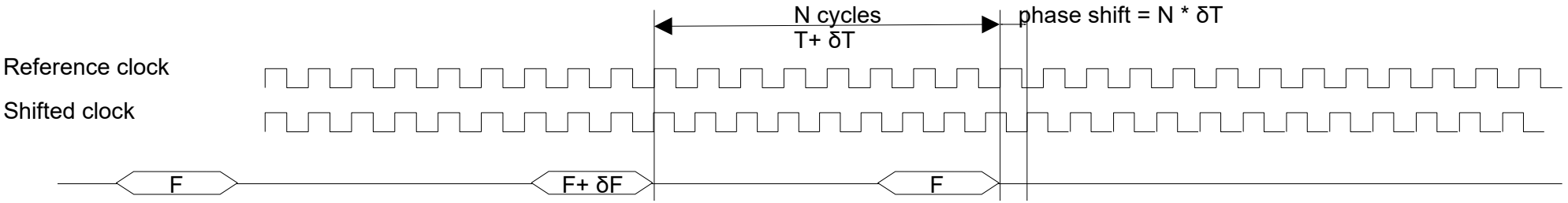


Figure 7.1. Si5392/94/95 Block Diagram

Phase adjust principle

Frequency increment or decrement during a controlled amount of clocks



Exemple :
F = 100 MHz
δF = 0.010001MHz
δT = 1/100000000 – 1/100010001 = 1ps
Programming of 100.010001 MHz during 500 cycles → phase shift = 500 ps

New clock tree

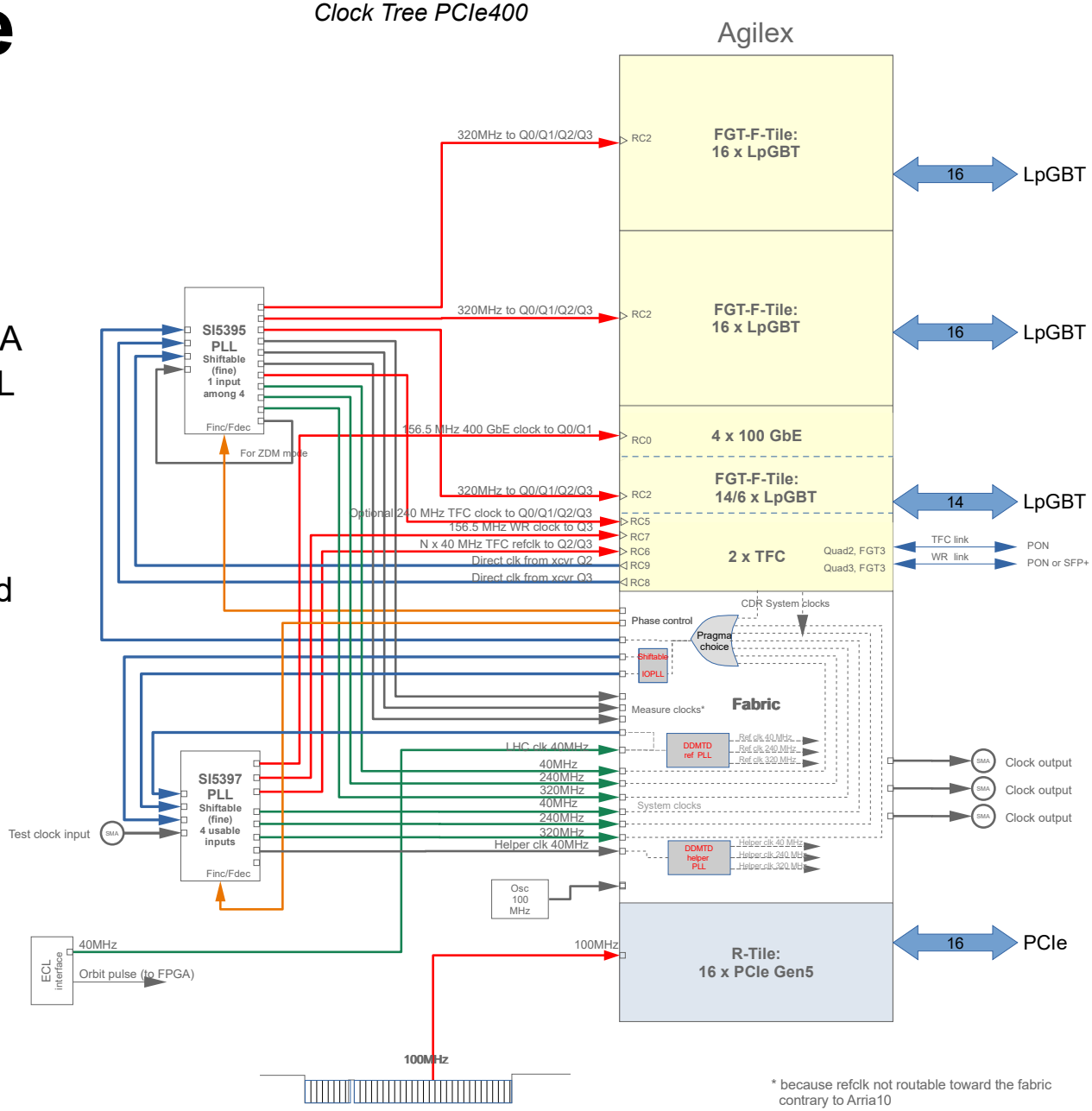
Simplifications

- only 2 PLLs,
- no more clock buffers
- SMA input directly on FPGA
- LHC freq generated by PLL in free running mode (internal source)

New features

- CDR cleaned clocks routed to xcvrs
- DDMTD helper clock

Clock Tree PCIe400



* because refclk not routable toward the fabric contrary to Arria10