

PCIe400 GIT repositories

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1. LHCb Upgrade Project

One board to rule them all

SODIN

SOL40

ECS

Front End Configuration/Monitoring

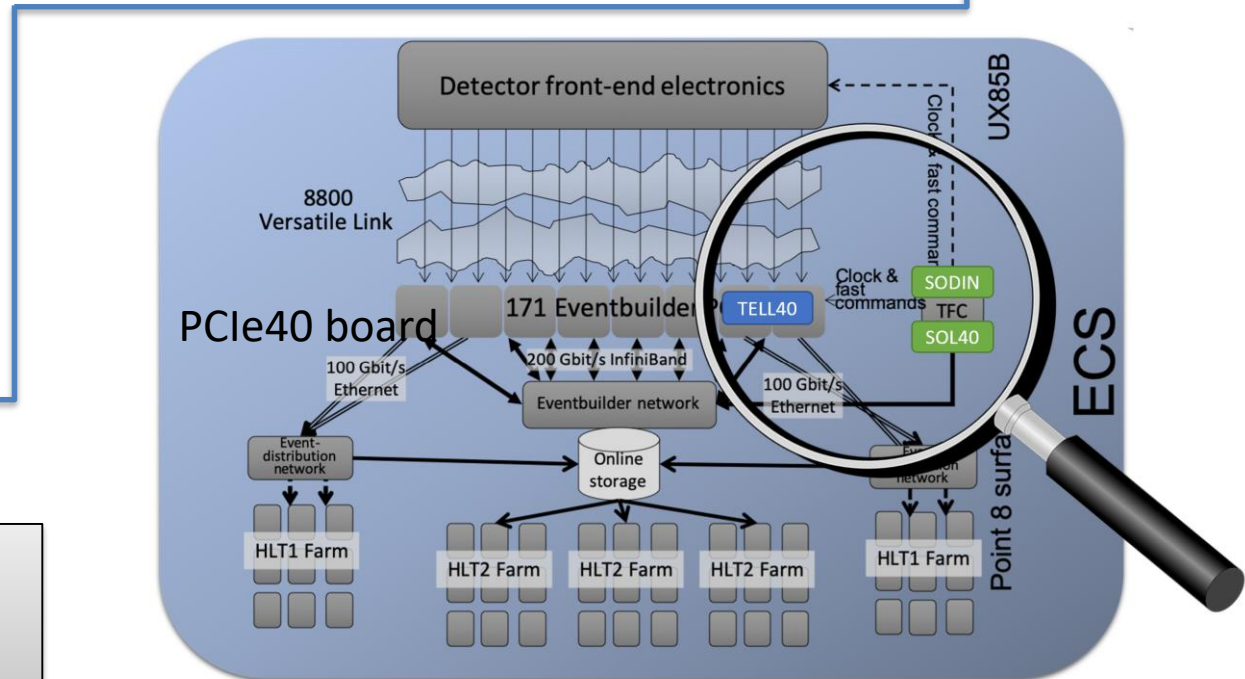
FE boards

TFC information

TFC information

TELL40

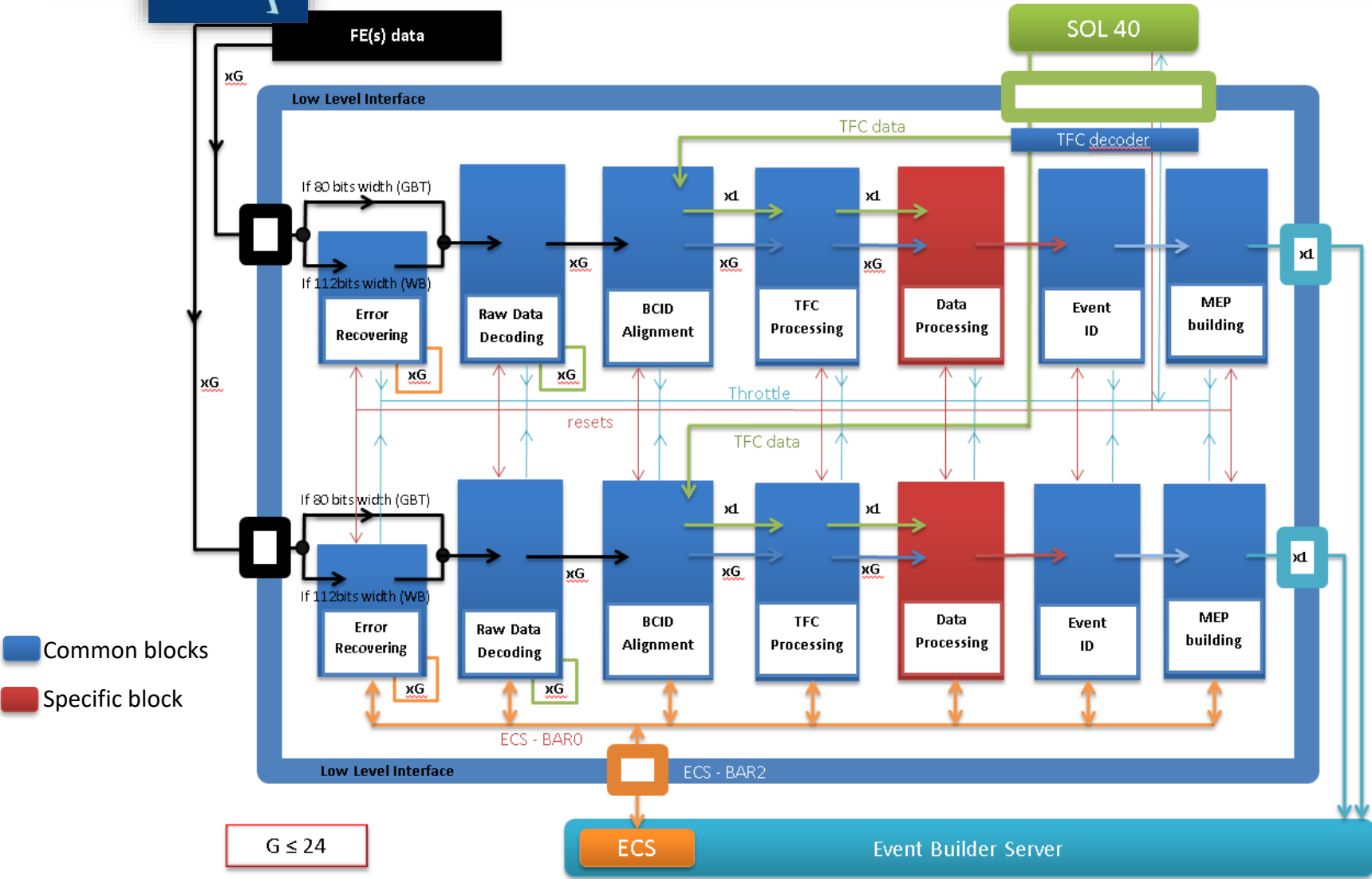
DATA



3 firmware flavors:

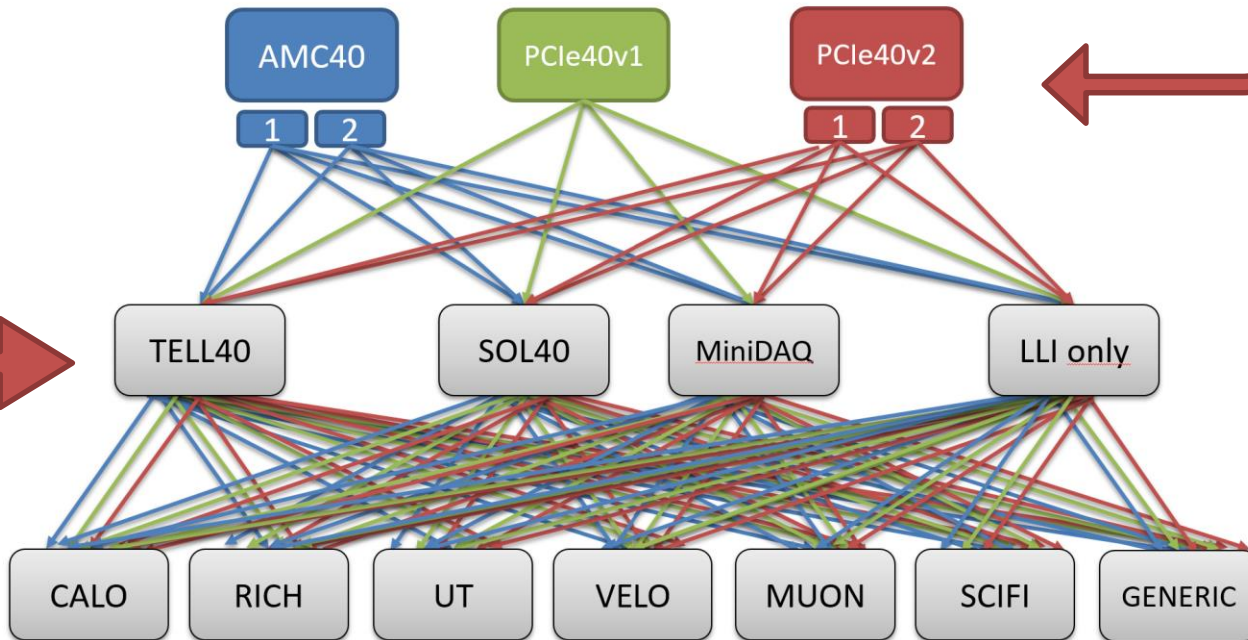
- SODIN
- SOL40
- TELL40

18/11/2021



PROBLEMS

- 5 hardware versions
- Many firmware flavors
 - 8 sub-detectors
- > 30 developers around the world





4. Firmware environment

SOLUTION

Créer un environnement de travail commun

- Etre capable de versionner le travail et de le partager de manière efficace
- Créer des scripts pour cacher la complexité de l'environnement de travail
- Créer des releases pour homogénéiser et déployer les développements de chaque partie.
- Intégrer une vérification continue et automatique pour valider les nouveaux développements.

Coordonner

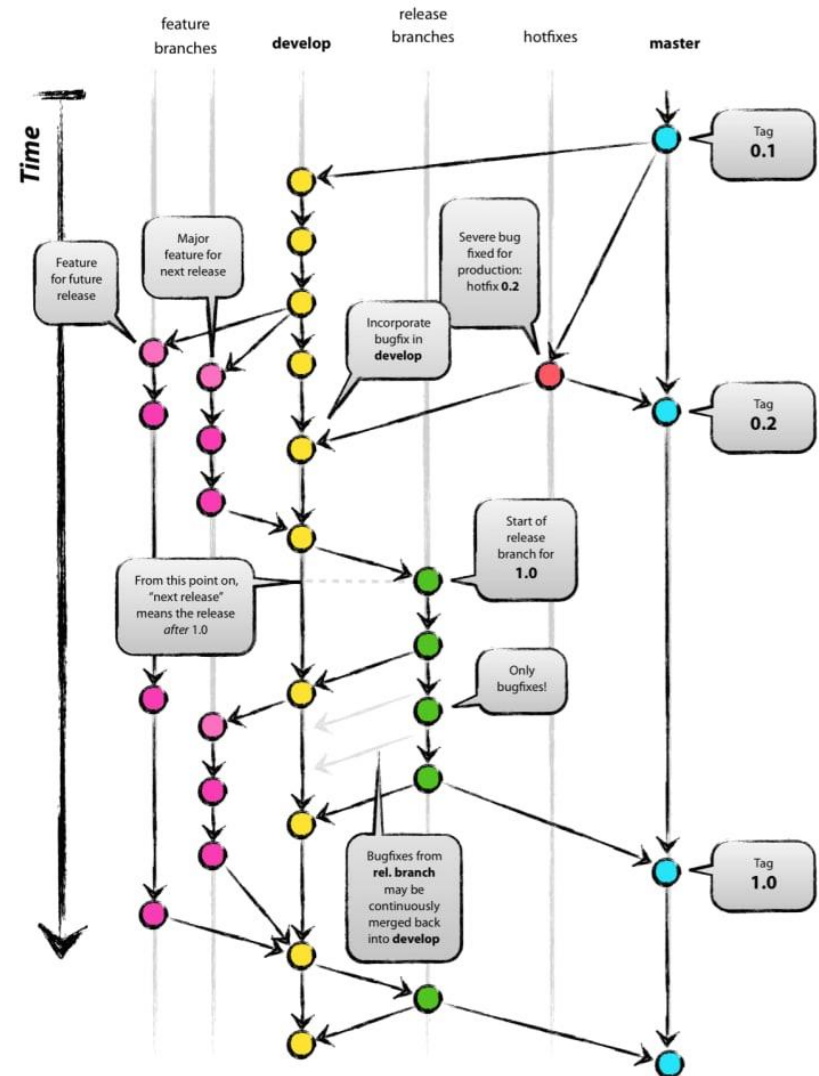
- Réunions
- Communication
- Documents
- Pédagogie
- Aide technique
- ...

Tout d'abord, c'est quoi Git ?

Il s'agit d'un logiciel de gestion de versions du code d'un projet informatique (**ou électronique**). Il s'agit d'un programme qui crée différentes versions d'un projet au fur et à mesure que les fichiers sont édités. Vous avez seulement à synchroniser, de manière manuelle ou automatique (à intervalle régulier par exemple), votre code en local, vers le serveur sur lequel il est hébergé. En effet, Git effectue des sauvegardes, snapshots de votre code chaque fois que vous le lui demandez. Il conviendra simplement d'ajouter quelques informations en renseignant le nom de la version que vous venez de créer. On appelle ces sauvegardes des Commits.

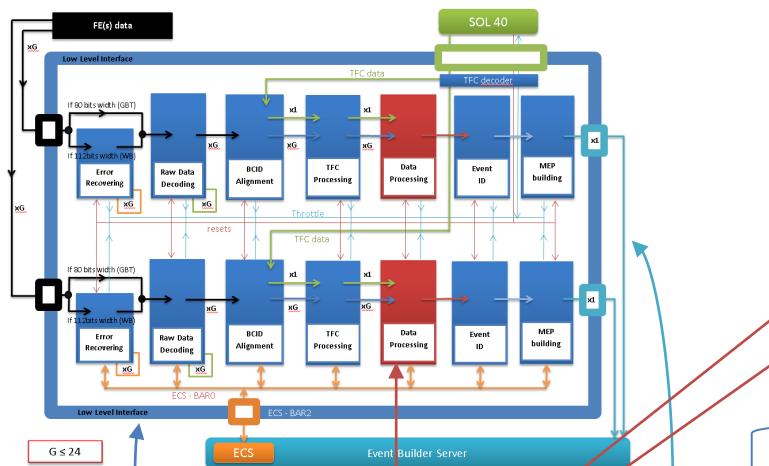
Pourquoi l'utiliser ?

- Modularisation
- Annuler vos erreurs
- travailler en mode déconnecté
- des pertes de données
- **Facilite la coordination des développements**



GIT architecture

Grace aux git sous-modules, il est tres facile d'avoir une organisation par block du firmware



Name	Last commit	Last update
bcm @ a8644397	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
calo @ 392ba839	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
data-generator @ 36456a98	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
l1i-amc40 @ 2Fc7F221	Update 'data-generator', 'l1i-amc40', 'l1i-gbt', 'l1i-simulation', 'scifi', '...	1 year ago
l1i-gbt @ d69b7cc8	Update 'bcm', 'calo', 'data-generator', 'l1i-gbt', 'l1i-pcie40v2', 'muo...	3 months ago
l1i-pcie40v1 @ bf94fefb	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
l1i-pcie40v2 @ a0beb027	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
l1i-simulation @ c3b617a0	Update 'data-generator', 'l1i-amc40', 'l1i-gbt', 'l1i-simulation', 'scifi', '...	1 year ago
muon @ feb62bc9	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
out-amc40 @ 64ffdaab	Update submodules 'l1i-pcie40v1', 'l1i-pcie40v2', 'out-amc40', 'out-...	1 year ago
out-pcie40 @ 515d8844	Update 'bcm', 'calo', 'data-generator', 'l1i-gbt', 'l1i-pcie40v2', 'muo...	3 months ago
rich @ cda93f28	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
scifi @ f9a0e8ac	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
scripts @ 1f9e3505	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
sodin @ 8bb02575	Update 'bcm', 'calo', 'data-generator', 'l1i-pcie40v1', 'l1i-pcie40v2', '...	3 weeks ago
sql40 @ 6942e033	Update 'bcm', 'calo', 'data-generator', 'l1i-gbt', 'l1i-pcie40v1', 'l1i-...	3 months ago



5. GIT

Name
bcm @ 3bc1587e
calo @ f16dac96
data-generator @ 6703deb1
lli-amc40 @ 2fc7f221
lli-gbt @ 8cb801f4
lli-pcie40v1 @ 09b7caee
lli-pcie40v2 @ ecb2a6de
lli-pon @ 394ddf5d
lli-simulation @ c3b617a0
mighty @ 0a76356c
muon @ f34cddd0
out-amc40 @ 64ffdaab
out-pcie40 @ 34af66d1
plume @ 46c654ed
rich @ d17ce2a4

Release X

Release X+1

New

New

New

New

New

New

GIT architecture
 Et les sous modules permettent de gerer les releases du code de facon local et global (grace aux TAGs)

In the main repository, the tag stores the commit to refer for each sub-modules

master tell40 age

16 Jun, 2021 4 commits

- Merge branch 'C_Sandbox' into 'master' Guillaume Vouters authored 5 months ago
- rebase from master Guillaume Vouters authored 5 months ago
- fix sync bunch of 10 bug in 3eport case Guillaume Vouters authored 5 months ago

0ba59326

31aa8f8d

da4921ed

2 types of scripts have been developed in order to hide the complexity of the GIT structure:

- **Scripts to handle the GIT repository with submodules**
 - SYNC (fetch)
 - CHECKOUT release
 - Start release
- **Scripts to help starting simulation (Mentor[QuestaSim]) and compilation (Intel[Quartus])**
 - Les scripts sont en .tcl (compris par Quartus et QuestaSim)
 - Seul les fichiers .vhd/.qsys/.ip/.sdc sont nécessaires de la part des utilisateurs



6. Scripts

SIMULATION SCRIPTS 1/2

Questa Sim-64 10.6c

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Layout NoDesign ColumnLayout AllColumns

Name	Type	Path
floatfixlib	Library	\$MODEL_TECH/./floatfixlib
ieee_env (empty)	Library	\$MODEL_TECH/./ieee_env
infect	Library	\$MODEL_TECH/./infect
mc2_lib	Library	\$MODEL_TECH/./mc2_lib
mgc_ams (empty)	Library	\$MODEL_TECH/./mgc_ams
mtiAvm	Library	\$MODEL_TECH/./avm
mtiOvm	Library	\$MODEL_TECH/./ovm-2.1.2
mtiPA (empty)	Library	\$MODEL_TECH/./pa_lib
mtiRnm	Library	\$MODEL_TECH/./rnm
mtiUPF	Library	\$MODEL_TECH/./upf_lib
mtiUvm	Library	\$MODEL_TECH/./uvm-1.1d
osvvm	Library	\$MODEL_TECH/./osvvm
sv_std	Library	\$MODEL_TECH/./sv_std
vhdipt_lib	Library	\$MODEL_TECH/./vhdipt_lib
vital2000	Library	\$MODEL_TECH/./vital2000
ieee	Library	\$MODEL_TECH/./ieee
modelsim_lib	Library	\$MODEL_TECH/./modelsim_lib
std	Library	\$MODEL_TECH/./std
std_developerskit	Library	\$MODEL_TECH/./std_developers
synopsys	Library	\$MODEL_TECH/./synopsys
verilog	Library	\$MODEL_TECH/./verilog

Convertir

Source

Source : screen:\\

Type : screen

Paramètres

Convertir

Affiche le flux de sortie

Désentrelacement

Profil Video - H.264 + MP3 (MP4)

Enregistrer le flux brut

Destination

Fichier de destination : E:\Videos\sim_video.mp4

Parcourir

Démarrer Annuler

Transcript

```
## // is prohibited from disclosure under the Trade Secrets Act,  
## // 18 U.S.C. Section 1905.  
## //  
QuestaSim>
```



6. Scripts

SIMULATION SCRIPTS 2/2

Questa Sim-64 10.6c

File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout Default

Library: work (Type: Library, Path: ./libraries/work/)

Transcript:

```
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/TEPX_data_concatenated has no driver.
# This port will contribute value (U) to the signal
# ** Warning: (vsim-8683) Uninitialized out port /top/tb/TELL40/data_proc/inst_process/concat_WB_noevtid/concatenation_wb_stepx_loop(23)/concat_step/latch_X/latch_stX/ready_OUT_S
# This port will contribute value (U) to the signal network.
# ** Warning: (vsim-8683) Uninitialized out port /top/tb/TELL40/data_proc/inst_process/concat_WB_noevtid/concatenation_wb_stepx_loop(23)/concat_step/latch_X/latch_stX/ready_OUT_S
# This port will contribute value (U) to the signal network.
```

Convertir

Source

Source : screen:\\

Type : screen

Paramètres

- Convertir
- Affiche le flux de sortie
- Désentrelacement

Profil: Video - H.264 + MP3 (MP4)

- Enregistrer le flux brut

Destination

Fichier de destination : E:\Videos\sim_video4.mp4

Démarrer Annuler

Now: 0 ps Delta: 0 sim:/top

Windows taskbar: 11:48 17/11/2021

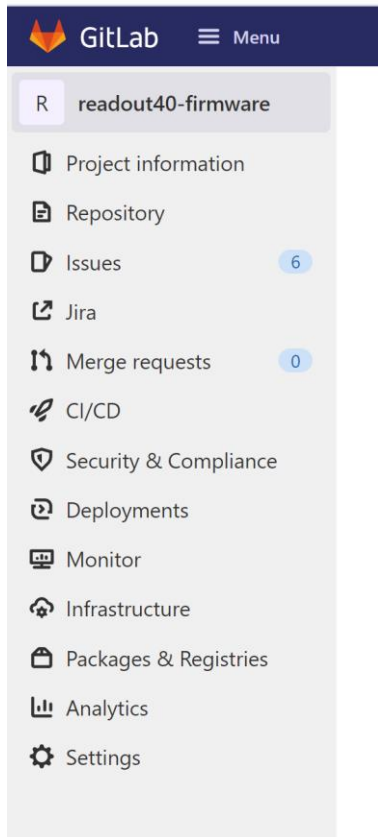


6. Scripts

The screenshot displays a Linux desktop environment. In the background, a terminal window titled 'admin@lappc-f510:~/GIT/firmware/test' shows a series of '\$' prompts and a file listing command 'll'. The listing output includes: 'total 4', 'drwxr-xr-x. 29 admin admin 4096 Nov', and 'admin@lappc-f510 test]#'. In the foreground, a 'Convertir' dialog box is open. The dialog has a 'Source' field containing 'screen:\\' and a 'Type' dropdown set to 'screen'. Under 'Paramètres', the 'Convertir' radio button is selected, while 'Affiche le flux de sortie' and 'Désentrelacement' are unchecked. The 'Profil' dropdown is set to 'Video - H.264 + MP3 (MP4)'. The 'Destination' section has a 'Fichier de destination' field containing 'E:\Videos\compil_video.mp4' and a 'Parcourir' button. At the bottom of the dialog are 'Démarrer' and 'Annuler' buttons. The desktop background is blue with 'CENTOS' branding and a '7' logo. The system tray at the bottom shows the date '08/11/2021' and time '16:46'.

La différence entre Git, Github ou Gitlab

Il est important de comprendre la différence entre Git et Github ou Gitlab. Git est un outil qui permet de gérer différents projets en les envoyant sur un serveur. Ce dernier est connecté à l'ordinateur d'autres développeurs qui envoient leur code et récupèrent le vôtre. Toute personne qui travaille sur un projet est connectée avec les autres, tout est synchronisé. Quant à GitHub et GitLab, il s'agit d'un logiciel, ou plateforme. Leur rôle est d'héberger ces différents projets qui utilisent Git. **Concrètement, ils proposent une interface graphique qui vous en simplifie l'utilisation et permet d'intégrer des fonctionnalités de gestion d'un dépôt Git.**



GitLab Menu

- R readout40-firmware
- Project information
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Name	Last commit
bcm @ a8644397	Update
calo @ 392ba839	Update
data-generator @ 36456a98	Update
lli-amc40 @ 2fc7f221	Update
lli-gbt @ d69b7cc8	Update
lli-pcie40v1 @ bf94fefb	Update
lli-pcie40v2 @ a0beb027	Update
lli-simulation @ c3b617a0	Update
muon @ feb62bc9	Update
out-amc40 @ 64ffdaab	Update
out-pcie40 @ 515d8844	Update
rich @ cda93f28	Update
scifi @ f9a0e8ac	Update 'bcm'
scripts @ 1f9e3505	Update 'bcm'
sodin @ 8bb02575	Update 'bcm'
calo @ 4942e033	Update 'bcm'

GitLab permet notamment:

- La gestion des droits du repository
- La creation de notification lors de merge, tag ou autre...
- La gestion participative des merge request
- La gestion des 'bugs' avec association aux branches et commits
- Des tests de vérification a chaque commit ou merge 'integration continue'
- Des stats
- ...



7. GitLab

CONTINUOUS INTEGRATION

Il est possible de générer des étapes de tests a chaque nouveau commit ou merge request ou TAG d'un repository.

Ce qui permet de vérifier certaines étapes importantes.

Possibilité aussi de créer un pipeline spécifique par chaque utilisateur.

The screenshot shows the GitLab CI/CD Pipelines page for the 'readout40-firmware' project. The main table lists four pipeline runs with their status, ID, trigger, commit, stages, and duration. A modal window titled 'Simulate' is open, showing a detailed view of the stages for a failed pipeline run (#2775924). The modal is divided into four columns: 'Simulate', 'Check', 'Compile', and 'Review'. Each column contains a list of jobs with their status and a refresh icon.

Status	Pipeline ID	Triggerer	Commit	Stages	Duration
failed	#2773254 Scheduled	[User]	master → 7c085755 Update 'bcm', 'calo', 'lli-gb...	[Icons: 1 failed, 2 warning, 2 success]	21:28:42 4 months ago
failed	#2772139 latest	[User]	v20210629-1 → 7c085755 Update 'bcm', 'calo', 'lli-gb...	[Icons: 1 failed, 1 warning, 3 success]	15:41:53 4 months ago
passed	#2771919	[User]	master → 7c085755 Update 'bcm', 'calo', 'lli-gb...	[Icons: 2 success]	00:33:23 4 months ago
failed	#2755924	[User]	merge/bcm@v6... → 7c085755 Update 'bcm', 'calo', 'lli-gb...	[Icons: 3 success, 1 failed, 1 warning, 3 success]	06:54:03 4 months ago

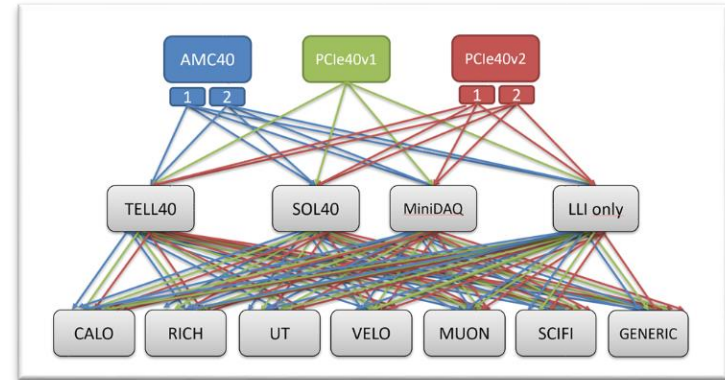
Simulate	Check	Compile	Review
[Success] mentor:pcie40v... [Refresh]	[Success] check:pcie40v1... [Refresh]	[Success] quartus:pcie40... [Refresh]	[Success] review:pcie40v... [Refresh]
[Success] mentor:pcie40v... [Refresh]	[Warning] check:pcie40v1... [Refresh]	[Success] quartus:pcie40... [Refresh]	[Success] review:pcie40v... [Refresh]

Scripts to handle the GIT repository with submodules

- SYNC (fetch)
- CHECKOUT release
- **Start release**
 - **Local tag 'sub-module'**
 - **Create a new branch in the main repository (with new submodule commits)**
 - **Create merge request to master (main repository)**
 - **Start a checking pipeline**
 - **merge request validation [human action]**
 - **Create a TAG to publish the release**

Release Checking Pipeline

- Simulation
- Simulation checker
- Compilation
- Compilation timing checking
- Compilation hardware test



1 related merge request: !230 Merge 'merge/bcm@v6.0.13+calo@v6.1.15+l1-pcie40v2@v6.5.3+l1-pon@v6.0.2+muon@v6.1.16+plume@v6.1.17+rich@v6.3.12+scifi@v6.6.1+scripts@v6.5.7+sodin@v6.3.7+sol40@v6.2.8+test@v6.2.13+tfcc@v6.2.15+top-level@v6.2.12+ut@v6.2.14+velo@v6.3.1'

Defines what job should be started

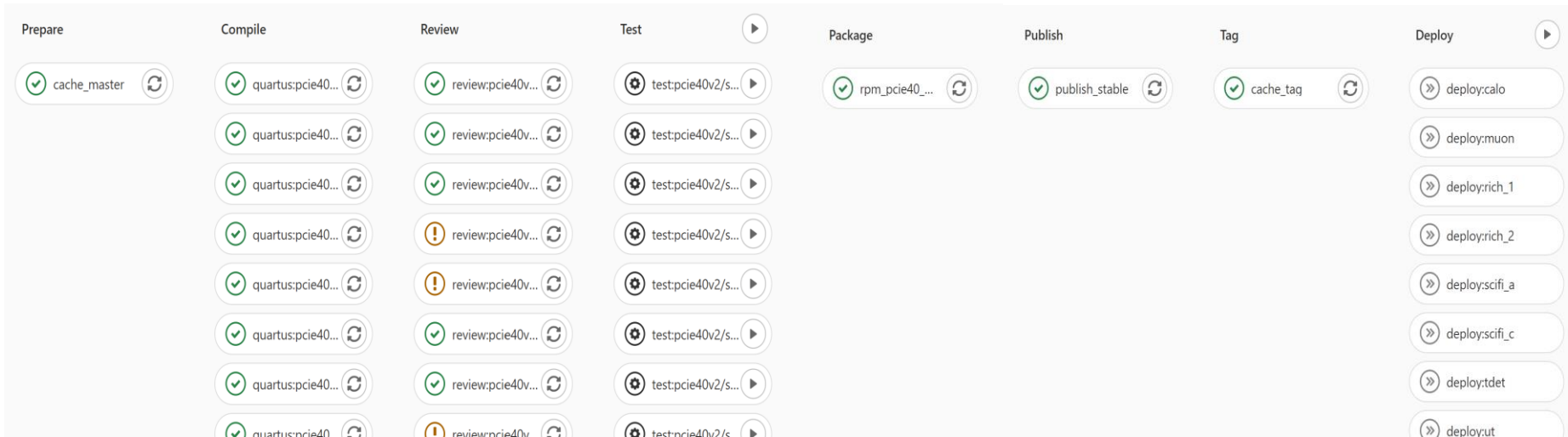
Pipeline Needs Jobs 354 Failed Jobs 74 Tests 0

Group jobs by Stage Job dependencies

Prepare	Simulate	Check	Compile	Review	Test
cache_master	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
create_mr	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...
	mentor:pcie40v...	check:pcie40v1...	quartus:pcie40...	review:pcie40v...	test:pcie40v2/ll...

Release Pipeline

- Compilation
- Compilation timing checking
- Compilation hardware test
- RPM
- déploiement





8. Firmware dependencies

GIT PROJECT

Le firmware est souvent lié au software, c'est tres difficile de rendre les 2 indépendants.

lhcb-readout40

lhcb-readout40 Group ID: 8234 [Leave group](#) 🔔 New subgroup New project

This project contains the firmware code for the readout boards of the LHCb upgrade project

Recent activity Last 90 days **Merge Requests opened** 48 **Issues opened** 26 **Members added** 0

Subgroups and projects Shared projects Archived projects

> F firmware Owner	0 32 2
> S software Owner	0 22 1
R readout40-docs Documentation repository for LHCb Upgrade Readout System	★ 6 10 months ago
R readout40-firmware Maintainer Firmware repository for LHCb Upgrade Readout System	★ 17 2 months ago
R readout40-software Software repository for LHCb Upgrade Readout System	★ 10 2 months ago



8. Firmware dependencies

SOFTWARE

Des pipeline de verification de release ont été aussi implémentés dans le coté software.
Les releases sont toujours réalisées en synchronization entre firmware et software

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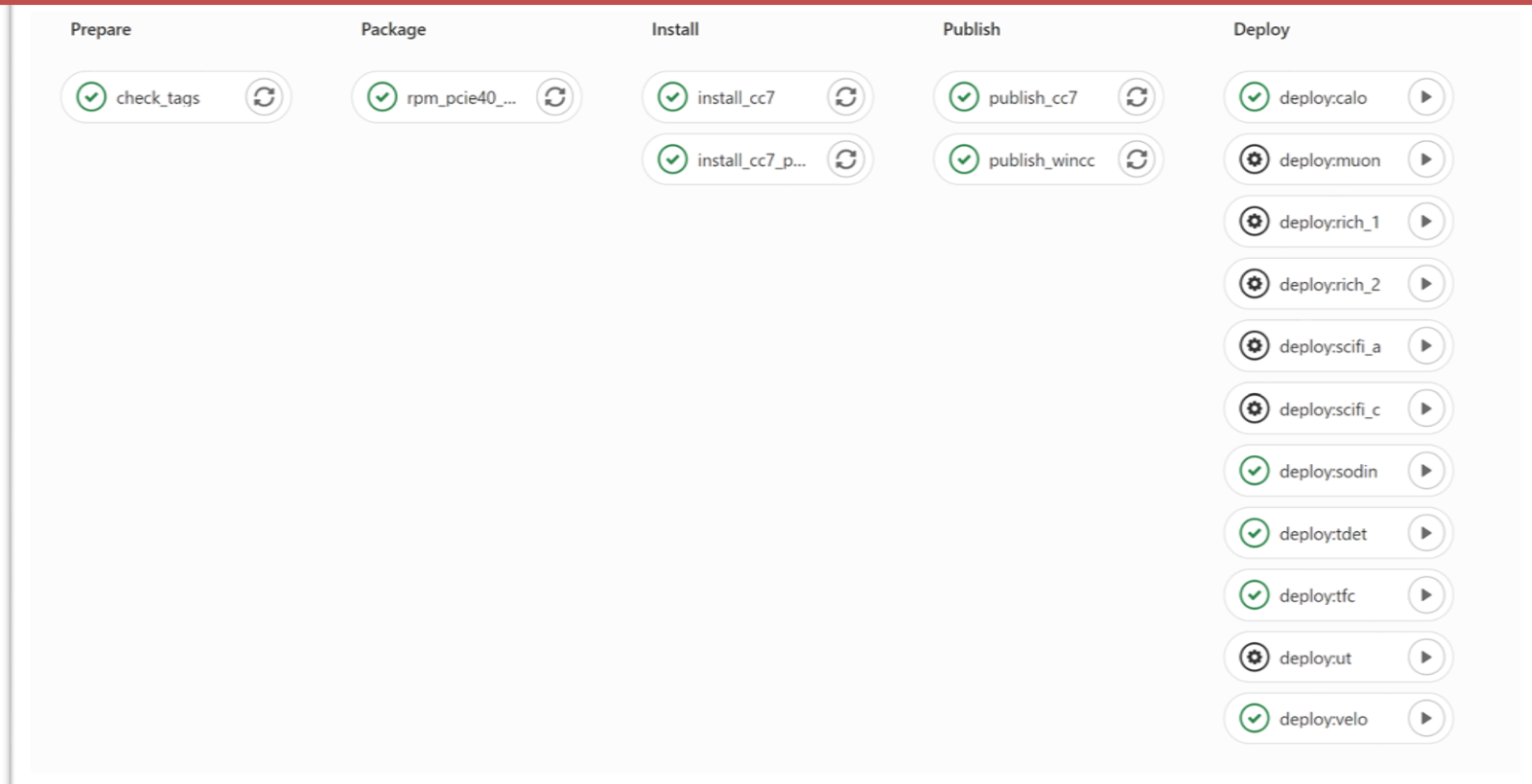
lhcb-readout40 > readout40-software > Pipelines

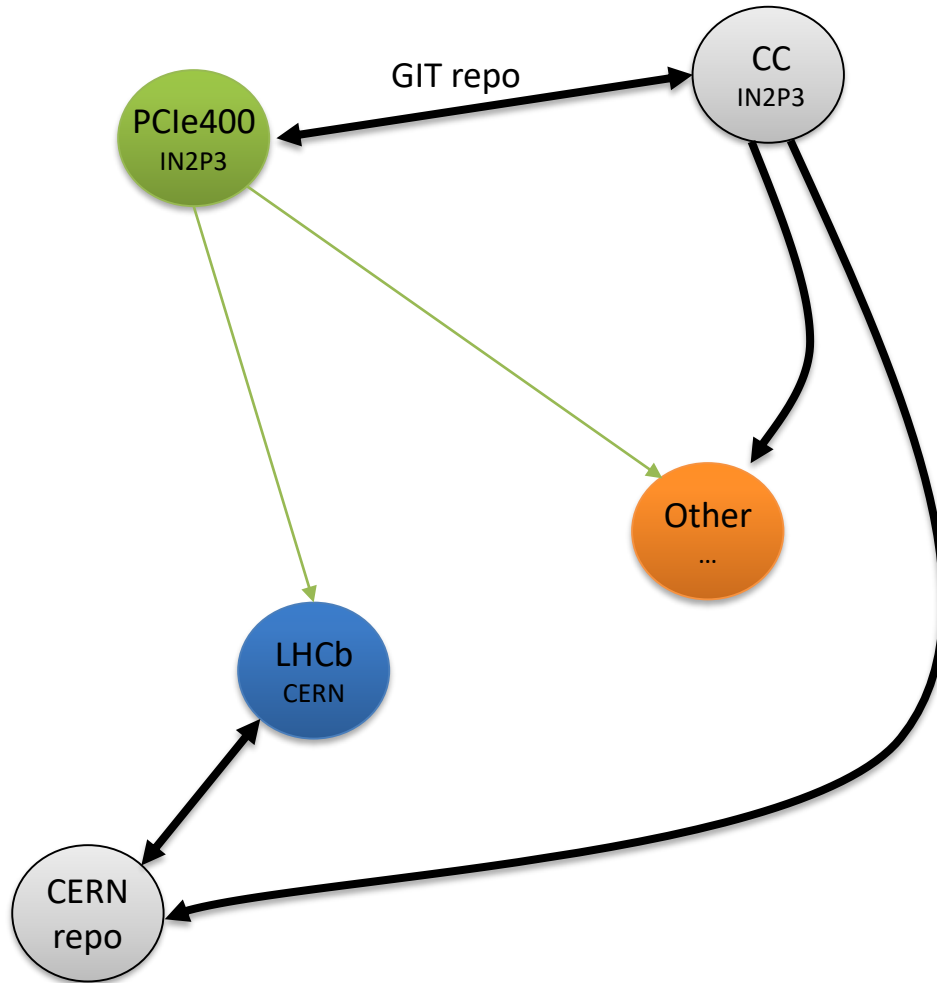
All 46 Finished Branches Tags

Filter pipelines

Status	Pipeline ID	Triggerer	Commit	Stages
passed	#3114378 latest		v20211006-1 -o- c5383c7b Update 'p40-lli-devices', 's...	✓ ✓ ✓ ✓ ✓
passed	#3095554 latest		v20211006-1 -o- c5383c7b Update 'p40-lli-devices', 's...	✓ ✓ ✓ ✓ !
passed	#3095176 latest		master -o- c5383c7b Update 'p40-lli-devices', 's...	✓ ✓ ✓ ! »

Des RPMs sont ainsi créés (firmware et software) pour ensuite être distribués sur le net.







Example firmware PCIe400 GIT structure

