Status CE65v2_xx chip

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CE65v2_xx (1.5mm x 1.5mm)

Versatile exploratory chip using matrix of pixels (48 col x 24 row) output is multiplexed to one analogue channel (matrix rolling shutter readout mode):

- ✓ share common pads structure, carrier and proxy boards
- ✓ 4 power domains: 3.3V analogue, 1.2 analogue, 3.3 digital, 1.2 digital
- ✓ 3.3 analog and 1.2 analog share same ground AVSS
- ✓ 3.3 digital and 1.2 digital share same ground DVSS

Power:

- digital (3.3V IO/1.2V CORE): DVDD33, DVDD12,DVSS
- analogue (3.3V): AVDD33, AVSS
- analogue (1.2V): AVDD12, AVSS

3 digital input pulses (3.3V): clock, start, calib

3 unprotected pads: HV, NWELL, PWELL

Output in 1.2V analogue domain

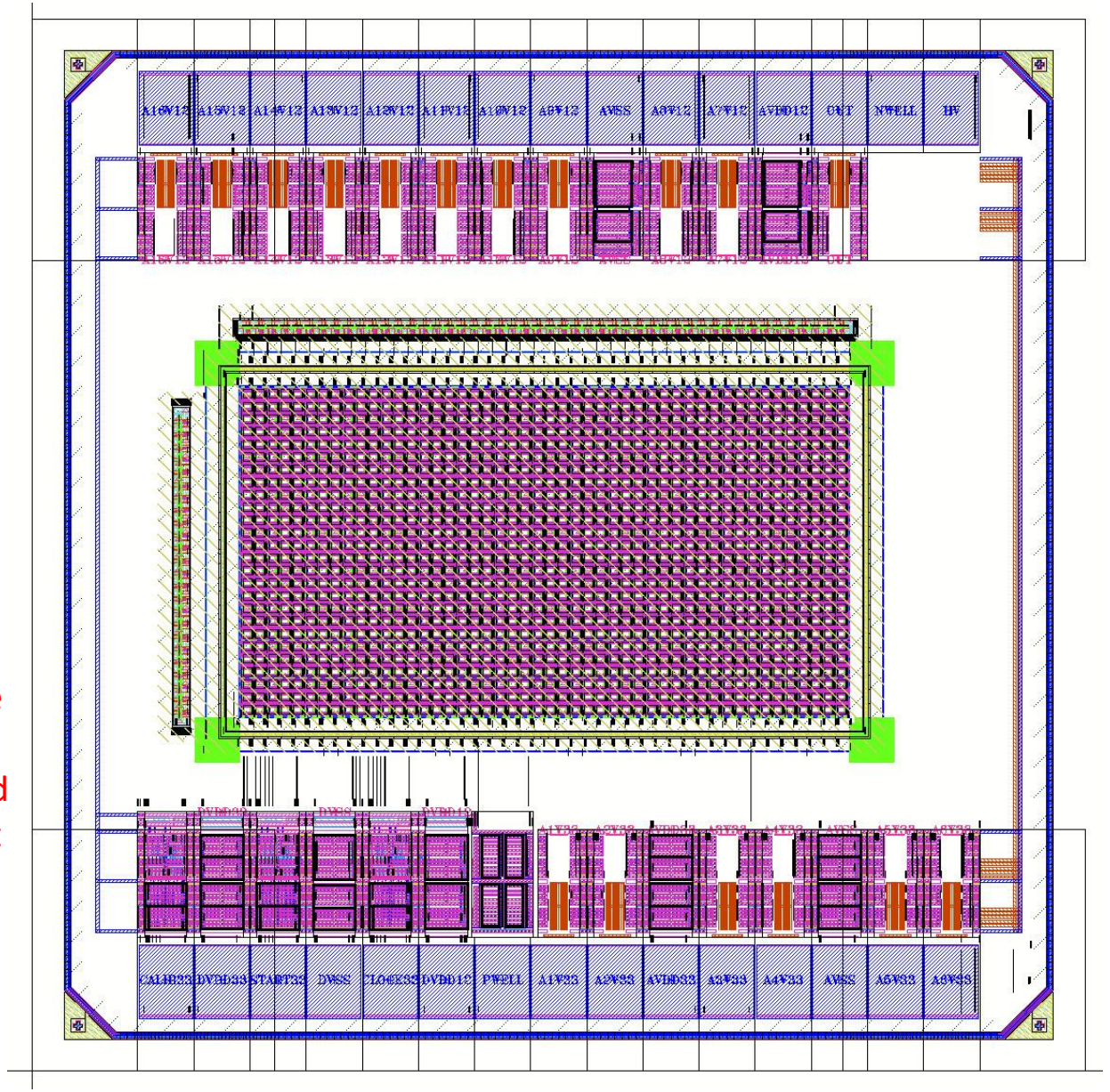
Likely we need one more pad: SUB (deep nwell around pad), previously it was connected to NWELL (nwell ring around matrix)

16 biases:

- 10 X 1.2 analogue biases

(to be compatible with MOSS/DPTS like FE)

- 6 x 3.3 analogue biases



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Different modifications/chips of CE65v2_xx

Modif.	Purpose	Pitch, um	Comment	N
CE65v2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (one best pixel from CE65 will be selected, preliminary test shown better S/N with in pixel amplifier)	(15*), 18, 22.5, 18_{hexsq}, 22.5_{hexsq} (22.5_{hex}**)	For lab and beam test, charge collection node, techno, optimization	4 (6)
CE65v2_A_xx	Precise measurements of multiplexed analogue or digital output of pixel FE ("_A_"): pulse duration, gain, FPN, noise, RTS..	18	For lab only, possibility to explore waveform with oscilloscope: FE optimization/tuning.	1 (existing FE from MOSS) + versions..
CE65v2_D_xx	Digital FE ("_D_"), matrix of pixels with digital storage -> digital clusters	18, 18_{hexsq}, 22.5, 22.5_{hexsq}	For lab and beam tests. Optimization of variants of digital FE + charge collection study. Redundant to MOSS/MOST/DPTS: so most likely, the design variants are restricted to the complimentary geometries, not implemented in large chips…	~4

* possible without calibration circuit due to small pitch

** "academic" study for exact hex layout

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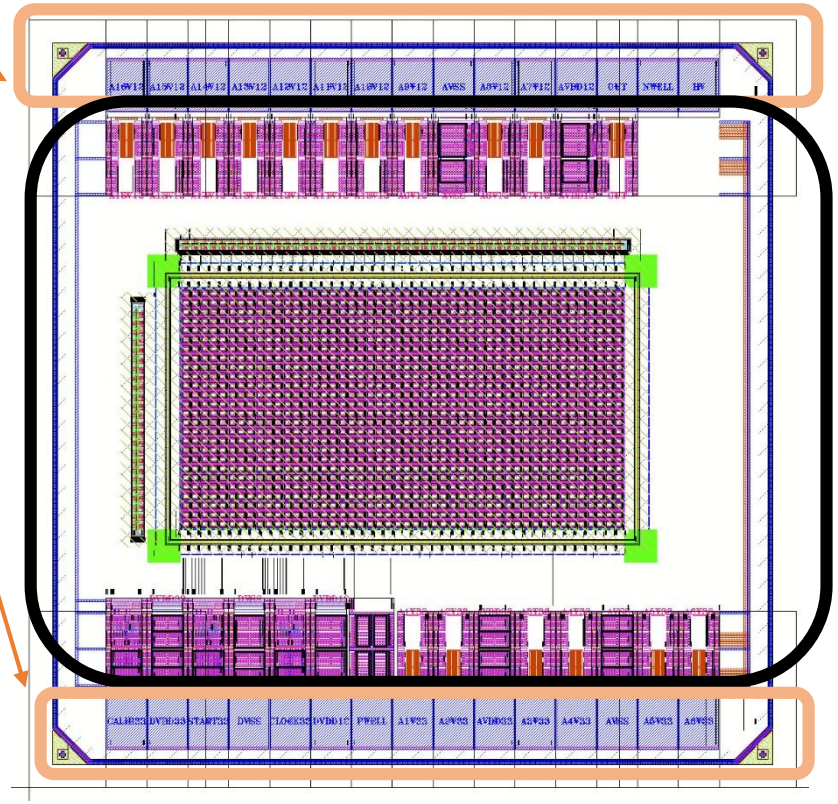
Design assumptions/requirements

1. Transistors used:
   - 3.3V MOS: MOS_NL, MOS_PL, MOS_NL_LS
   - 1.2V SLVt: MOS_NSL, MOS_PSL
2. Use standard PADS IO with 6M metal stack libraries, however :
   - Use blocks from new padring 6M stack for small chips(“CERN_CUSTOM_IO_CELLS_r1_2022_02_16”):
     - IO_PAD_ACNR_W100_ISC_W105_SS
     - IO_PAD_NP_W80_STACK_ISC_L105
     - SRG_SID_WCAP15_W10_NM65_4M_15um



CORE and PADS IO: 6M stack

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Status of design CE65v2: target to have one completed version (CE65v2_C) for mock submission

Block	Feature	Schematics	Layout	Comment
Pixel: sensing diode(AC) + FE for CE65v2_C_xx chips	18um and 22.5um	OK	OK	Will be reused for hex/hexsq
Digital cells	18um and 22.5um shift register cells	OK	OK	Row and column shift registers: Layout OK, schematics to be done will be reused for hex/hexsq designs
Memory	Only for CE65v2_Dxx modification	To be done(*)	To be done(*)	Can be analogue storage of digital…
Column periphery and analogue output buffer	18um 22.5um	OK, from mlr1	To be done	Common to all chips
Pixel matrix	18um and 22.5um	To be done	OK	Layout for hex and hexsq to be done(*)
PADs IO	Digital IO, analogue bias, power + unprotected (NWELL, PWELL, HV)	OK	Ongoing(01/03/22)	Adaptation/reuse of cells from padring: "CERN_CUSTOM_IO_CELLS_r1_2022_02_16"
Top level chip	18um and 22.5um	To be done	OK, global interconnection to be done	Layout for hex and hexsq to be done(*)

*** not needed for mock submission**

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