

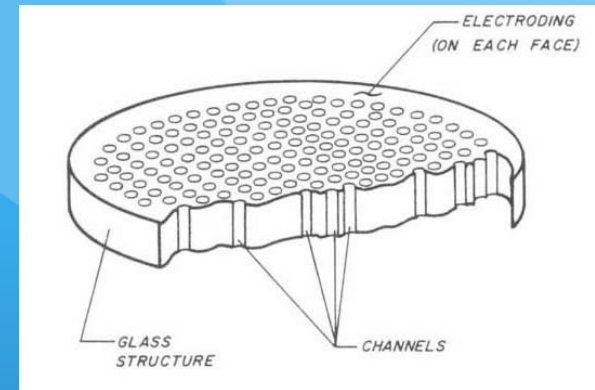
# PICMIC status

I.Laktineh

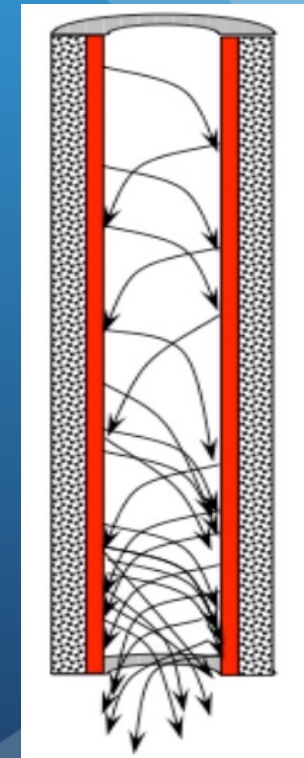
on behalf of the PICMIC groups

IP2I, IPHC, IJCLAB, CPP

# Micro Channel Plate (MCP)

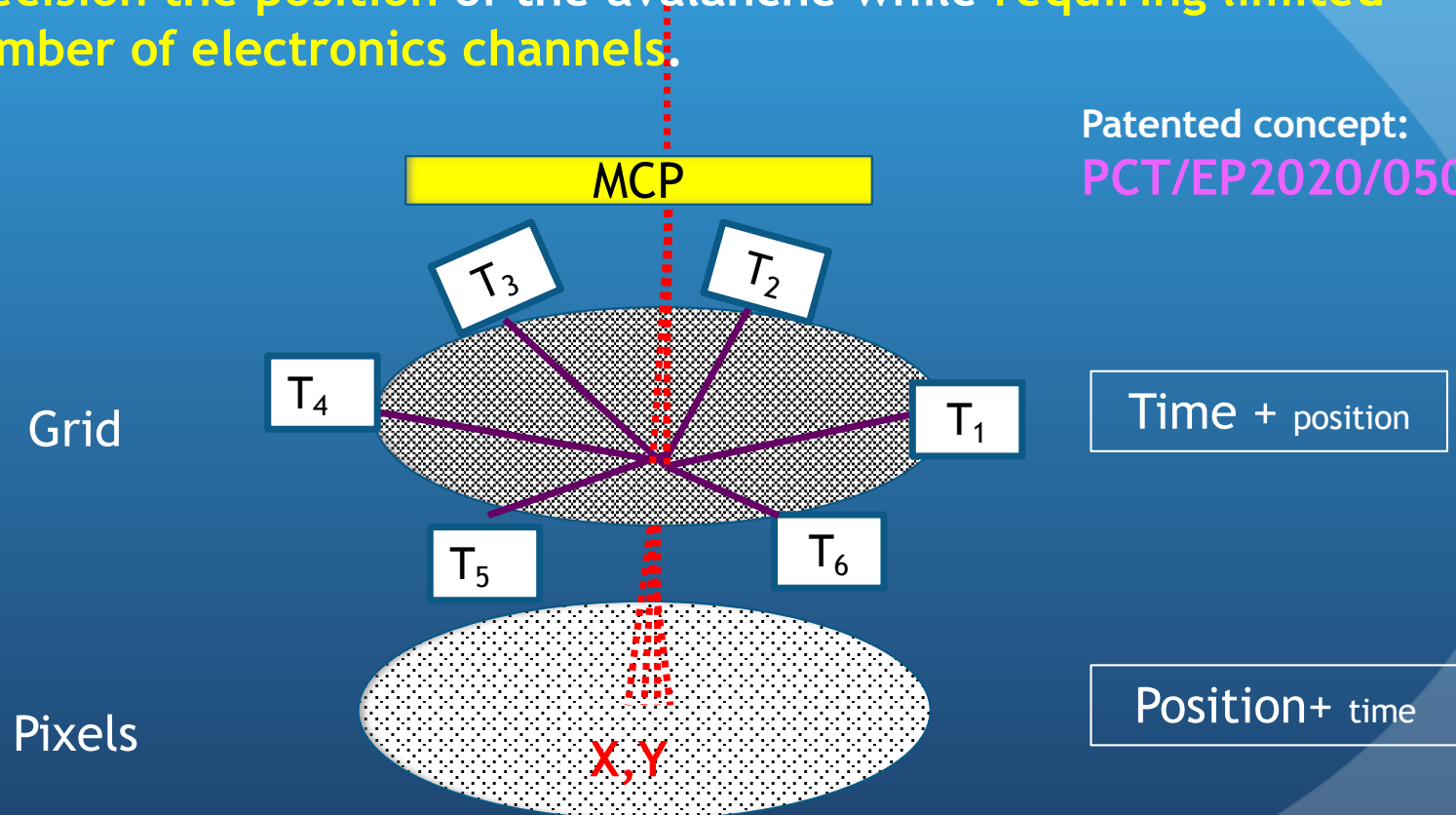


- MCP is considered as the best timing device with a few picoseconds of time resolution.
- Most often there are two plates with the channels oriented in a slightly tilted way (chevrons) to increase the gain and at the same time reduce the ion return impact.
- MCP has an excellent intrinsic spatial resolution since the avalanche produced by the incoming particle is constrained to one of the glass tube whose diameter can be as small as  $2\ \mu\text{m}$
- MCP are often used for their timing while their spatial resolution is not appropriately exploited.



To fully exploit MCP we propose the following scheme:

- ❑ A **transparent grid** placed downstream and read out by sensors with excellent **time resolution**
- ❑ A detection **matrix with micrometric pixels** to measure with great **precision the position** of the avalanche while **requiring limited number of electronics channels**.



Patented concept:

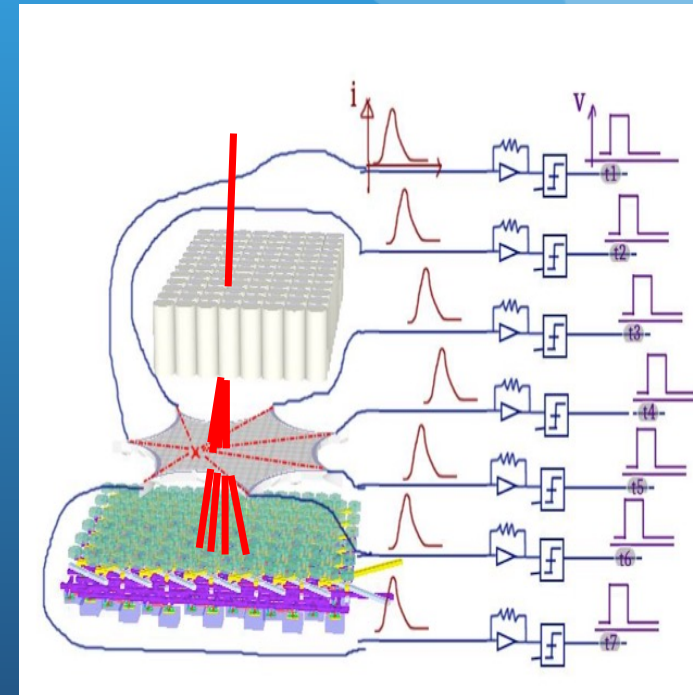
PCT/EP2020/050058

## Concept description

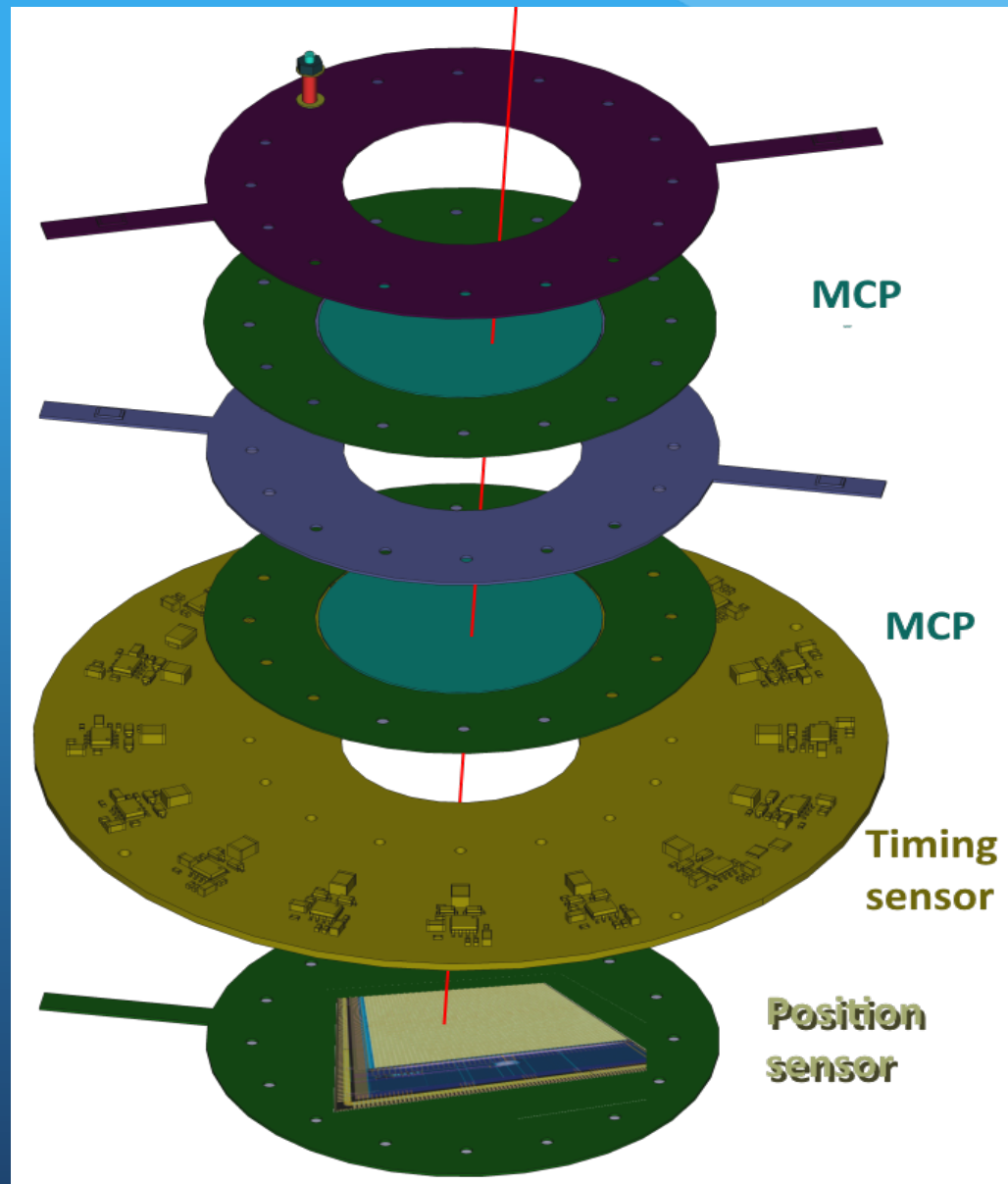
- The avalanche crosses a transparent grid connected on its periphery to a few timing sensors
- The avalanche is then collected by pixels

  - 1- Measure X,Y, from the fired woven strips by crossing them geometrically
  - 2- Measure  $T_i$  (from time sensors)
  - 3- Subtract time propagation using speed propagation and X-Y)
  - 4- average on the  $(T_i - T_i(\text{propag}))$

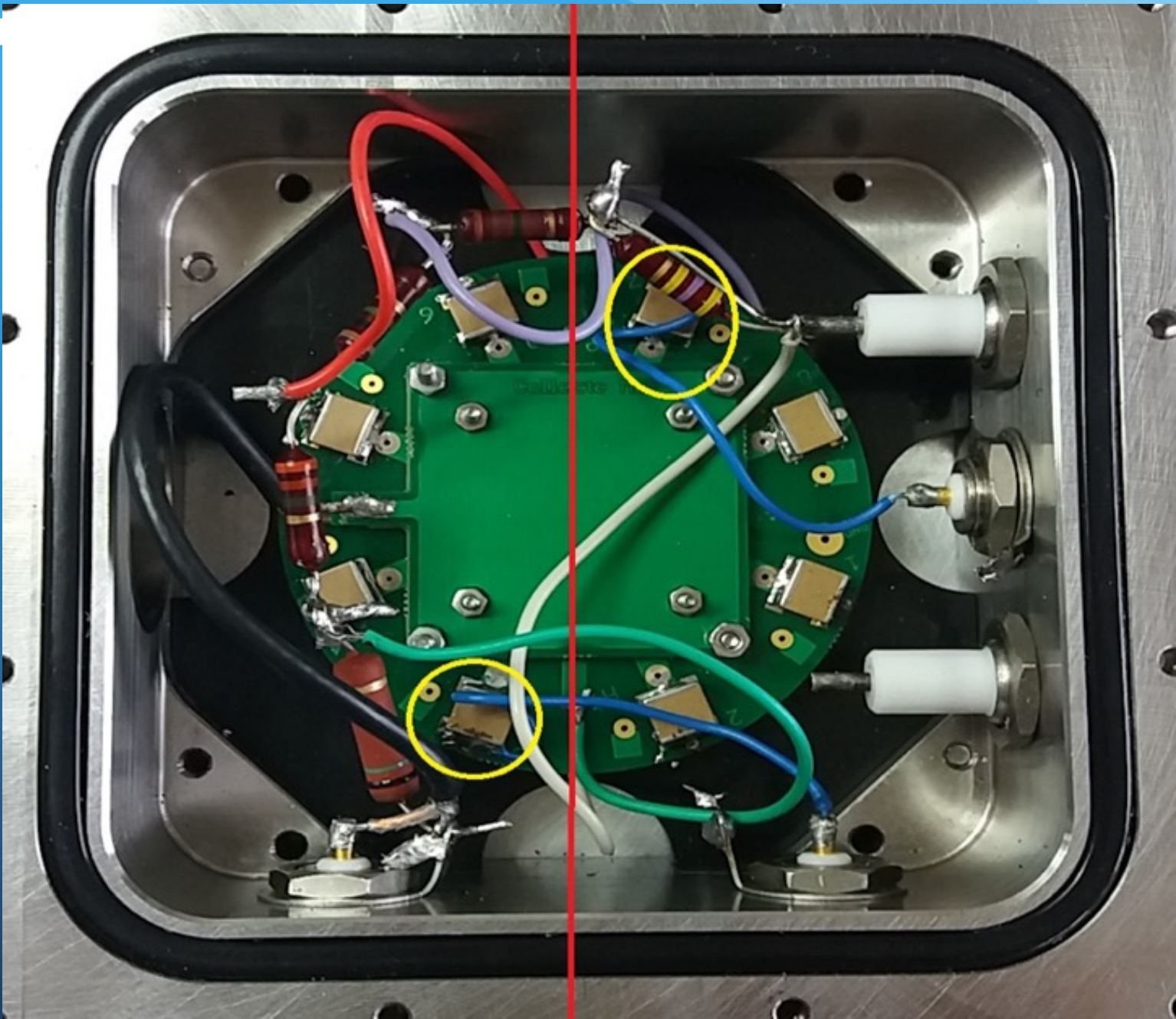
$$T_{\text{abs}} = \frac{\sum_0^N T_i - T_{i-\text{propag}}}{N}$$





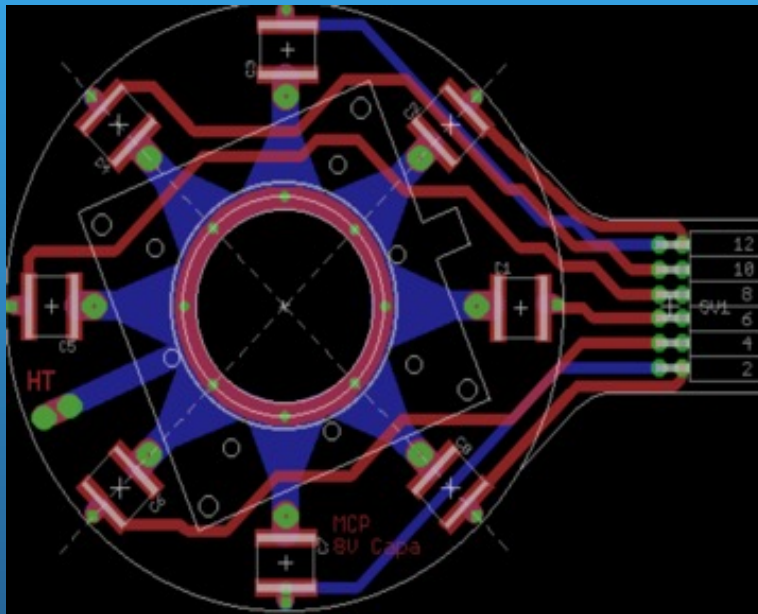


Cu



# Time Measurement

Principle components for this measurement already exist.



8-point PCB for the time measurement.

PCB to be in contact with the grid (already produced and tested)



SAMPIC: TDC ASIC allowing to reach 3 ps time resolution



**SAMPIC WAVEFORM-TDC Software V3.3.4**

Interface Configuration Run Graph Firmware Special

MAIN VERTICAL HORIZONTAL TRIGGER TOT

**External Trigger**

Level Use Ext Trig as Enable Trig

Software TTL NIM Open Gate on Ext Trig

Internal Osc Edge Ext Trig Gate 80 ns

External Signal Edge Ext Trig Gate 80 ns

**Advanced Trigger Options**

Channel Trigger Mode

Self Trigger

External Trigger

Central Trigger

Chained to previous Channel

Internal Threshold (relative to Baseline)

-0.180 0.220

-0.380 0.620

-0.580 0.820

-0.780 1.020

Edge 0.140

**Central Trigger Parameters** : ALL SAMPICs

Central Trigger Type Central Trigger Effect:

Central OR Or if participating to CT  Trig All Channels

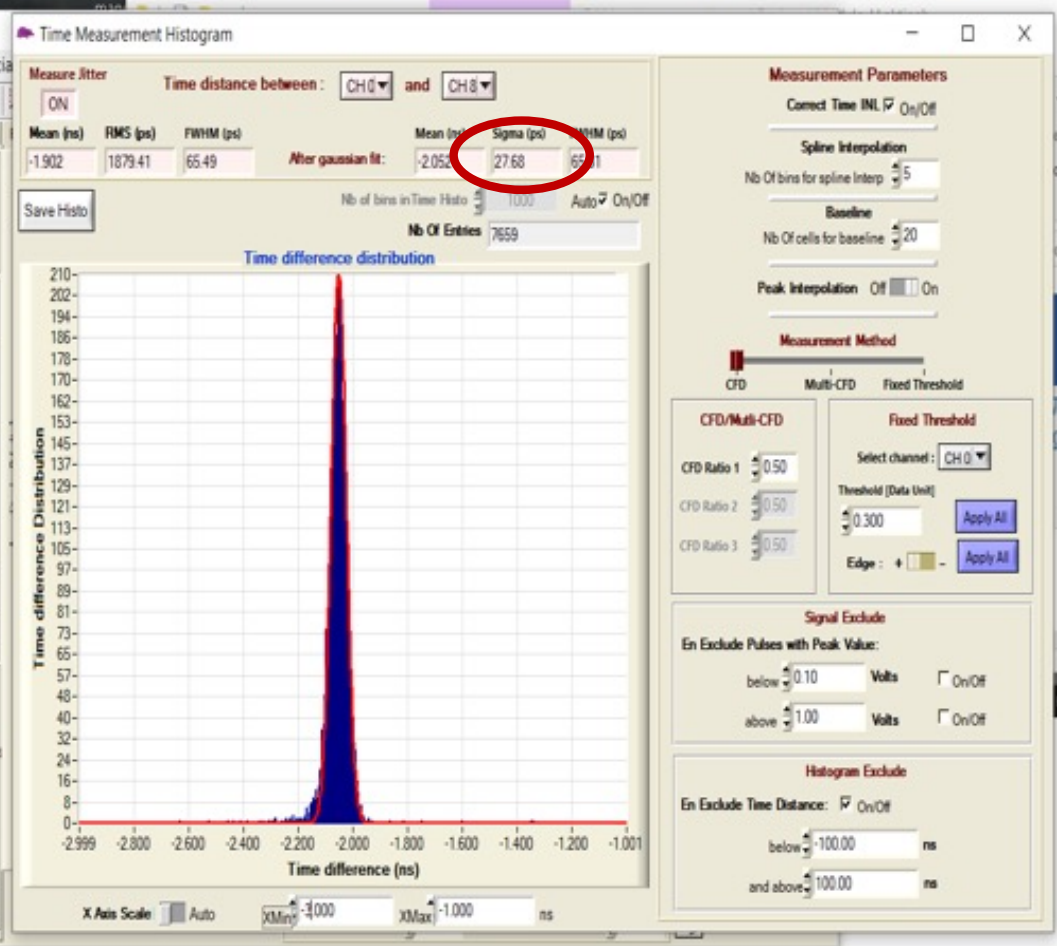
Triggered CHs > 2 Primitive Source:

Triggered CHs > 3 Raw Discn  Gated Discn

Channels Primitives Gate Length: 2 x 1/8 Clk Period 0.00 ns

Central Trigger Channel Sources : All channels

Ch0 Ch1 Ch2 Ch3 Ch4 Ch5 Ch6 Ch7 Ch8 Ch9 Ch10 Ch11 Ch12 Ch13 Ch14 Ch15



Sélectionner tout

Aucun

Inverser la sélection

Sélectionner

chercher dans : Module\_La...

Connexion Partager

Équation

Symbole

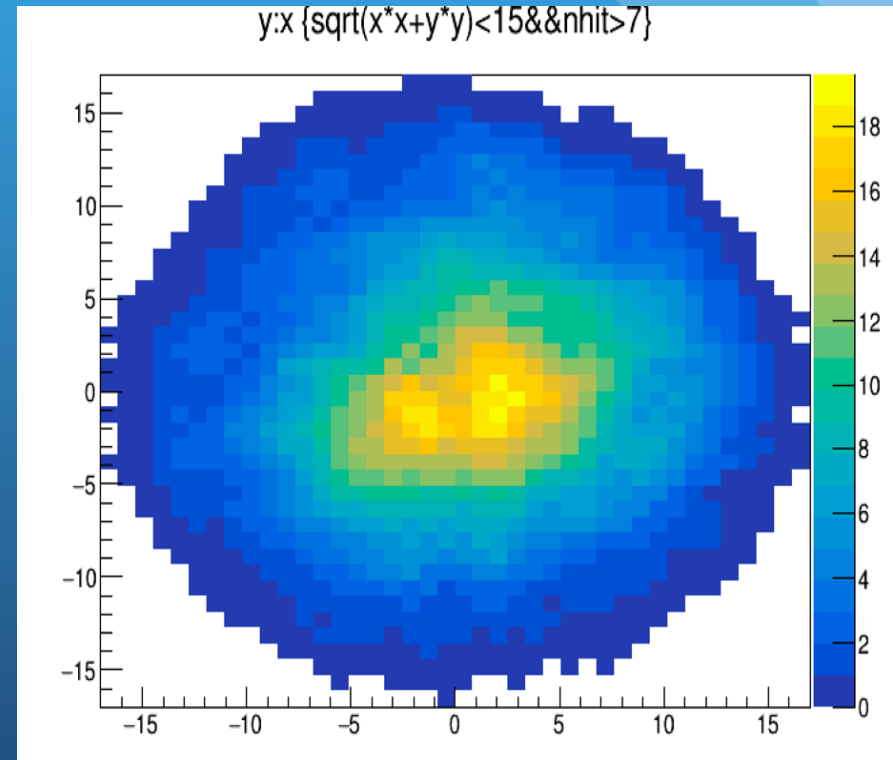
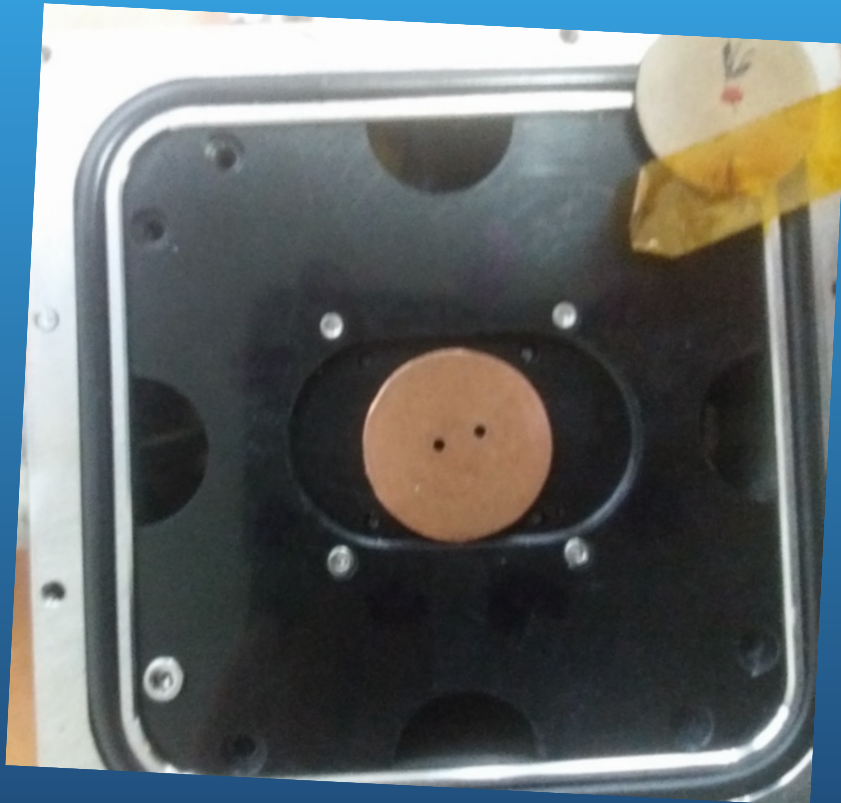
Symboles

170 %

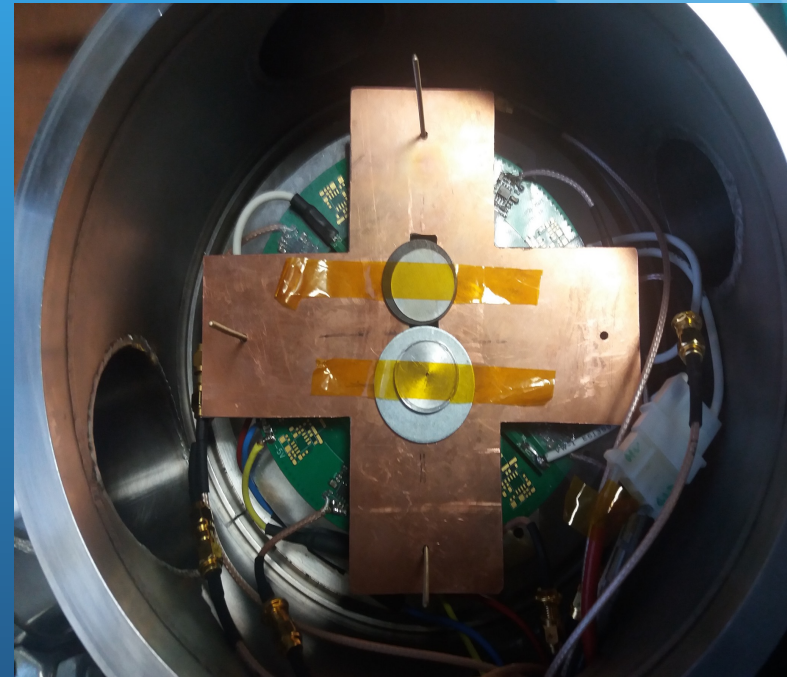
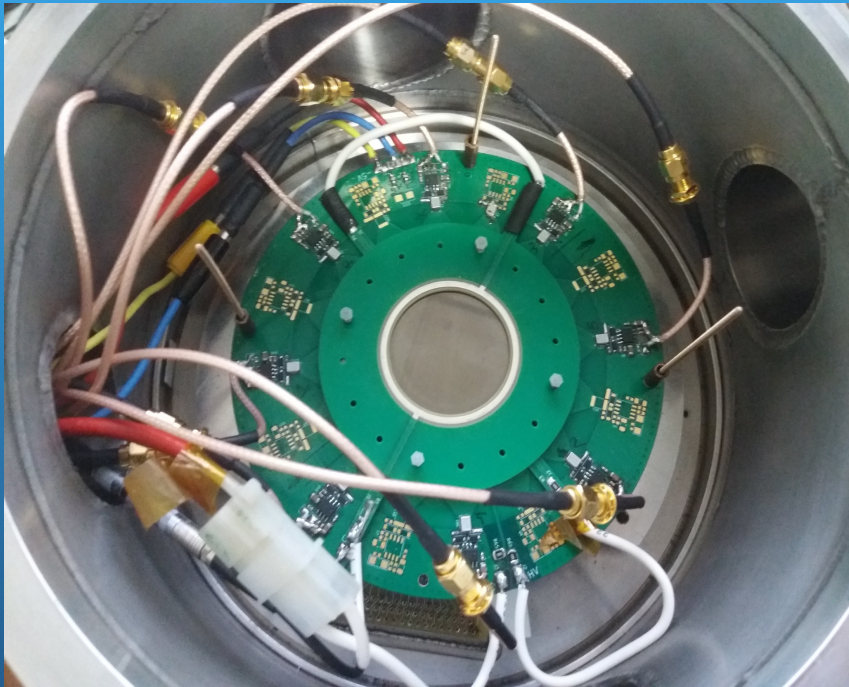
FRA 17:11

$\Delta T$

Waiting to have the pixel matrix, two algorithms using the difference of time arrival among the different channels were developed to obtain the position of the hitting particle → a new concept: delay plane



- A new timing PCB equipped with 16 channels was conceived and produced
- A new setup thanks to R. Barbier is used to host this large PCB

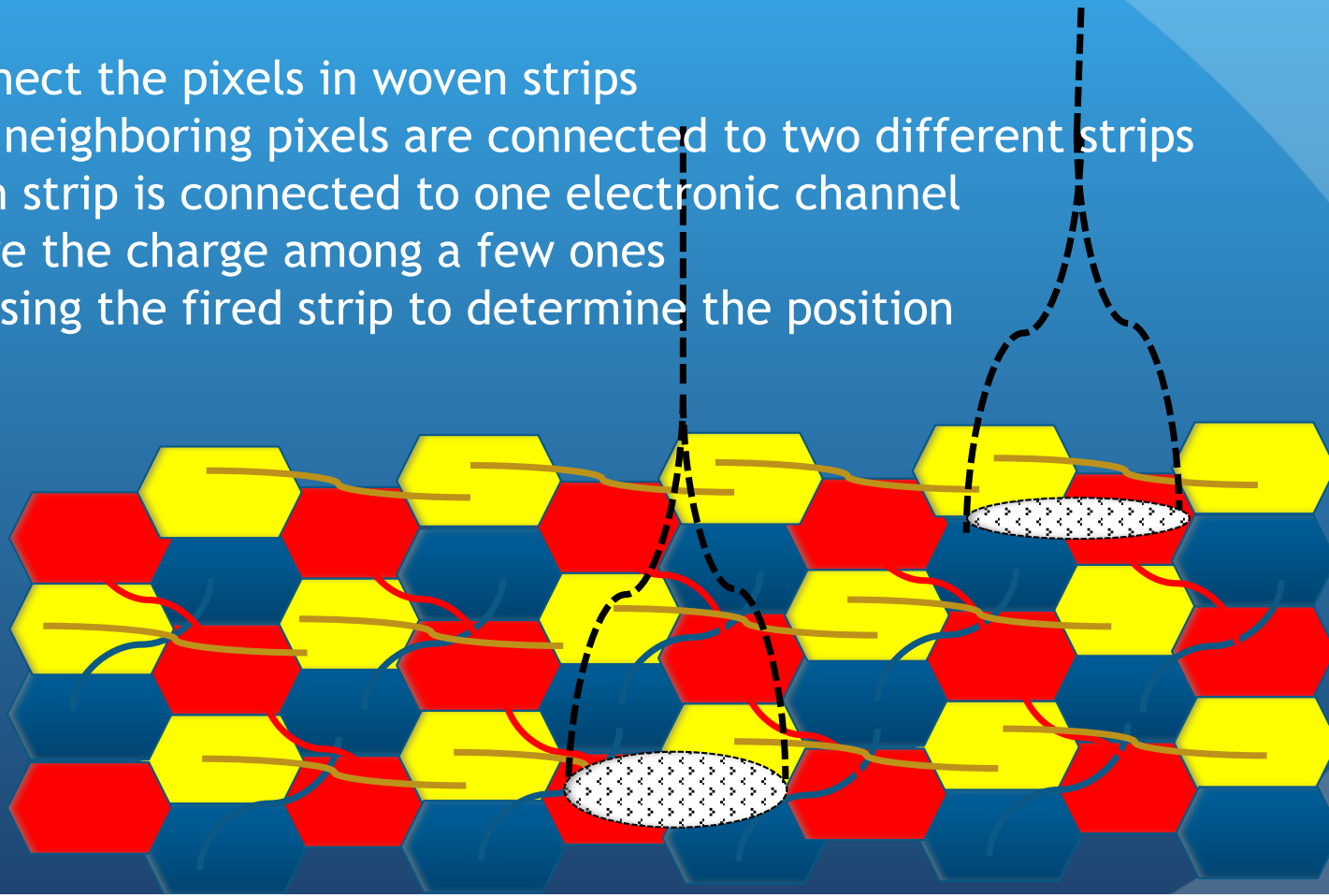




## Position measurement

To reach few microns resolution with a limited number of electronic channels, a genuine concept was developed, successfully tested and patented.

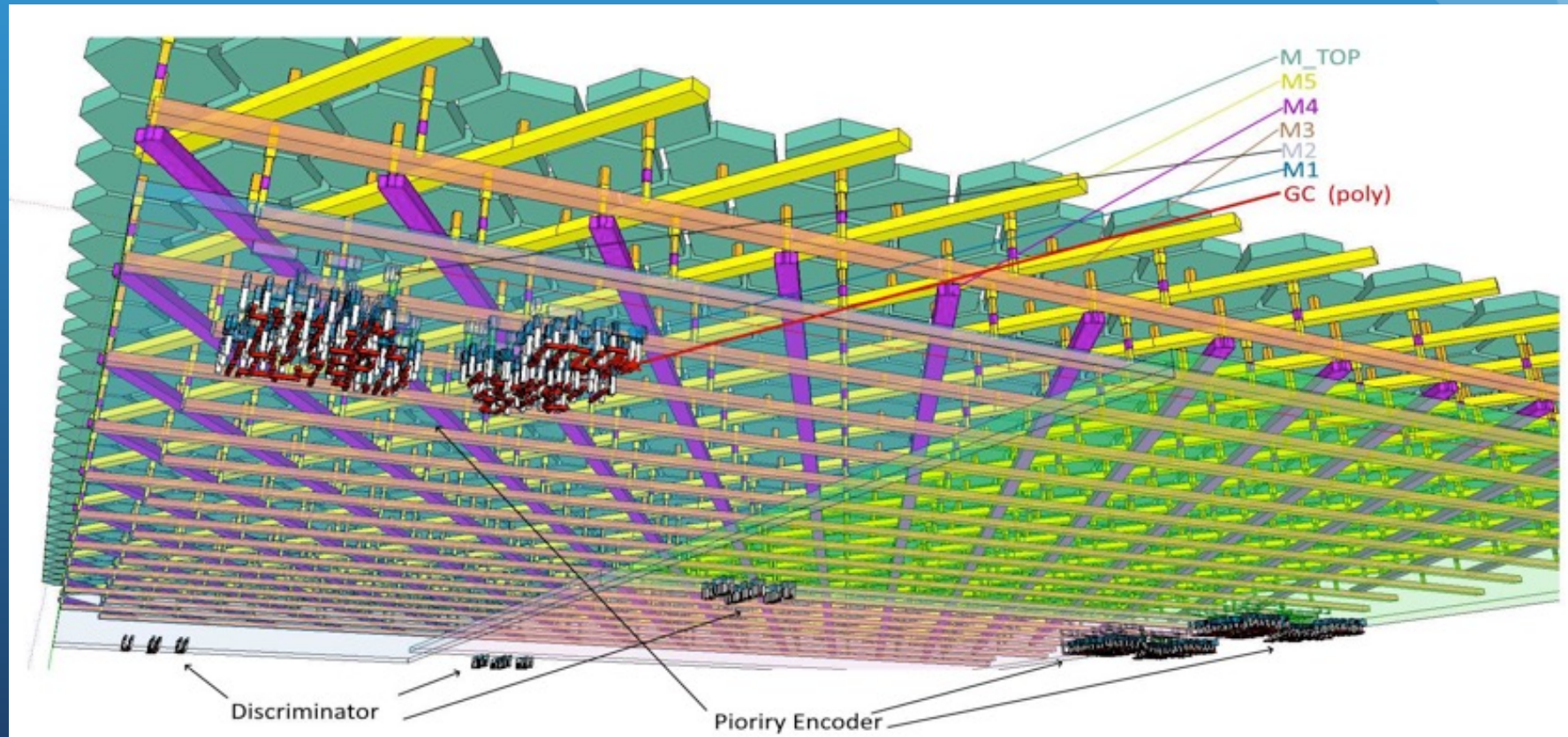
- ❑ Connect the pixels in woven strips
- ❑ Two neighboring pixels are connected to two different strips
- ❑ Each strip is connected to one electronic channel
- ❑ Share the charge among a few ones
- ❑ Crossing the fired strip to determine the position



$N \times N \rightarrow 3N$  : Reduction of electronic channels, power consumption and occupancy

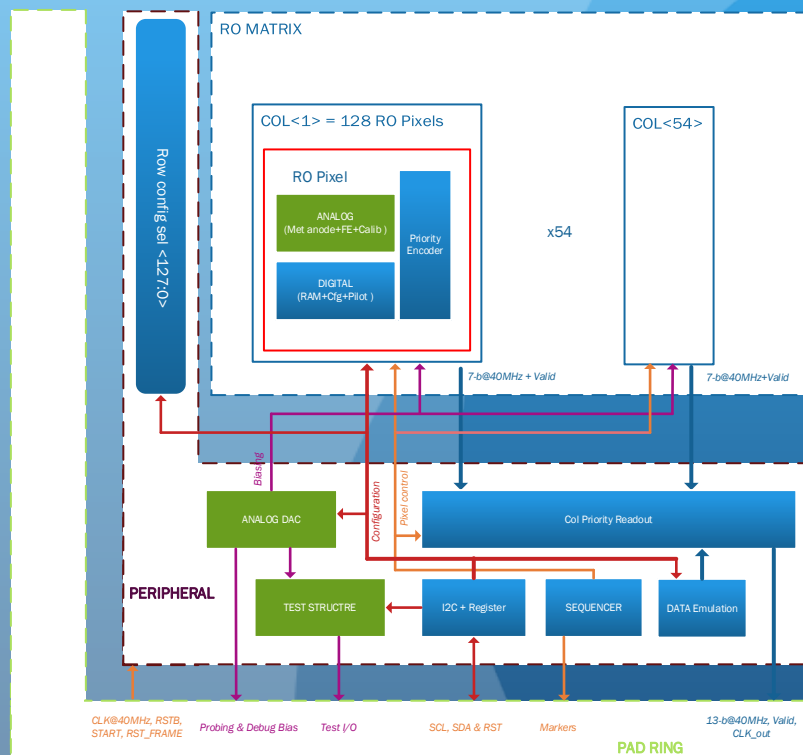
# Position Measurement

Exploiting the expertise IN2P3 in  $\mu$ electronics, we propose to read out the connected pixels by CMOS discriminators in TJ 180 nm (6 metal layers) technology.





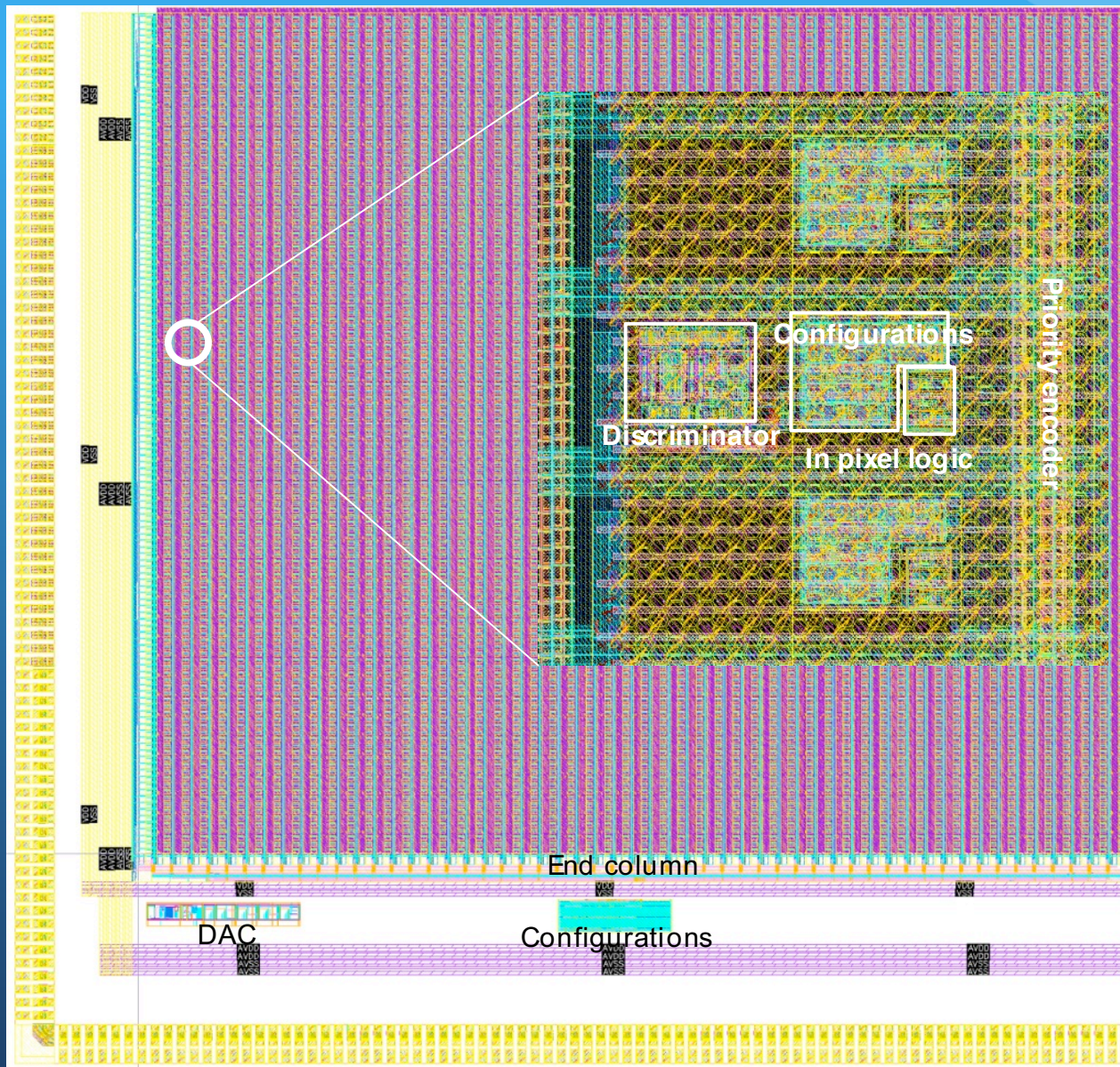
# PICMIC Architecture



Priority Encoder

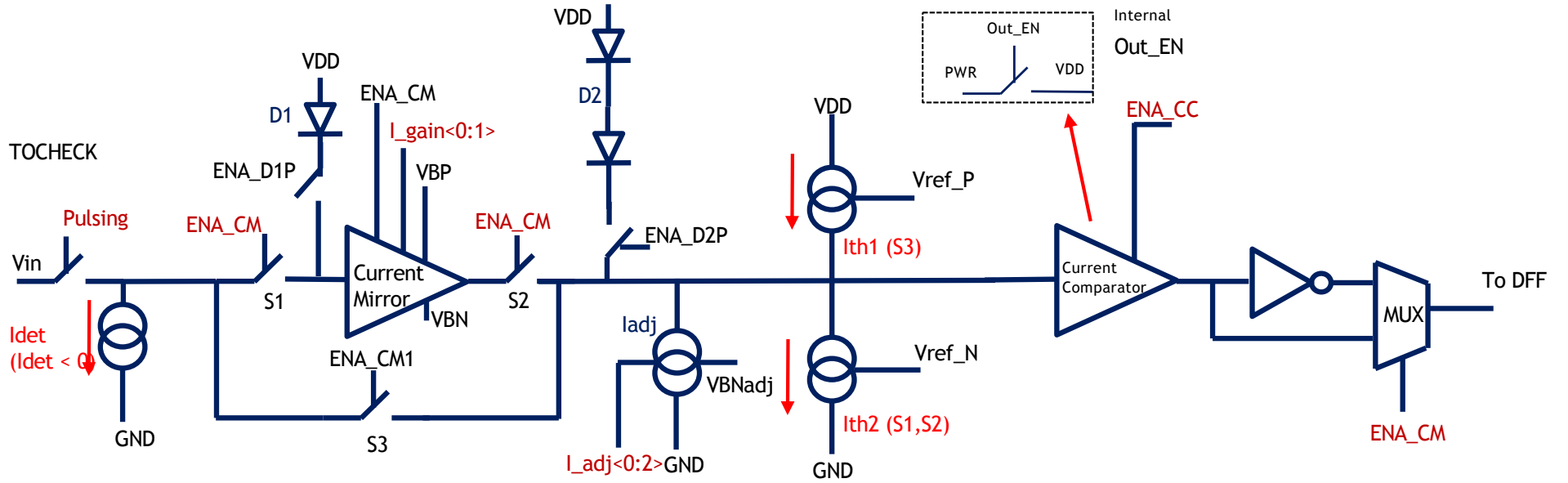
Parameters	Value
Design Flow	Cadence DoT flow
Technology	TJ CIS 180nm
Power supplies	1.8V
Power density	>172mW/cm <sup>2</sup> (only analog static current)
Die dimension	~7.5x7.5 mm <sup>2</sup> (6.5x7.5mm <sup>2</sup> active)
Anode dimension	~22μ <sup>2</sup> (5μm hexagonal pitch)
Readout pixel dimension	50μm x 140μm
Readout matrix	128x54 cells (only 2556 active)
Input clock	40MHz
Read-out port	13-bit parallel, 1 sync clock out, 1 marker (programmable 1clk cycle resolution)
I/O Pad	CMOS
Slow control	I2C
Max data rate (1Mhz hit rate)	390Mbps

# PICMIC Layout

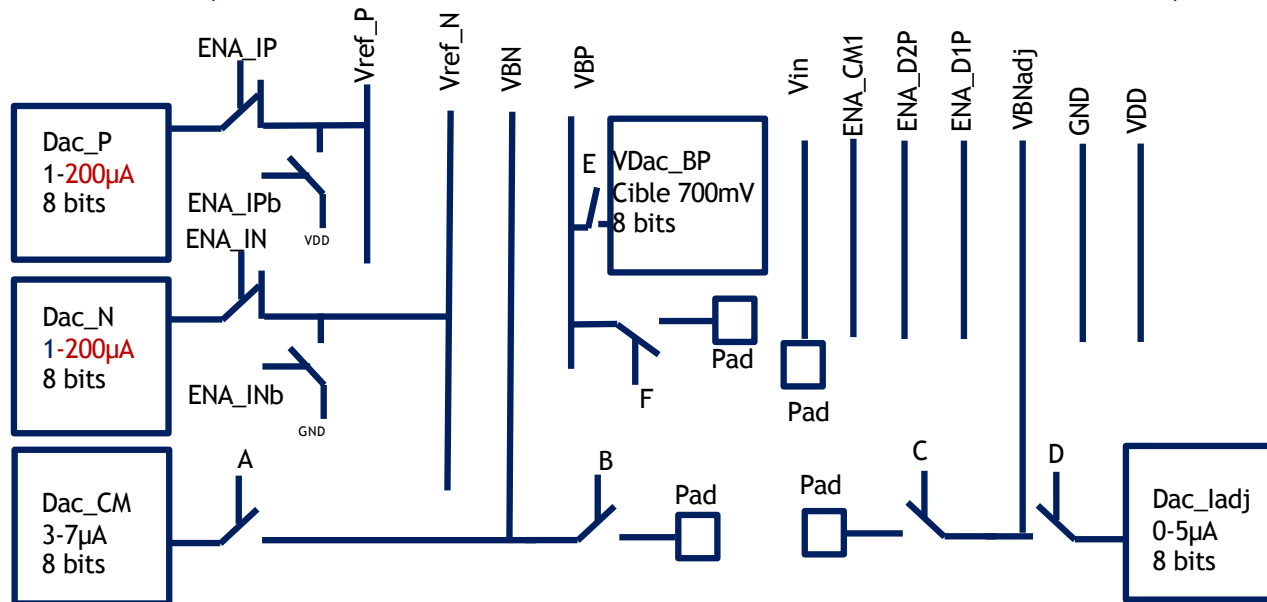


- Only 2556 RO cells are active among the 6912
- The active RO cells are placed in a way to improve heating dissipation
- The 2556 RO cells allow reading out the 2 216 000 pixels

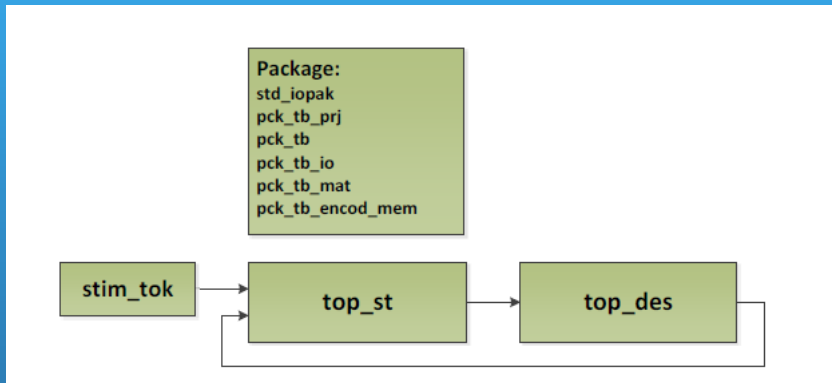
## Front End lock



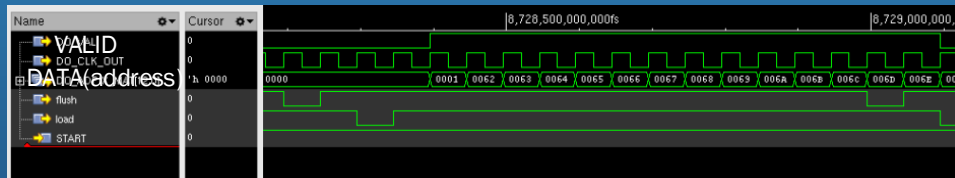
Column lines



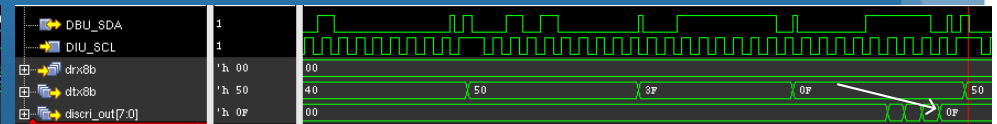
# PICMIC Simulation (Digital Matrix + Peripheral)



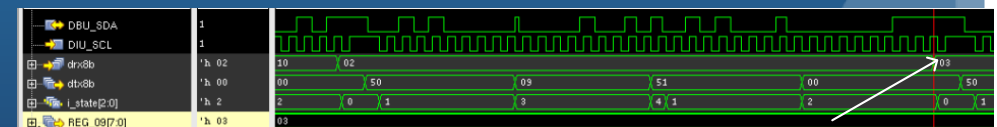
- ❑ The simulation validates:
  - ❑ I2C Register R & W
  - ❑ Analog matrix output by different hit patterns
  - ❑ Output data stream with CTS



Output data stream



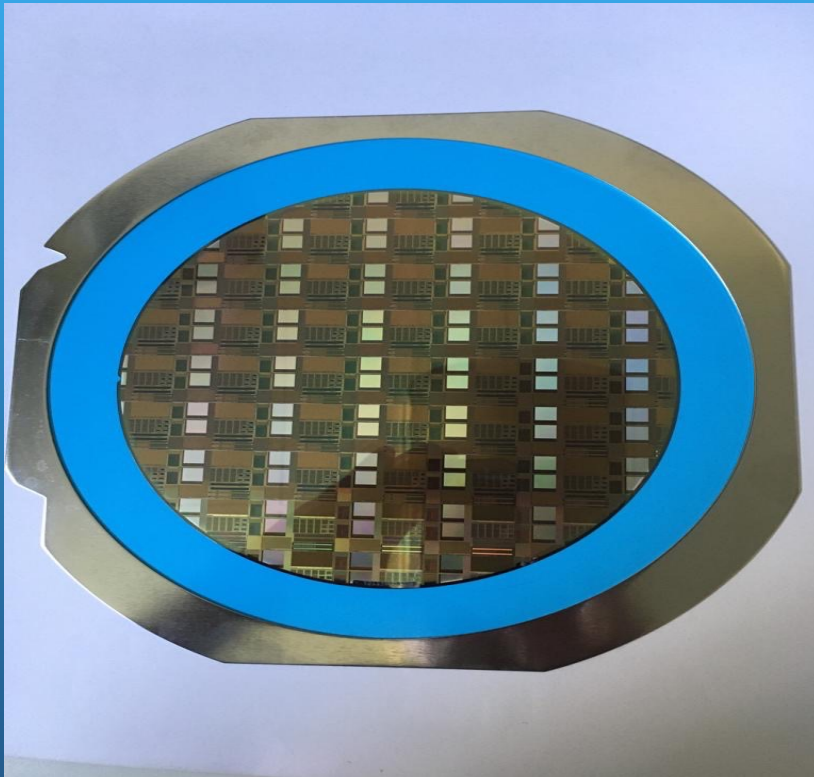
Write Configuration Registers



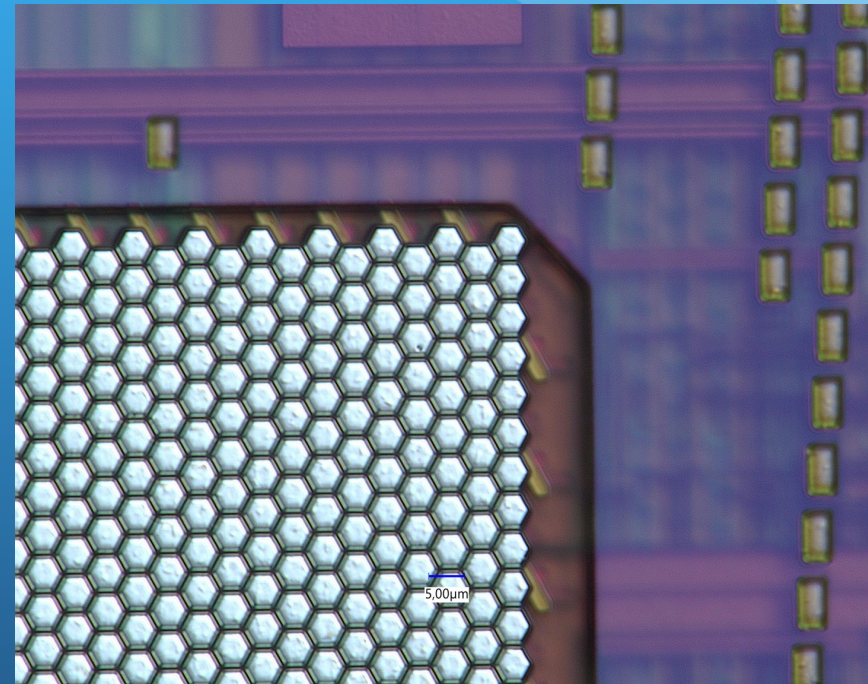
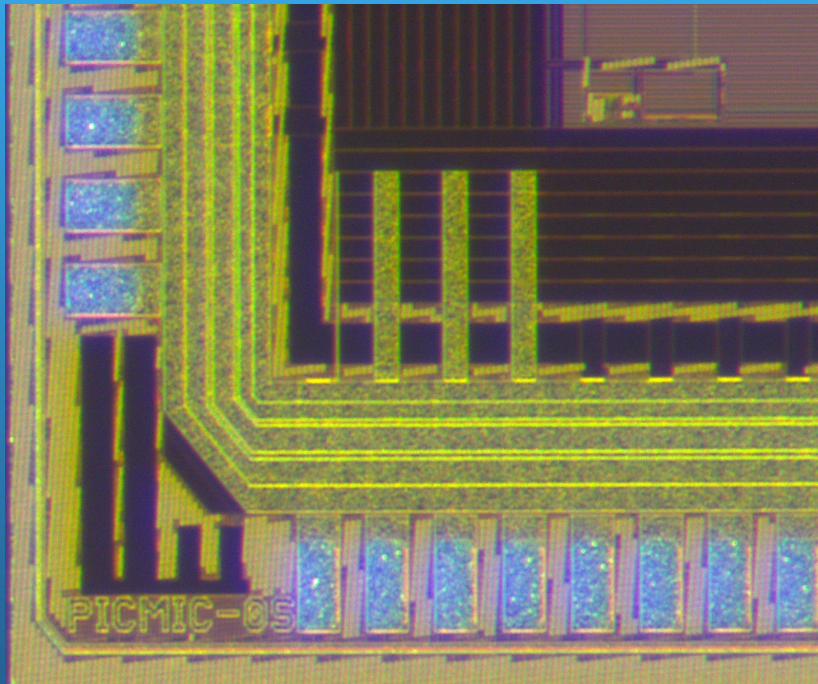
Read Configuration Registers



The chip was submitted in November 2021 (TowerJazz) and received on July 2022

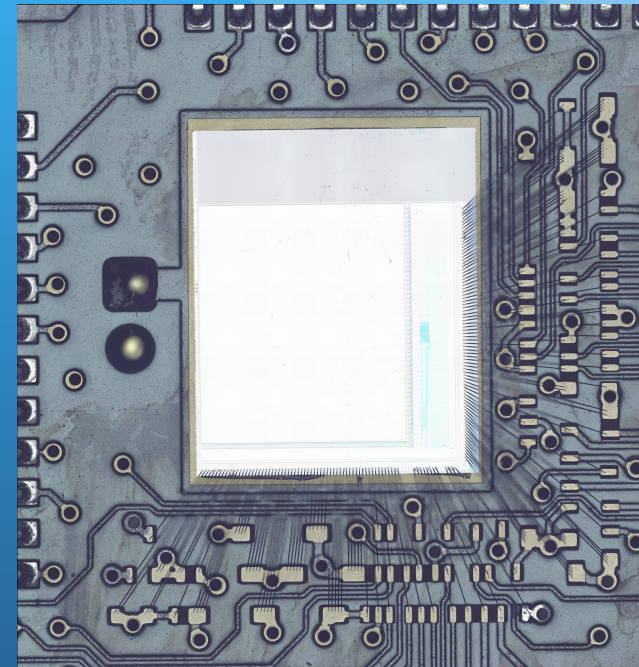
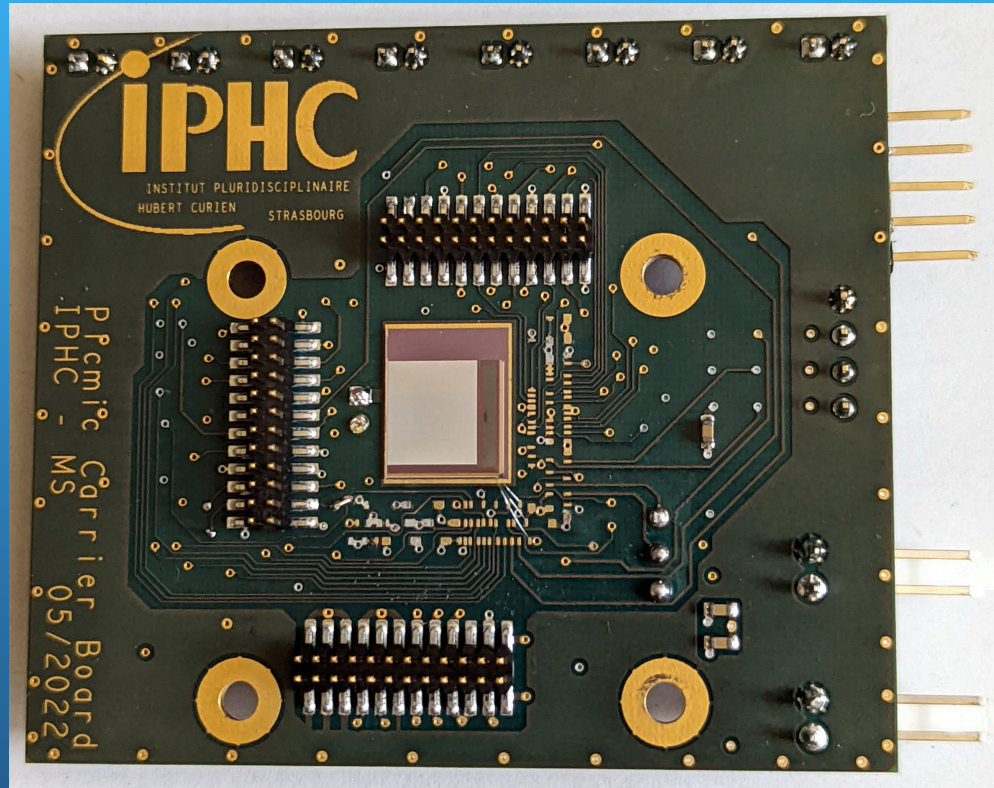


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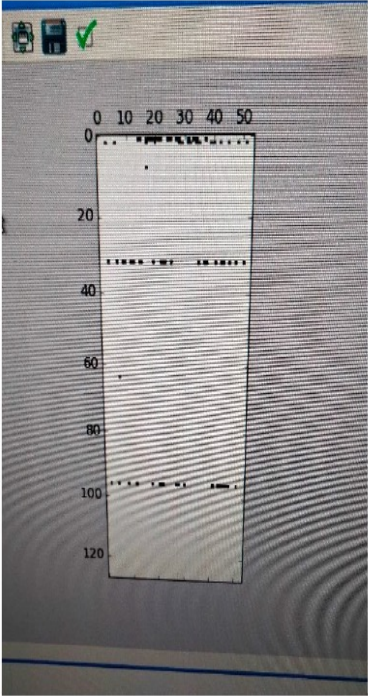


Tests were carefully prepared by IPHC electronics team.

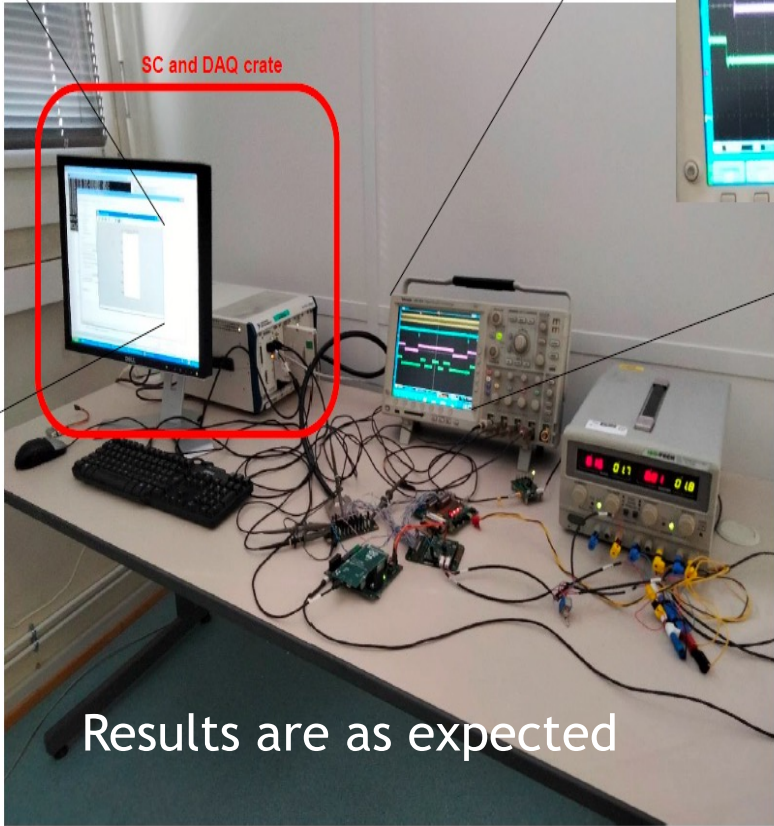


A system used for other application was adapted to test PICMIC chip

# Digital test bench

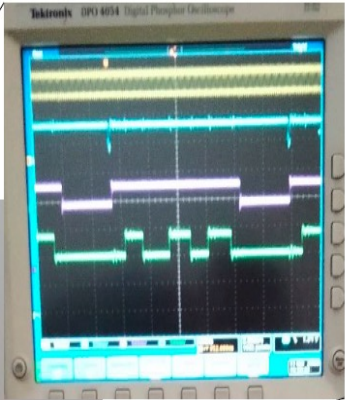


Pulsing pattern applied to picmic

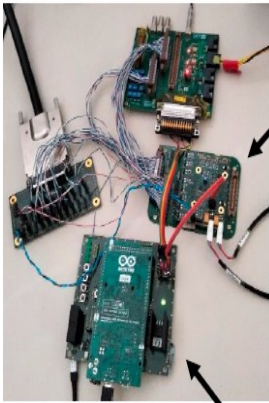


Results are as expected

Readout from picmic



Clk  
Marker  
Valid  
Data

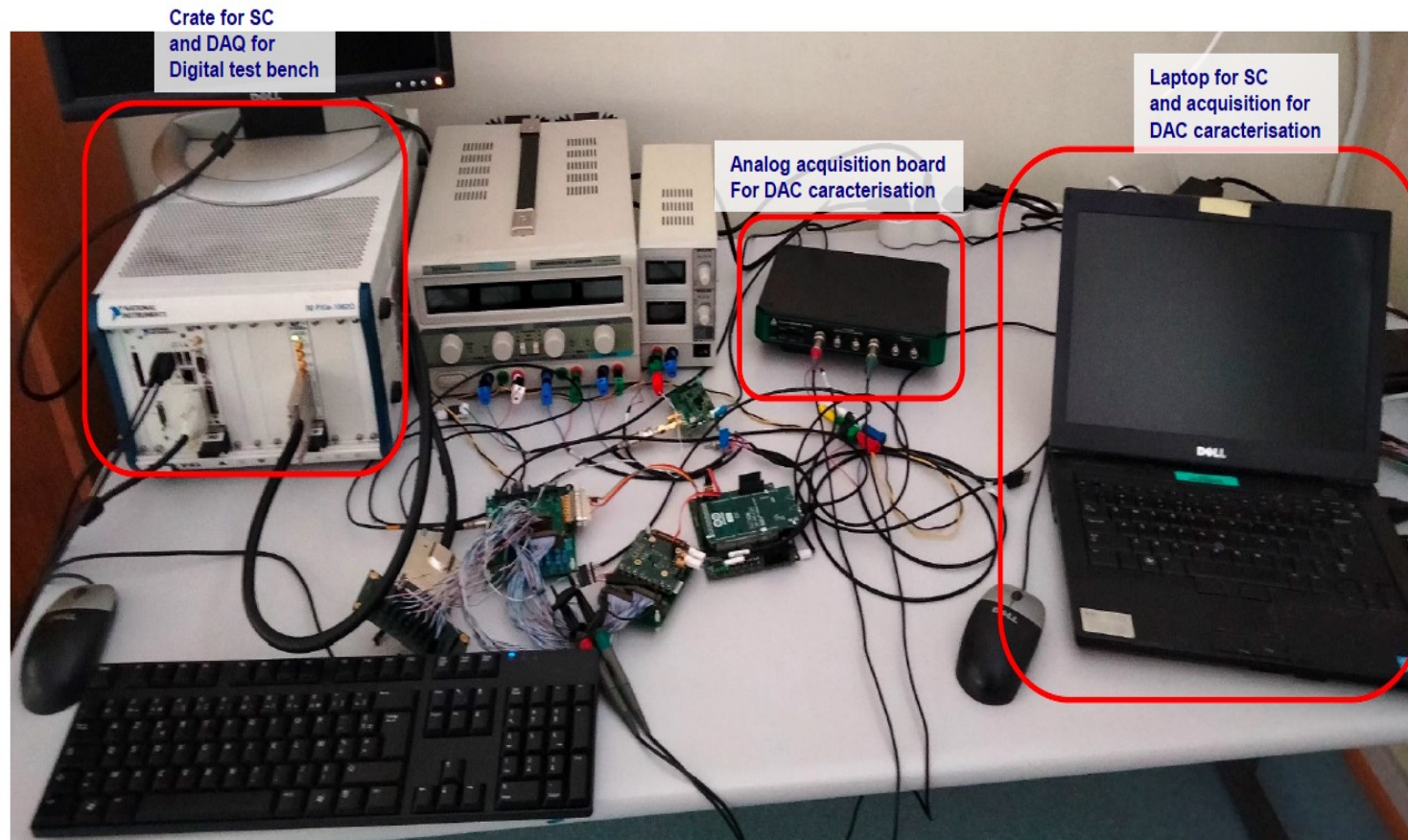


Picmic on  
Carrier board

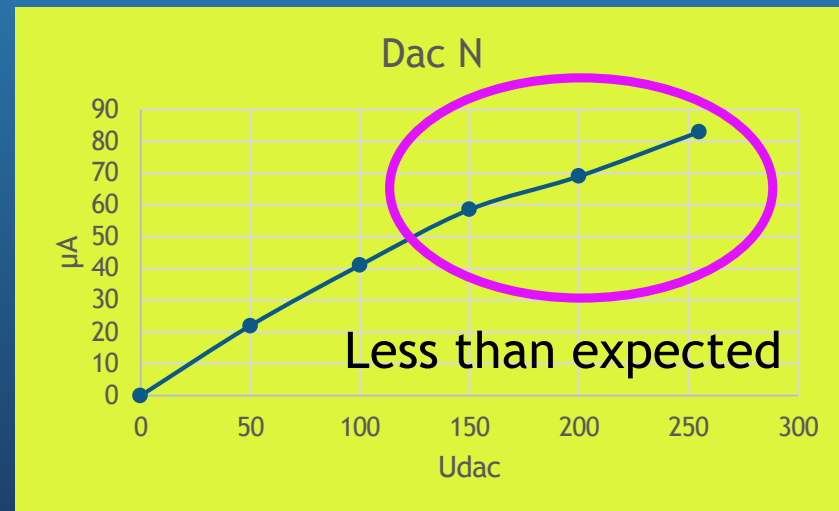
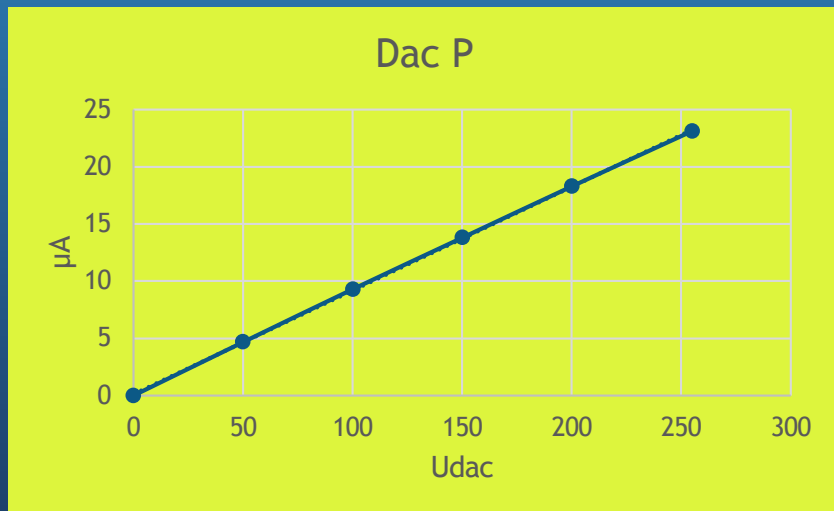
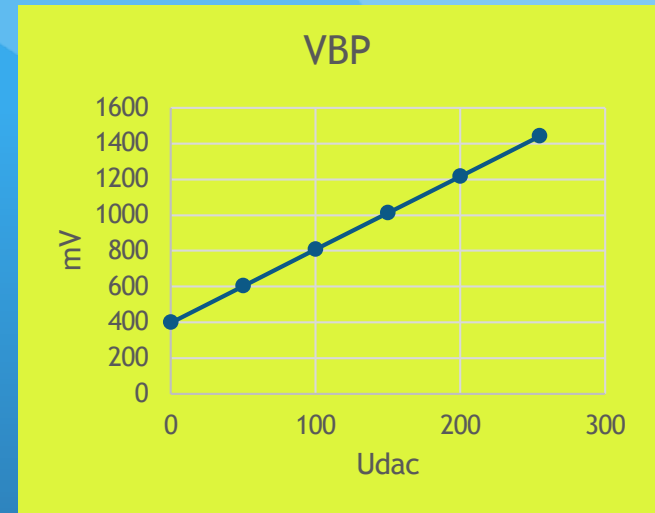
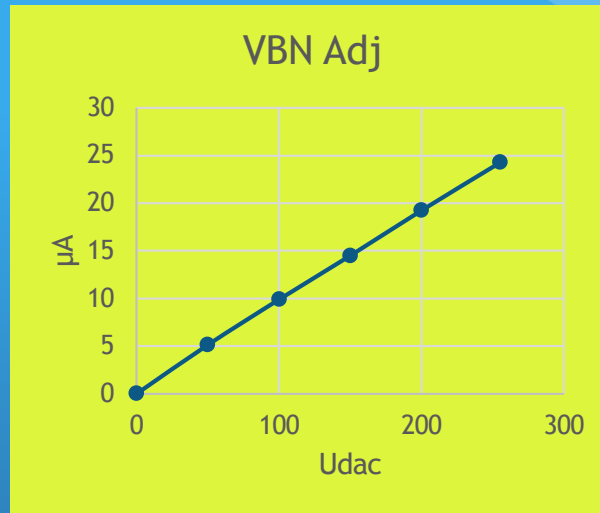
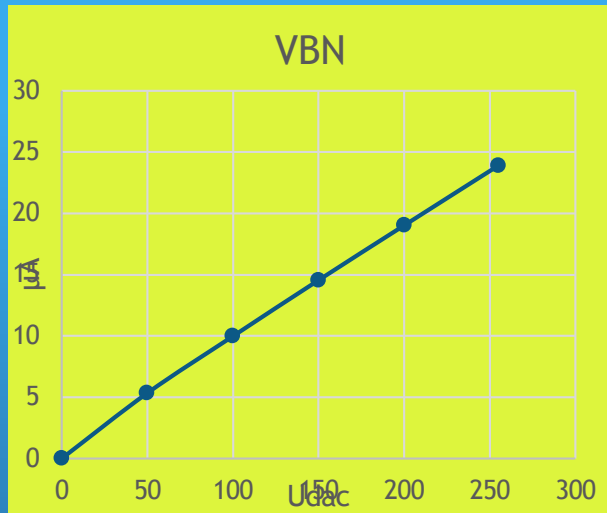
Slow control board



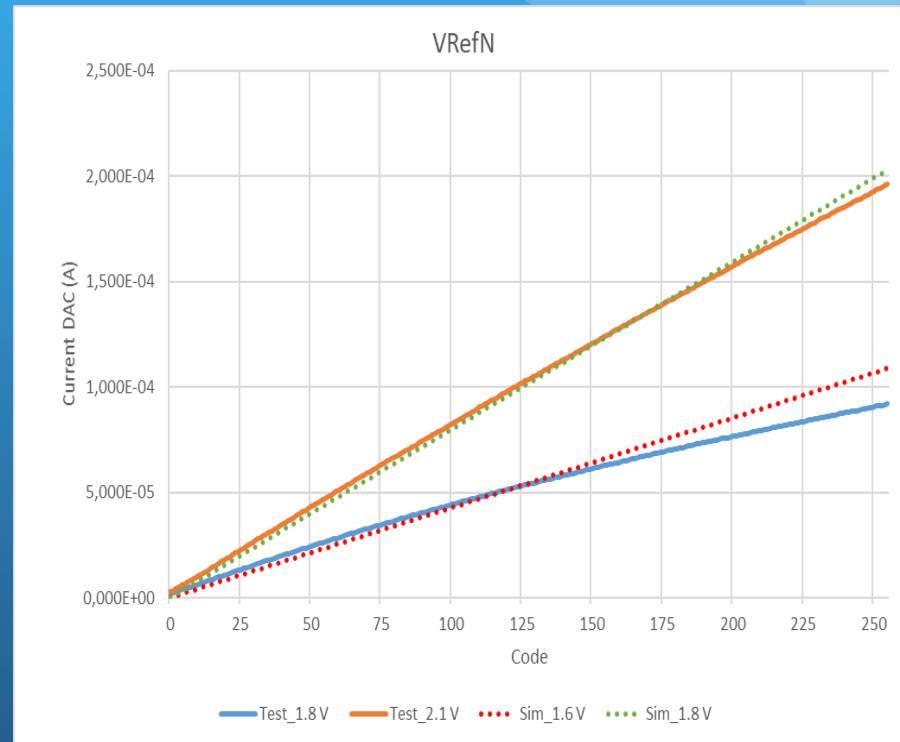
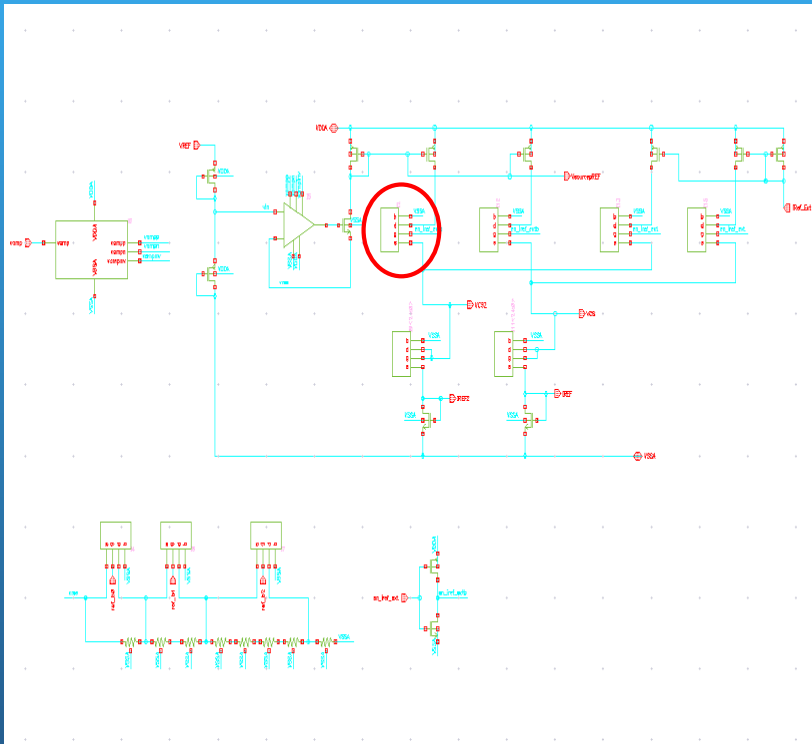
# Digital and DAC characterization test bench



# DAC measurements



## Problem understood and a solution found

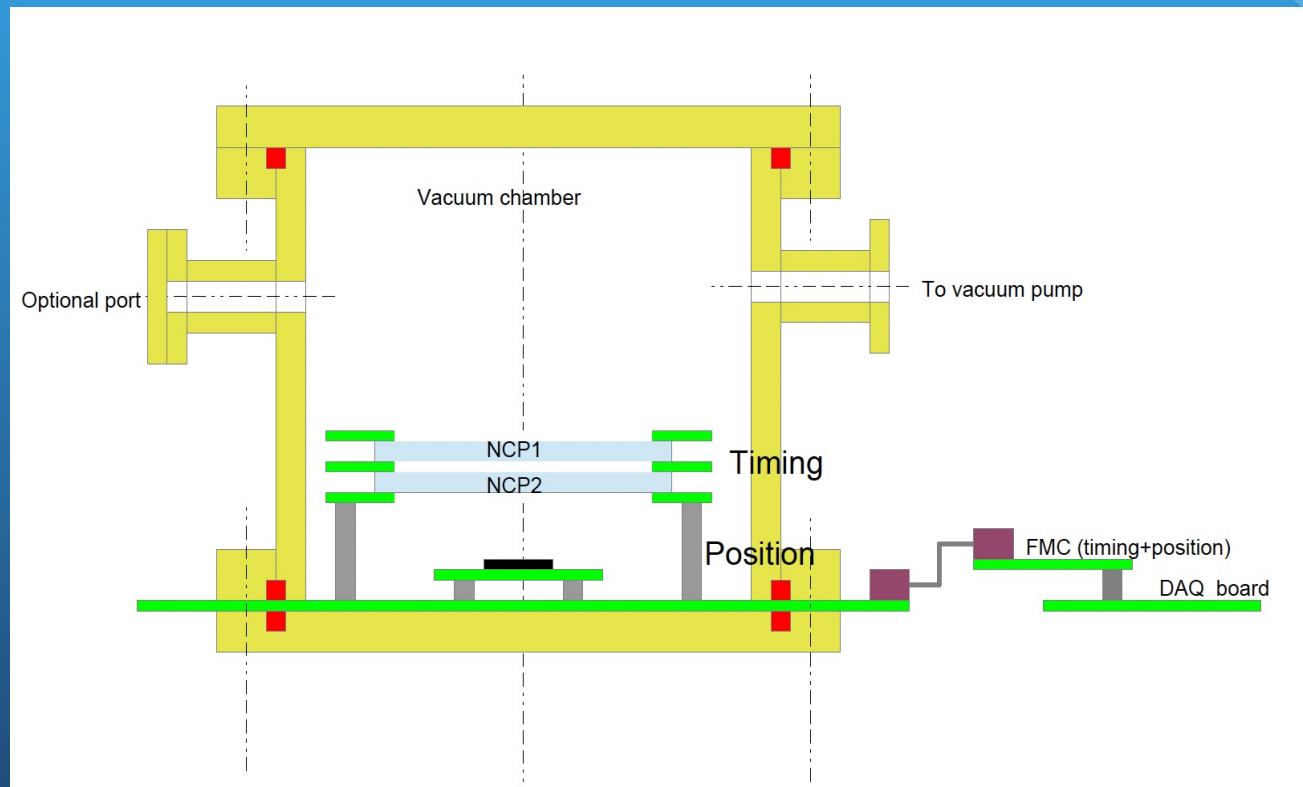


Either increase the VDD from 1.6 to 2 V or use an external DAQ

Next step is to test the sensor using charge injection

# Towards the first PICMIC demonstrator

The position sensors are being validated, we envisage to build our first prototype



# Towards the first PICMIC demonstrator

The position sensors are being validated, a new board to host the sensor is being designed by IP2I. The design and realization of the first prototype has started.

The first version will use SAMPIC module to

- 1) Measure the time information from the 8 (16) sensors as in the present scheme.
- 2) To distribute the same clock (40 MHz) to both the timing and position chips
- 3) To collect data from both and associate them.

The two last will need a card that be developed By IJCLAB colleagues and placed within the SAMPIC module.

The protocol has been agreed upon among IJCLAB, IPHC and IP2I and the design will start soon



# Next step

SAMPIC is an excellent tool but has dead time of about 1  $\mu\text{s}$ .

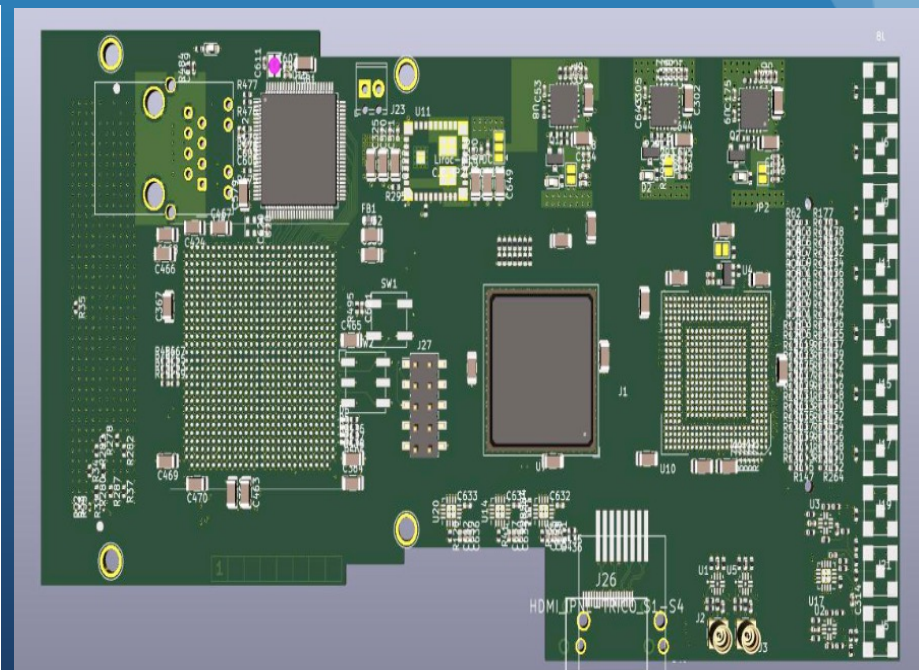
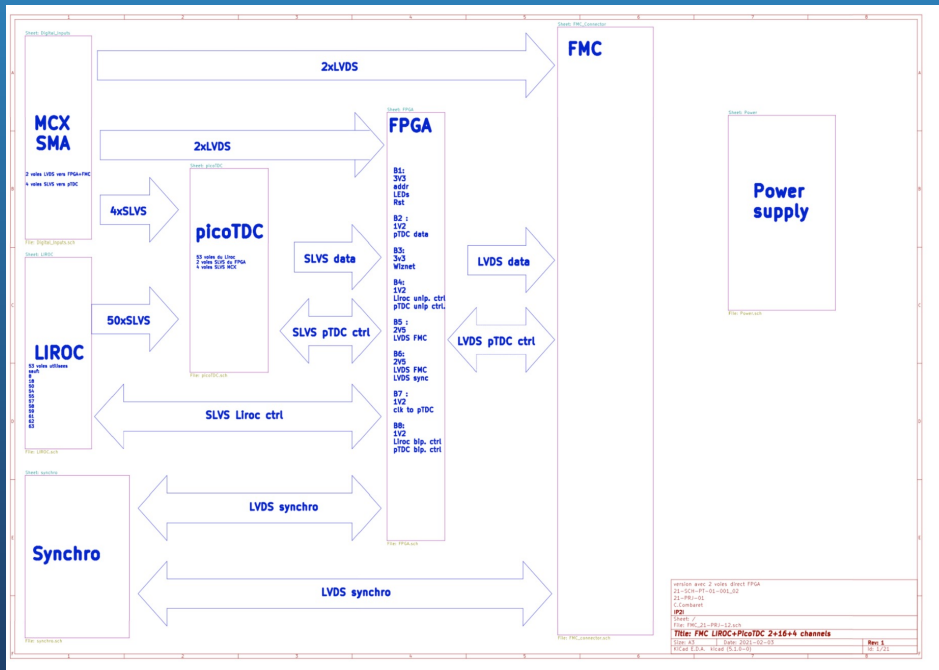
We envisage to use another TDC with negligible dead time to use PICMIC with higher rate



# Next step: Time Measurement

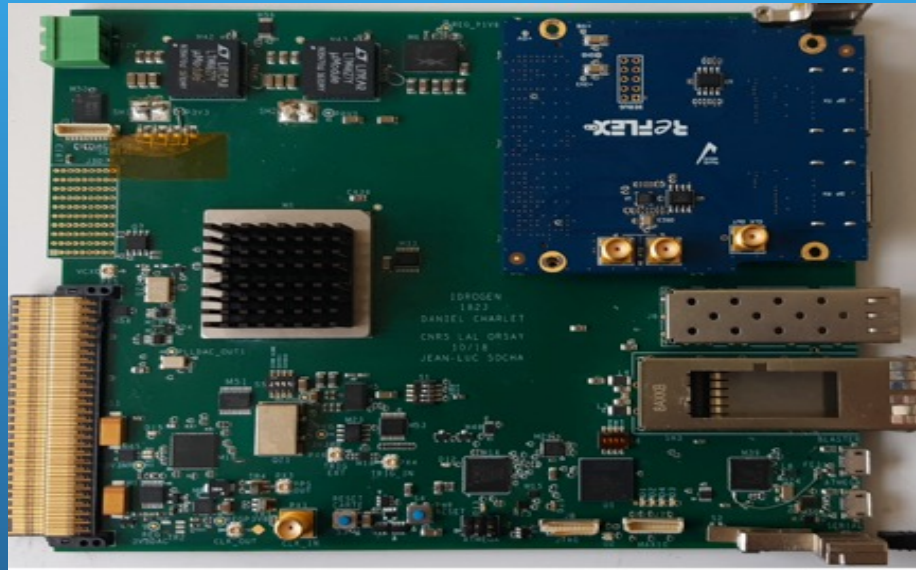
A board integrating a low-jitter timing preamplifier and discriminator (LIROC-OMEGA) as well as a precise TDC (picoTDC-CERN) was conceived. The board will use the GBTX developed by the CERN to communicate with The DAQ system.

The timing board will soon be finalized (all components are available)



## Next step: Acquisition

IDROGEN board that was developed within the DAQGEN of the IN2P3 will be used.



To be able to exploit the IDROGEN board we need:

- develop appropriate interface/mezzanine boards between the IDROGEN and the timing and position boards.
- develop an appropriate firmware

This work is now in advanced stage thanks to A. Back and D. Charlet from IJCLAB.



# Summary

- Principle of very precise time measurement is ok
- Principle of very position measurement is being validated
- A first demonstrator using SAMPIC for time measurement and combining both time and position measurements based on SAMPIC DAQ will allow to have the first demonstrator.
- In parallel a new DAQ system using IDROGEN and exploiting the Liroc of OMEGA group and the CERN picoTDC chips are being developed and will be ready early next year.