

## Fec test report:

Date: 2021-04-28 11:30:02

Tester name: LC

### Test#1 Monitoring values

Failed

0	FEC label	071	OK
1	FEC DC2438 ID	4b0000024dc6b826	OK
2	FEC_T (to 35°C)	24.938	OK
3	FEC_Vdd (3.2V to 3.4V)	3.260	OK
4	FEC_I (1.2A to 1.6A)	1.612	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.930	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3006	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3092	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3117	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3128	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3101	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3045	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3094	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3024	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 24.938 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.260 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.930 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.806 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 4b0000024dc6b826

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.930 V
120	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.930 V
125	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 TdcM(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 TdcM(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.930 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	311.2	0.7	2 r	265.9	0.6	2 r	312.2	0.7	2 r	316.3	0.7	2 r	283.9	0.7	2 r	332.9	0.7	2 r	298.1	0.7	2 r	340.3	0.7
3	218.4	4.8	3	230.0	4.7	3	318.6	5.0	3	232.8	6.1	3	183.6	5.6	3	350.2	4.9	3	182.8	5.5	3	290.9	5.3
4	219.3	4.2	4	201.8	4.6	4	283.6	4.4	4	282.6	5.2	4	201.2	5.5	4	336.6	4.5	4	202.9	4.8	4	260.6	5.2
5	278.3	4.8	5	196.8	4.7	5	280.2	4.6	5	228.1	6.2	5	190.2	5.5	5	312.5	4.7	5	230.5	5.1	5	228.2	5.3
6	231.5	4.5	6	223.4	4.3	6	257.6	4.2	6	290.4	5.1	6	214.5	5.5	6	180.3	4.4	6	243.4	4.9	6	219.7	4.9
7	165.7	4.9	7	218.2	4.9	7	294.3	4.7	7	259.0	5.6	7	200.0	5.2	7	241.4	4.7	7	170.2	5.2	7	322.6	5.4
8	134.7	4.3	8	173.6	4.5	8	277.6	4.3	8	202.7	5.2	8	178.4	5.5	8	279.4	4.5	8	167.5	4.7	8	328.1	5.2
9	199.1	4.6	9	195.9	4.5	9	293.4	4.8	9	262.0	5.4	9	204.1	5.1	9	301.9	4.6	9	263.9	4.7	9	283.2	5.1
10	218.7	4.2	10	236.8	4.3	10	297.0	4.4	10	229.4	4.9	10	214.7	5.3	10	264.8	4.6	10	220.9	4.9	10	251.3	5.2
11	144.2	4.7	11	126.6	4.6	11	275.7	4.8	11	262.2	5.4	11	274.1	5.3	11	264.7	4.7	11	179.1	5.0	11	262.1	5.2
12	180.2	4.3	12	235.2	4.0	12	284.0	4.3	12	284.5	5.0	12	227.0	5.3	12	265.4	4.5	12	236.7	4.6	12	236.2	5.1
13	173.3	4.7	13	171.2	4.8	13	257.8	4.5	13	195.6	5.6	13	221.8	5.2	13	260.7	4.5	13	264.0	4.8	13	300.3	5.1
14	207.9	4.5	14	194.9	4.6	14	187.1	4.4	14	250.1	5.0	14	156.5	5.1	14	297.9	4.4	14	150.7	4.9	14	241.4	4.9
15 f	169.6	1.6	15 f	154.8	1.6	15 f	369.5	1.5	15 f	174.3	1.6	15 f	185.3	1.7	15 f	313.0	1.7	15 f	202.3	1.6	15 f	291.9	1.5
16	192.4	4.5	16	246.7	4.6	16	325.7	4.5	16	274.9	5.4	16	258.1	4.9	16	326.7	4.6	16	176.0	4.7	16	256.4	5.1
17	142.3	4.4	17	129.2	4.2	17	381.8	4.1	17	212.1	5.0	17	217.4	5.0	17	344.9	4.5	17	138.1	4.6	17	305.6	5.1
18	226.5	4.3	18	219.6	4.7	18	363.6	4.5	18	199.3	5.1	18	250.3	5.0	18	252.3	4.6	18	76.5	4.7	18	214.7	5.0
19	217.0	4.2	19	63.2	4.1	19	229.2	4.1	19	228.8	4.7	19	218.9	5.1	19	289.3	4.6	19	128.0	4.8	19	218.0	4.8
20	149.4	4.6	20	237.9	4.5	20	296.0	4.5	20	269.8	5.2	20	255.2	4.9	20	242.5	4.4	20	168.4	4.8	20	266.9	5.0
21	224.3	4.1	21	202.5	4.1	21	308.8	4.3	21	209.5	4.6	21	250.5	5.1	21	320.6	4.5	21	129.6	4.9	21	306.1	5.0
22	216.6	4.4	22	259.5	4.2	22	294.1	4.6	22	271.8	5.2	22	285.5	4.8	22	321.1	4.4	22	179.2	4.7	22	197.6	5.5
23	209.7	4.0	23	143.7	4.3	23	305.9	4.3	23	288.9	4.5	23	205.0	5.0	23	304.9	4.4	23	199.9	4.8	23	226.0	4.8
24	211.0	4.4	24	170.9	4.2	24	252.4	4.3	24	321.4	4.8	24	283.2	4.8	24	302.4	4.6	24	130.1	5.1	24	292.6	5.2
25	77.1	4.3	25	159.9	4.3	25	281.4	4.1	25	277.8	4.7	25	254.5	5.2	25	338.4	4.7	25	191.5	4.8	25	218.8	4.8
26	193.8	4.4	26	221.0	4.3	26	289.6	4.4	26	259.5	5.0	26	299.3	4.8	26	244.0	4.5	26	204.0	4.7	26	181.1	5.2
27	236.1	4.1	27	175.4	4.4	27	310.0	4.1	27	258.9	4.7	27	198.5	5.2	27	252.7	4.4	27	108.5	4.6	27	278.4	5.0
28 f	253.8	1.6	28 f	151.6	1.7	28 f	260.7	1.7	28 f	207.7	1.7	28 f	199.4	1.8	28 f	202.5	1.7	28 f	208.4	1.7	28 f	262.4	1.7
29	263.5	4.3	29	207.7	4.6	29	308.6	4.3	29	261.1	5.1	29	294.1	4.8	29	295.0	4.5	29	152.4	4.6	29	265.5	5.1
30	213.5	4.1	30	167.3	4.2	30	318.6	4.5	30	251.4	4.7	30	175.3	5.2	30	277.0	4.2	30	217.4	5.2	30	384.9	5.1
31	191.6	4.4	31	126.6	4.8	31	270.2	4.3	31	187.1	5.1	31	208.8	5.0	31	280.3	4.5	31	199.2	4.8	31	266.8	4.9
32	203.3	3.9	32	189.7	4.2	32	289.0	4.2	32	285.0	4.7	32	298.3	5.0	32	248.4	4.5	32	130.1	4.6	32	240.2	5.0
33	173.2	4.2	33	225.2	4.0	33	258.2	4.2	33	248.2	4.9	33	296.3	5.1	33	271.4	4.3	33	215.8	4.8	33	209.9	5.0
34	193.1	4.2	34	119.1	4.1	34	322.5	4.1	34	182.6	4.5	34	265.0	5.2	34	292.6	4.6	34	249.1	4.7	34	272.6	5.1
35	190.4	4.5	35	175.3	4.5	35	282.4	4.5	35	258.5	5.1	35	180.2	5.3	35	284.1	4.7	35	161.9	4.9	35	176.4	5.3
36	221.0	4.0	36	157.6	4.1	36	243.8	4.1	36	175.5	4.8	36	201.6	5.3	36	275.9	4.8	36	257.5	4.9	36	311.7	5.0
37	171.0	4.3	37	167.9	4.5	37	226.2	4.5	37	367.8	4.8	37	196.7	4.8	37	253.8	4.5	37	212.4	4.7	37	264.8	5.0
38	244.6	4.2	38	189.1	4.1	38	277.6	4.2	38	125.0	4.5	38	293.4	5.0	38	286.5	4.7	38	269.1	5.0	38	202.5	5.2
39	261.8	4.7	39	137.7	4.3	39	251.0	4.5	39	273.3	5.0	39	247.3	5.2	39	278.7	4.8	39	242.0	5.3	39	212.9	5.4
40	227.4	3.9	40	200.4	4.1	40	270.6	4.3	40	268.7	4.6	40	224.3	5.0	40	275.9	4.3	40	268.1	5.1	40	362.0	5.4
41	295.4	4.2	41	145.4	4.2	41	288.3	4.0	41	233.8	4.2	41	203.3	4.4	41	309.5	4.1	41	267.3	4.3	41	272.0	4.5
42	146.1	4.0	42	206.2	4.0	42	334.2	4.1	42	242.8	4.5	42	191.7	4.5	42	363.1	4.1	42	181.6	4.6	42	237.3	5.2
43	153.5	4.2	43	142.5	4.0	43	299.6	4.0	43	283.8	4.1	43	114.8	4.4	43	193.0	4.1	43	187.1	4.3	43	312.6	4.6
44	165.5	4.0	44	193.9	3.8	44	292.3	4.1	44	189.5	4.4	44	264.9	4.4	44	322.9	4.7	44	108.6	4.4	44	175.1	5.2
45	242.3	3.9	45	158.4	3.8	45	278.3	4.0	45	235.7	4.0	45	238.2	4.4	45	290.0	4.0	45	155.8	4.3	45	244.3	4.6
46	269.3	3.8	46	148.4	3.9	46	273.7	4.2	46	239.6	4.4	46	241.4	4.4	46	277.5	4.3	46	136.6	5.0	46	221.5	4.9
47	168.2	3.9	47	126.5	3.8	47	273.9	4.0	47	284.7	4.4	47	171.0	4.1	47	262.8	4.0	47	132.9	4.2	47	233.3	4.7
48	143.0	4.6	48	212.2	4.0	48	267.2	4.0	48	335.9	4.5	48	197.5	4.6	48	170.9	4.2	48	207.5	4.7	48	251.3	5.1
49	255.8	3.6	49	92.7	3.7	49	284.3	3.9	49	275.5	4.1	49	244.2	4.3	49	233.7	4.0	49	164.7	4.4	49	259.6	4.5
50	225.1	4.1	50	207.1	3.9	50	283.6	4.0	50	299.1	4.4	50	270.5	4.5	50	356.7	4.2	50	161.6	4.6	50	307.3	5.2
51	158.8	4.1	51	143.6	4.0	51	354.8	3.9	51	222.8	4.1	51	220.6	4.2	51	237.8	4.0	51	177.0	4.4	51	243.4	4.7
52	181.3	4.3	52	162.9	3.9	52	267.9	4.1	52	222.5	4.6	52	236.3	4.3	52	186.5	3.9	52	169.6	4.6	52	255.6	4.7
53 f	240.6	1.4	53 f	131.4	1.4	53 f	335.6	1.6	53 f	253.3	1.5	53 f	233.6	1.5	53 f	250.5	1.5	53 f	185.0	1.6	53 f	225.1	1.6
54	189.4	3.9	54	225.0	4.0	54	351.6	4.1	54	283.4	4.2	54	78.0	4.2	54	313.0	4.2	54	163.3	4.3	54	221.8	4.4
55	209.9	4.0	55	241.7	4.1	55	349.6	4.2	55	297.6	4.5	55	233.7	4.5	55	224.7	4.3	55	72.8	4.7	55	247.9	5.2
56	249.9	3.9	56	191.9	3.9	56	366.5	4.0	56	283.9	4.1	56	183.3	4.5	56	291.9	4.2	56	196.0	4.2	56	274.7	4.7
57	243.1	4.2	57	214.3	3.9	57	331.4	4.3	57	203.9	4.5	57	210.4	4.7	57	253.6	4.4	57	108.7	4.4	57	192.0	5.1
58	223.2	4.0	58	258.6	3.7	58	290.1	3.9	58	246.6	4.1	58	257.1	4.2	5								



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	303.5	9.8	1 r	359.9	8.5	1 r	420.3	10.1	1 r	297.0	10.8	1 r	311.0	9.9	1 r	440.7	10.1	1 r	301.6	8.4	1 r	403.9	9.5
2 r	250.1	0.7	2 r	250.0	0.6	2 r	250.5	0.7	2 r	250.6	0.7	2 r	250.3	0.7	2 r	249.7	0.7	2 r	250.3	0.7	2 r	250.4	0.7
3	251.2	4.7	3	250.8	4.7	3	250.7	4.9	3	250.2	5.9	3	249.4	5.5	3	250.6	4.8	3	251.5	5.3	3	250.4	5.4
4	251.2	4.2	4	250.9	4.2	4	250.4	4.3	4	251.5	5.1	4	251.4	5.7	4	248.2	4.8	4	251.2	4.8	4	250.4	5.0
5	250.2	4.7	5	250.8	4.9	5	250.6	4.7	5	250.1	6.0	5	250.0	5.5	5	250.1	4.7	5	248.6	5.0	5	250.7	5.3
6	250.3	4.5	6	250.8	4.3	6	249.4	4.3	6	250.0	4.9	6	251.4	5.6	6	250.0	4.6	6	250.9	4.8	6	250.8	5.1
7	250.2	4.7	7	249.8	4.6	7	251.7	4.7	7	251.1	5.7	7	250.6	5.2	7	250.4	4.7	7	250.7	5.2	7	249.5	5.0
8	249.4	4.3	8	248.4	4.3	8	250.3	4.5	8	250.0	5.0	8	250.4	5.6	8	250.3	4.6	8	250.4	4.6	8	250.1	5.2
9	249.6	4.6	9	251.1	4.9	9	251.2	4.7	9	249.9	5.4	9	249.9	5.1	9	249.3	4.6	9	250.1	4.9	9	252.1	5.2
10	250.3	4.2	10	250.2	4.3	10	249.5	4.3	10	250.9	5.0	10	248.9	5.3	10	250.5	4.6	10	250.8	4.8	10	251.4	5.3
11	250.3	4.6	11	250.8	4.7	11	249.3	4.5	11	249.7	5.5	11	250.7	5.0	11	249.4	4.6	11	250.1	4.9	11	250.1	5.0
12	250.0	4.2	12	250.8	4.2	12	251.4	4.1	12	249.6	5.0	12	252.5	5.2	12	250.3	4.6	12	249.7	4.7	12	250.7	5.1
13	251.2	4.4	13	250.3	4.4	13	248.0	4.6	13	249.9	5.3	13	250.2	5.0	13	250.5	4.4	13	249.6	4.8	13	250.6	5.2
14	249.4	4.0	14	251.1	4.5	14	250.9	4.2	14	249.8	4.8	14	250.7	5.2	14	249.3	4.9	14	250.9	4.7	14	250.5	4.9
15 f	249.2	1.6	15 f	250.5	1.6	15 f	250.9	1.6	15 f	250.8	1.7	15 f	250.9	1.7	15 f	249.8	1.6	15 f	250.5	1.6	15 f	249.7	1.6
16	250.5	4.2	16	249.8	4.5	16	250.5	4.4	16	250.5	5.2	16	249.8	5.0	16	249.4	4.5	16	248.6	4.8	16	249.7	5.1
17	249.4	4.1	17	250.4	4.1	17	249.9	4.3	17	250.5	4.9	17	251.3	5.2	17	249.1	4.2	17	251.4	4.5	17	250.2	5.0
18	249.5	4.7	18	249.5	4.5	18	250.3	4.4	18	251.2	5.1	18	251.1	4.8	18	251.2	4.4	18	249.7	4.6	18	249.2	4.9
19	250.3	4.4	19	250.9	4.0	19	249.6	4.3	19	250.9	4.7	19	251.9	5.1	19	249.6	4.7	19	250.5	4.5	19	249.0	5.0
20	251.0	4.5	20	248.7	4.5	20	250.1	4.4	20	249.9	5.3	20	252.5	5.0	20	249.1	4.6	20	250.8	4.7	20	249.2	4.9
21	249.4	4.5	21	248.9	4.2	21	251.6	4.3	21	249.3	4.7	21	248.8	5.0	21	248.8	4.3	21	250.5	4.8	21	251.5	5.1
22	249.2	4.3	22	251.3	4.2	22	250.1	4.4	22	250.7	5.1	22	252.3	4.9	22	250.1	4.6	22	249.4	4.8	22	250.7	5.1
23	248.9	4.2	23	249.2	4.2	23	250.7	4.1	23	250.1	4.7	23	249.6	5.2	23	248.7	4.4	23	250.6	4.6	23	250.7	4.8
24	248.7	4.3	24	248.9	4.5	24	250.8	4.3	24	250.3	4.9	24	251.9	4.7	24	249.6	4.4	24	250.8	4.7	24	250.6	5.0
25	250.2	4.1	25	249.4	4.2	25	250.7	3.9	25	251.8	4.6	25	250.7	5.2	25	250.4	4.5	25	250.8	4.6	25	250.6	4.9
26	250.1	4.4	26	250.0	4.4	26	251.1	4.4	26	249.8	5.0	26	251.2	4.8	26	249.7	4.6	26	250.0	4.7	26	250.2	5.2
27	251.1	4.0	27	251.6	4.2	27	252.5	4.2	27	250.1	4.8	27	250.8	4.9	27	250.0	4.5	27	250.7	4.5	27	252.7	4.8
28 f	250.1	1.5	28 f	249.6	1.7	28 f	250.0	1.6	28 f	250.1	1.6	28 f	251.0	1.8	28 f	249.2	1.7	28 f	250.6	1.7	28 f	250.2	1.7
29	248.9	4.5	29	250.6	4.3	29	250.6	4.4	29	251.2	5.0	29	249.8	4.6	29	250.1	4.6	29	251.4	4.6	29	249.8	5.0
30	248.0	4.1	30	250.6	4.3	30	249.9	4.2	30	251.2	4.7	30	250.6	5.1	30	249.7	4.2	30	250.0	4.7	30	249.9	4.8
31	249.1	4.1	31	250.9	4.2	31	251.0	4.4	31	249.8	5.1	31	251.2	4.8	31	249.5	4.5	31	249.6	4.7	31	249.2	5.0
32	250.7	4.1	32	250.3	4.3	32	250.7	4.1	32	250.2	4.6	32	250.0	5.0	32	250.5	4.3	32	251.2	4.8	32	251.2	4.7
33	250.2	4.2	33	250.4	4.5	33	250.8	4.3	33	250.2	4.9	33	250.7	4.7	33	251.1	4.4	33	249.5	4.6	33	250.9	5.3
34	250.6	4.1	34	250.0	3.9	34	249.4	4.0	34	250.2	4.5	34	249.8	5.2	34	249.9	4.6	34	249.9	4.6	34	251.0	5.0
35	250.4	4.4	35	250.2	4.2	35	251.0	4.4	35	250.5	4.8	35	249.8	4.9	35	249.3	4.7	35	250.0	4.5	35	250.7	5.0
36	251.7	3.8	36	249.8	4.2	36	249.8	4.2	36	250.9	4.7	36	250.4	5.1	36	248.9	4.4	36	250.3	4.7	36	249.5	5.1
37	251.0	4.3	37	250.7	4.3	37	250.7	4.4	37	250.8	5.0	37	248.6	4.9	37	250.1	4.4	37	250.6	4.9	37	248.8	4.9
38	248.8	4.2	38	250.4	4.2	38	249.8	4.1	38	251.1	4.5	38	251.0	5.3	38	250.7	4.4	38	252.0	4.8	38	249.9	5.3
39	251.5	4.5	39	250.3	4.2	39	249.7	4.6	39	250.8	5.2	39	250.7	5.2	39	249.6	4.6	39	250.1	5.1	39	252.2	5.6
40	251.1	4.0	40	251.6	4.5	40	249.5	3.8	40	248.5	4.7	40	249.4	5.0	40	248.8	4.6	40	249.3	4.8	40	249.1	5.3
41	250.1	3.9	41	249.0	3.9	41	251.2	4.2	41	250.4	4.1	41	249.9	4.5	41	249.3	4.1	41	250.2	4.5	41	250.3	4.5
42	250.5	4.3	42	250.4	4.0	42	250.3	4.3	42	248.3	4.4	42	249.1	4.5	42	249.5	4.7	42	250.7	4.7	42	250.5	5.4
43	248.7	4.2	43	249.6	4.0	43	250.1	3.7	43	251.6	4.0	43	249.2	4.2	43	250.7	3.9	43	252.3	4.4	43	250.7	4.7
44	250.0	4.2	44	249.6	3.9	44	251.8	4.4	44	250.8	4.4	44	250.5	4.4	44	248.3	4.4	44	249.4	4.6	44	248.9	5.2
45	250.6	4.2	45	251.6	3.8	45	250.6	4.1	45	250.1	4.3	45	251.0	4.5	45	249.3	3.9	45	250.6	4.4	45	251.0	4.6
46	249.8	4.2	46	251.2	4.0	46	251.2	4.0	46	249.4	4.5	46	250.0	4.6	46	250.5	4.2	46	250.8	4.6	46	249.4	5.0
47	249.4	4.2	47	250.2	4.0	47	250.6	3.9	47	250.6	4.1	47	251.7	4.5	47	248.4	4.3	47	250.6	4.3	47	251.8	4.8
48	249.1	4.2	48	250.6	4.0	48	251.9	4.2	48	250.7	4.4	48	250.1	4.5	48	250.3	4.3	48	250.1	4.6	48	251.4	5.2
49	250.1	4.2	49	250.2	3.8	49	250.6	4.1	49	249.0	4.0	49	250.0	4.3	49	248.9	4.3	49	250.7	4.3	49	249.3	4.6
50	251.1	4.2	50	248.8	4.0	50	250.1	4.2	50	250.1	4.5	50	250.5	4.4	50	249.7	4.5	50	249.4	4.5	50	251.6	5.2
51	251.3	3.9	51	249.3	4.0	51	250.5	4.0	51	251.6	4.3	51	250.1	4.3	51	249.5	4.0	51	249.7	4.2	51	250.0	4.7
52	250.9	4.2	52	249.0	4.4	52	248.9	4.0	52	249.8	4.4	52	251.0	4.5	52	250.3	4.3	52	250.8	4.8	52	247.4	5.3
53 f	249.3	1.4	53 f	249.9	1.4	53 f	250.3	1.6	53 f	250.3	1.5	53 f	249.9	1.6	53 f	250.5	1.7	53 f	249.8	1.4	53 f	249.9	1.6
54	251.3	4.1	54	248.0	3.8	54	248.0	4.0	54	249.6	4.1	54	250.2	4.3	54	247.5	4.2	54	250.6	4.5	54	249.3	4.5
55	250.4	4.2	55	250.4	4.2	55	251.9	4.2	55	250.7	4.5	55	251.6	4.5	55	250.0	4.3	55	249.9	4.7	55	249.8	5.5
56	249.6	4.1	56	249.3	4.0	56	249.3	3.9	56	250.2	4.2	56	249.9	4.4	56	250.4	4.1	56	250.5	4.4	56	251.1	4.9
57	250.0	4.2	57	250.6	4.4	57	250.0	4.3	57	250.7	4.4	57	250.3	4.5	57	249.8	4.4	57	251.1	4.7	57	250.4	5.0
58	251.2	3.9	58	249.7	3.9	58	252.0	3.9	58	248.3	4.0												