

Fec test report:

Date: 2021-04-28 08:03:28

Tester name: LC

Test#1 Monitoring values

Failed

| | | | |
|---|------------------------|------------------|------|
| 0 | FEC label | 066 | OK |
| 1 | FEC DC2438 ID | 7c0000024d9b9326 | OK |
| 2 | FEC_T (to 35°C) | 28.844 | OK |
| 3 | FEC_Vdd (3.2V to 3.4V) | 3.290 | OK |
| 4 | FEC_I (1.2A to 1.6A) | 1.06 | FAIL |
| 5 | FEC_Vad (1.9V to 2.0V) | 1.950 | OK |

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpm 4.0)

| | | | | |
|---|---------------|-------------|---------------|------|
| 0 | After chip #0 | Mean FAILED | STDDEV FAILED | FAIL |
| 1 | After chip #1 | Mean FAILED | STDDEV FAILED | FAIL |
| 2 | After chip #2 | Mean FAILED | STDDEV FAILED | FAIL |
| 3 | After chip #3 | Mean FAILED | STDDEV FAILED | FAIL |
| 4 | After chip #4 | Mean FAILED | STDDEV FAILED | FAIL |
| 5 | After chip #5 | Mean FAILED | STDDEV FAILED | FAIL |
| 6 | After chip #6 | Mean FAILED | STDDEV FAILED | FAIL |
| 7 | After chip #7 | Mean FAILED | STDDEV FAILED | FAIL |

Test#4 AD9637 test patterns

Passed

| | | | | |
|---|----------------|--|-------------------|----|
| 0 | ADC channel #0 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 1 | ADC channel #1 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 2 | ADC channel #2 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 3 | ADC channel #3 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |
| 4 | ADC channel #4 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 5 | ADC channel #5 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 6 | ADC channel #6 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 7 | ADC channel #7 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |

Test#5 Pulser run

Passed

| | | | | |
|---|---------------|-----------------------------------|----------------|----|
| 0 | After chip #0 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3007 | OK |
| 1 | After chip #1 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3066 | OK |
| 2 | After chip #2 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3120 | OK |
| 3 | After chip #3 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3124 | OK |
| 4 | After chip #4 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3181 | OK |
| 5 | After chip #5 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3026 | OK |
| 6 | After chip #6 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3130 | OK |
| 7 | After chip #7 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3057 | OK |

FEC test final result:

Failed

| Monitoring test | | | |
|-----------------|---------------------------|-------|--|
| NO | Command | Error | Response |
| 0 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 1 | fe 0 moni T 0 | 0 | 0 Tdcm(2) Fem(00) FEC_T: 28.844 degC |
| 2 | fe 0 moni V 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V |
| 3 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 4 | fe 0 pulser 0 base 0x3FFF | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 5 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 6 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 7 | fe 0 moni I 0 | 0 | 0 Tdcm(2) Fem(00) FEC_I: 0.530 A |
| 8 | fe 0 moni S 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Serial: 7c0000024d9b9326 |

| Slow control registers test | | | |
|-----------------------------|--|-------|--|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 2 | fe fec_enable | 0 | 0 Tdcm(2) Fem(00) Reg(1) = 0x2048007 (33849351) FEC_Enable: 1 |
| 3 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 4 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 5 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 6 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 7 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 8 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 9 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 10 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 11 | fe 0 after 0 wrchk 3 0x0 0x0101 0x0101 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified) |
| 12 | fe 0 after 1 wrchk 3 0x0 0x0202 0x0202 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified) |
| 13 | fe 0 after 2 wrchk 3 0x0 0x0303 0x0303 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified) |
| 14 | fe 0 after 3 wrchk 3 0x0 0x0404 0x0404 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified) |
| 15 | fe 0 after 4 wrchk 3 0x0 0x0505 0x0505 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified) |
| 16 | fe 0 after 5 wrchk 3 0x0 0x0606 0x0606 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified) |
| 17 | fe 0 after 6 wrchk 3 0x0 0x0707 0x0707 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified) |
| 18 | fe 0 after 7 wrchk 3 0x0 0x0808 0x0808 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified) |
| 19 | fe 0 after 0 read 3 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101 |
| 20 | fe 0 after 1 read 3 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202 |
| 21 | fe 0 after 2 read 3 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303 |
| 22 | fe 0 after 3 read 3 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404 |
| 23 | fe 0 after 4 read 3 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505 |
| 24 | fe 0 after 5 read 3 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606 |
| 25 | fe 0 after 6 read 3 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707 |
| 26 | fe 0 after 7 read 3 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808 |
| 27 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 28 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 29 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 30 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 31 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 32 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 33 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 34 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |

| ADC pattern test | | | |
|------------------|--------------------------|-------|---|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe 0 test_mode | 0 | 0 Tdcm(2) Fem(00) Reg(5) = 0x110420c4 (285483204) Test_Mode: 0 |
| 2 | be 0 state eb | 0 | 0 Tdcm(2) Reg(27) = 0x8020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current |
| 3 | be 0 state tg | 0 | 0 Tdcm(2) Reg(27) = 0x8020003 (Trigger_Generator: FEM_BUSY) |
| 4 | be 0 state pm | 0 | 0 Tdcm(2) Reg(27) = 0x8020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 5 | fe 0 state | 0 | 0 Tdcm(2) Fem(00) State = 0x11 (Aligned Dev_Ready) |
| 6 | daq 0xFFFF F | 0 | 0 Tdcm(2): daq paused |
| 7 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 8 | fe 0 emit_empty_ch 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 10 | fe 0 keep_rst 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 11 | fe 0 skip_rst 2 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x40000 |
| 12 | fe adc 0 model AD9637 | 0 | 0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637) |
| 13 | fe adc 0 write 0x14 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0) |
| 14 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 15 | fe adc 0 write 0x5 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1) |
| 16 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 17 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 18 | fe adc 0 write 0x5 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2) |
| 19 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 20 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |

| | | | |
|----|-------------------------|---|---|
| 21 | fe adc 0 write 0x5 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4) |
| 22 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 23 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 24 | fe adc 0 write 0x5 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8) |
| 25 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 26 | fe adc 0 write 0x4 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1) |
| 27 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 28 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 29 | fe adc 0 write 0x4 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2) |
| 30 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 31 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 32 | fe adc 0 write 0x4 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4) |
| 33 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 34 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 35 | fe adc 0 write 0x4 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8) |
| 36 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 37 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 38 | fe 0 subtract_ped 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 39 | fe 0 zero_suppress 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 40 | fe 0 zs_pre_post 4 8 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0xc4 |
| 41 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 42 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 43 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 44 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 45 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 46 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 47 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 48 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 49 | be 0 trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x1000 |
| 50 | be 0 trig_ena 0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 51 | be 0 state eb | 0 | 0 Tdc(2) Reg(27) = 0x8020003 (Event_Builder: COLLECTING_SOE_WAIT_FEM_PKT Current) |
| 52 | be 0 state tg | 0 | 0 Tdc(2) Reg(27) = 0x8020003 (Trigger_Generator: FEM_BUSY) |
| 53 | be 0 state pm | 0 | 0 Tdc(2) Reg(27) = 0x8020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 54 | fe 0 state | 0 | 0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready) |
| 55 | fe adc 0 write 0x4 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15) |
| 56 | fe adc 0 write 0x5 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15) |
| 57 | fe adc 0 write 0xD 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0) |

| Pulser test | | | |
|-------------|------------------------------------|-------|---|
| NO | Command | Error | Response |
| 0 | daq 0FFFFFFF F | 0 | 0 Tdc(2): daq paused |
| 1 | fe 0 after 0:7 wrchk 3 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 2 | fe 0 after 0:7 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 3 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 4 | fe 0 emit_empty_ch 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 5 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 6 | fe 0 keep_rst 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 7 | fe 0 skip_rst 2 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000 |
| 8 | fe 0 test_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 test_mode 1 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x400 |
| 10 | fe 0 tdata A 0x1FF | 0 | 0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510 |
| 11 | fe 0 test_zbt 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 12 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 13 | fe 0 asic_mask | 0 | 0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0 |
| 14 | fe 0 pulser 0 enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 15 | fe 0 pulser 0 ft_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 16 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 17 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 18 | fe 0 pulser 0 ampl 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff |
| 19 | fe 0 pulser 0 delay 3000 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0xbb8 |
| 20 | fe pulser load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 21 | fe 0 pulser 0 enable 1 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x10000 |
| 22 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 23 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 24 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 25 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 26 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 27 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 28 | be 0 trig_delay 0 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 29 | be 0 trig_delay 1 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 30 | be 0 trig_delay 2 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 31 | be 0 trig_delay 3 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 32 | be 0 ss_trig_delay 0x4 | 0 | 0 Tdc(2) Reg(14) <- 0x4 |
| 33 | be 0 ss_trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x10000 |
| 34 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 35 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 36 | be 0 isobus 0x0C | 0 | 0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear) |

| | | | |
|-----|--|---|--|
| 37 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 38 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 39 | fe 0 asic_mask 0xfffe | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000 |
| 40 | fe 0 after 0 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration |
| 41 | fe 0 after 0 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 42 | fe 0 after 0 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 43 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 44 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 45 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 46 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 47 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 48 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 49 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 50 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 51 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 52 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 53 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 54 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 55 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 56 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 57 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 58 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 59 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 60 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 61 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 62 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 63 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 64 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 65 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 66 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 67 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 68 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 69 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 70 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 71 | fe 0 asic_mask 0xfffd | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffd0000 |
| 72 | fe 0 after 1 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration |
| 73 | fe 0 after 1 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 74 | fe 0 after 1 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 75 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 76 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 77 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 78 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 79 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 80 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 81 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 82 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 83 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 84 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 85 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 86 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 87 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 88 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 89 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 90 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 91 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 92 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 93 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 94 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 95 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 96 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 97 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 98 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 99 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 100 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 101 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 102 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 103 | fe 0 asic_mask 0xfffb | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffb0000 |
| 104 | fe 0 after 2 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration |
| 105 | fe 0 after 2 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 106 | fe 0 after 2 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 107 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 108 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 109 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 110 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 111 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 112 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 113 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 114 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |

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| 115 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 116 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 117 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 118 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 119 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 120 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 121 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 122 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 123 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 124 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 125 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 126 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 127 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 128 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 129 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 130 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 131 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 132 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 133 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 134 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 135 | fe 0 asic_mask 0xffff | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000 |
| 136 | fe 0 after 3 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration |
| 137 | fe 0 after 3 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 138 | fe 0 after 3 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 139 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 140 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 141 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 142 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 143 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 144 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 145 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 146 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 147 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 148 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 149 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 150 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 151 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 152 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 153 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 154 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 155 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 156 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 157 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 158 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 159 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 160 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 161 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 162 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 163 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 164 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 165 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 166 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 167 | fe 0 asic_mask 0xffef | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000 |
| 168 | fe 0 after 4 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration |
| 169 | fe 0 after 4 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 170 | fe 0 after 4 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 171 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 172 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0 |

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| 193 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 194 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 195 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 196 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 197 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 198 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 199 | fe 0 asic_mask 0xffdf | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000 |
| 200 | fe 0 after 5 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration |
| 201 | fe 0 after 5 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 202 | fe 0 after 5 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 203 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 204 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 205 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 206 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 207 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 208 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 209 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 210 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 211 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 212 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 213 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 214 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 215 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 216 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 217 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 218 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 219 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 220 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 221 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 222 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 223 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 224 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 225 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 226 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 227 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 228 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 229 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 230 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 231 | fe 0 asic_mask 0xffbf | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000 |
| 232 | fe 0 after 6 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration |
| 233 | fe 0 after 6 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 234 | fe 0 after 6 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 235 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 236 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 237 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 238 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 239 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 240 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 241 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 242 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 243 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 244 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 245 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 246 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 247 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 248 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 249 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 250 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 251 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 252 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 253 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 254 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 255 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 256 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 257 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 258 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 259 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 260 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 261 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 262 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 263 | fe 0 asic_mask 0xff7f | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000 |
| 264 | fe 0 after 7 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration |
| 265 | fe 0 after 7 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 266 | fe 0 after 7 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 267 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 268 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 269 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 270 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |

| | | | |
|-----|--------------------------|---|--|
| 271 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 272 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 273 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 274 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 275 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 276 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 277 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 278 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 279 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 280 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 281 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 282 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 283 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 284 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 285 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 286 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 287 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 288 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 289 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 290 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 291 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 292 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 293 | be 0 trig_ena 0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |

Pedestal data before centermean

| CHIP 0 | | | CHIP 1 | | | CHIP 2 | | | CHIP 3 | | | CHIP 4 | | | CHIP 5 | | | CHIP 6 | | | CHIP 7 | | |
|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 |
| 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 486.1 | 9.4 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 |
| 2 r | 322.7 | 0.7 | 2 r | 363.1 | 0.6 | 2 r | 295.2 | 0.7 | 2 r | 318.1 | 0.7 | 2 r | 267.1 | 0.6 | 2 r | 312.3 | 0.7 | 2 r | 264.7 | 0.7 | 2 r | 342.8 | 0.7 |
| 3 | 294.2 | 4.8 | 3 | 409.1 | 4.5 | 3 | 362.3 | 4.8 | 3 | 192.0 | 5.1 | 3 | 293.0 | 5.2 | 3 | 227.8 | 4.3 | 3 | 237.2 | 5.0 | 3 | 343.4 | 5.3 |
| 4 | 283.9 | 4.5 | 4 | 387.1 | 4.7 | 4 | 252.5 | 4.4 | 4 | 252.8 | 4.8 | 4 | 207.0 | 5.2 | 4 | 199.9 | 4.3 | 4 | 219.7 | 5.1 | 4 | 314.9 | 4.5 |
| 5 | 212.7 | 4.3 | 5 | 349.8 | 4.5 | 5 | 290.0 | 4.7 | 5 | 273.1 | 4.8 | 5 | 151.2 | 4.6 | 5 | 230.6 | 4.6 | 5 | 187.2 | 4.9 | 5 | 359.5 | 4.8 |
| 6 | 319.3 | 4.4 | 6 | 375.8 | 4.0 | 6 | 350.0 | 4.2 | 6 | 196.8 | 4.7 | 6 | 280.4 | 5.0 | 6 | 309.1 | 4.6 | 6 | 169.9 | 4.4 | 6 | 313.8 | 4.6 |
| 7 | 267.4 | 4.0 | 7 | 341.6 | 4.4 | 7 | 260.7 | 4.3 | 7 | 244.8 | 4.9 | 7 | 229.2 | 5.0 | 7 | 197.4 | 4.8 | 7 | 130.6 | 4.6 | 7 | 375.0 | 5.2 |
| 8 | 254.3 | 4.2 | 8 | 310.8 | 3.9 | 8 | 299.0 | 4.2 | 8 | 262.2 | 4.2 | 8 | 185.4 | 4.7 | 8 | 245.9 | 4.0 | 8 | 208.8 | 4.2 | 8 | 366.3 | 4.9 |
| 9 | 234.3 | 4.1 | 9 | 297.9 | 4.3 | 9 | 258.0 | 4.7 | 9 | 177.3 | 5.0 | 9 | 188.8 | 4.9 | 9 | 251.7 | 3.9 | 9 | 193.5 | 4.4 | 9 | 253.9 | 4.2 |
| 10 | 317.8 | 4.4 | 10 | 363.0 | 4.1 | 10 | 264.3 | 4.2 | 10 | 173.7 | 4.9 | 10 | 236.5 | 5.2 | 10 | 211.6 | 4.4 | 10 | 231.9 | 4.7 | 10 | 298.5 | 4.5 |
| 11 | 246.9 | 4.6 | 11 | 328.8 | 4.3 | 11 | 248.1 | 4.5 | 11 | 177.9 | 4.5 | 11 | 314.2 | 4.9 | 11 | 162.0 | 4.3 | 11 | 145.8 | 4.4 | 11 | 362.4 | 4.7 |
| 12 | 174.6 | 4.0 | 12 | 376.0 | 4.0 | 12 | 265.0 | 4.5 | 12 | 244.8 | 4.2 | 12 | 232.9 | 5.0 | 12 | 227.9 | 4.8 | 12 | 246.6 | 4.6 | 12 | 334.6 | 4.7 |
| 13 | 258.5 | 4.2 | 13 | 341.5 | 4.0 | 13 | 329.0 | 4.5 | 13 | 264.1 | 4.7 | 13 | 150.4 | 5.2 | 13 | 183.0 | 4.2 | 13 | 165.8 | 4.5 | 13 | 284.3 | 4.5 |
| 14 | 273.1 | 3.9 | 14 | 351.2 | 4.4 | 14 | 304.1 | 4.1 | 14 | 246.6 | 4.5 | 14 | 206.1 | 5.2 | 14 | 228.7 | 4.4 | 14 | 190.2 | 4.5 | 14 | 302.4 | 4.8 |
| 15 f | 209.6 | 1.5 | 15 f | 372.7 | 1.4 | 15 f | 265.3 | 1.5 | 15 f | 189.0 | 1.6 | 15 f | 215.1 | 1.5 | 15 f | 284.7 | 1.4 | 15 f | 150.4 | 1.5 | 15 f | 262.6 | 1.5 |
| 16 | 199.7 | 4.5 | 16 | 316.3 | 4.4 | 16 | 281.3 | 4.3 | 16 | 211.5 | 4.7 | 16 | 243.7 | 4.4 | 16 | 253.1 | 4.2 | 16 | 143.4 | 4.6 | 16 | 327.3 | 4.2 |
| 17 | 172.1 | 4.0 | 17 | 269.1 | 3.8 | 17 | 273.0 | 4.2 | 17 | 283.3 | 4.6 | 17 | 208.3 | 5.3 | 17 | 129.4 | 4.2 | 17 | 241.6 | 4.4 | 17 | 343.1 | 4.6 |
| 18 | 304.8 | 4.1 | 18 | 326.2 | 4.2 | 18 | 354.9 | 4.1 | 18 | 239.2 | 4.7 | 18 | 251.9 | 4.8 | 18 | 158.8 | 4.1 | 18 | 305.1 | 4.4 | 18 | 330.9 | 4.5 |
| 19 | 218.5 | 4.2 | 19 | 279.4 | 4.0 | 19 | 244.0 | 4.2 | 19 | 281.9 | 4.4 | 19 | 247.6 | 4.5 | 19 | 202.8 | 4.4 | 19 | 192.9 | 4.4 | 19 | 245.7 | 4.6 |
| 20 | 268.1 | 4.2 | 20 | 366.2 | 4.3 | 20 | 240.4 | 4.1 | 20 | 269.2 | 4.3 | 20 | 235.4 | 4.2 | 20 | 205.8 | 4.1 | 20 | 216.0 | 4.3 | 20 | 330.6 | 4.6 |
| 21 | 313.2 | 4.1 | 21 | 424.1 | 3.9 | 21 | 199.8 | 4.5 | 21 | 253.9 | 4.0 | 21 | 158.3 | 4.8 | 21 | 168.2 | 4.4 | 21 | 62.4 | 4.6 | 21 | 300.9 | 4.7 |
| 22 | 224.9 | 4.2 | 22 | 372.3 | 4.2 | 22 | 302.7 | 4.2 | 22 | 234.7 | 4.3 | 22 | 263.2 | 4.6 | 22 | 220.7 | 4.5 | 22 | 147.4 | 4.1 | 22 | 241.8 | 4.2 |
| 23 | 257.7 | 4.1 | 23 | 375.4 | 4.5 | 23 | 260.6 | 4.3 | 23 | 108.9 | 4.3 | 23 | 155.4 | 5.5 | 23 | 213.5 | 3.9 | 23 | 180.0 | 4.5 | 23 | 235.4 | 4.8 |
| 24 | 203.0 | 4.2 | 24 | 388.0 | 4.0 | 24 | 269.6 | 4.1 | 24 | 193.7 | 4.7 | 24 | 180.1 | 4.7 | 24 | 219.3 | 4.2 | 24 | 178.0 | 4.6 | 24 | 320.7 | 4.4 |
| 25 | 338.2 | 4.2 | 25 | 335.9 | 4.0 | 25 | 288.1 | 4.5 | 25 | 159.1 | 4.4 | 25 | 235.5 | 4.9 | 25 | 121.1 | 4.0 | 25 | 140.6 | 4.4 | 25 | 290.8 | 4.4 |
| 26 | 265.4 | 4.4 | 26 | 342.6 | 4.4 | 26 | 292.2 | 4.1 | 26 | 212.3 | 4.4 | 26 | 193.4 | 4.5 | 26 | 214.8 | 4.0 | 26 | 178.2 | 4.7 | 26 | 346.9 | 4.3 |
| 27 | 380.9 | 4.1 | 27 | 290.5 | 4.1 | 27 | 312.4 | 4.1 | 27 | 203.9 | 4.2 | 27 | 227.6 | 5.0 | 27 | 228.2 | 4.2 | 27 | 253.6 | 4.8 | 27 | 303.4 | 4.8 |
| 28 f | 286.4 | 1.5 | 28 f | 315.7 | 1.6 | 28 f | 266.6 | 1.5 | 28 f | 289.4 | 1.7 | 28 f | 211.4 | 1.5 | 28 f | 202.9 | 1.6 | 28 f | 159.6 | 1.7 | 28 f | 351.3 | 1.6 |
| 29 | 155.7 | 4.2 | 29 | 302.9 | 4.4 | 29 | 284.4 | 4.1 | 29 | 213.2 | 4.2 | 29 | 215.2 | 5.0 | 29 | 110.8 | 4.4 | 29 | 136.1 | 4.2 | 29 | 279.4 | 4.5 |
| 30 | 286.4 | 4.0 | 30 | 318.2 | 4.2 | 30 | 207.6 | 4.0 | 30 | 243.4 | 4.3 | 30 | 194.9 | 4.5 | 30 | 176.8 | 4.2 | 30 | 240.2 | 4.4 | 30 | 282.9 | 4.5 |
| 31 | 266.2 | 4.3 | 31 | 293.9 | 4.0 | 31 | 153.4 | 4.1 | 31 | 211.9 | 4.5 | 31 | 169.0 | 4.8 | 31 | 286.9 | 4.5 | 31 | 159.6 | 4.8 | 31 | 323.1 | 4.6 |
| 32 | 329.1 | 3.9 | 32 | 383.1 | 4.1 | 32 | 236.9 | 4.1 | 32 | 178.5 | 4.3 | 32 | 282.5 | 5.1 | 32 | 282.0 | 4.2 | 32 | 121.7 | 4.7 | 32 | 330.6 | 4.8 |
| 33 | 264.5 | 4.1 | 33 | 381.5 | 4.0 | 33 | 287.0 | 3.9 | 33 | 274.4 | 4.5 | 33 | 110.1 | 4.7 | 33 | 314.4 | 4.6 | 33 | 125.5 | 4.3 | 33 | 247.3 | 4.6 |
| 34 | 208.4 | 3.9 | 34 | 335.0 | 3.8 | 34 | 303.0 | 4.3 | 34 | 354.4 | 4.2 | 34 | 251.3 | 4.8 | 34 | 215.1 | 4.3 | 34 | 134.7 | 4.5 | 34 | 321.2 | 4.3 |
| 35 | 272.5 | 4.5 | 35 | 339.1 | 3.9 | 35 | 301.1 | 4.0 | 35 | 293.0 | 4.4 | 35 | 210.7 | 4.7 | 35 | 232.6 | 4.3 | 35 | 286.5 | 4.3 | 35 | 333.3 | 4.1 |
| 36 | 255.8 | 3.8 | 36 | 296.8 | 3.9 | 36 | 258.0 | 4.1 | 36 | 354.0 | 4.3 | 36 | 161.8 | 4.8 | 36 | 233.1 | 4.4 | 36 | 166.8 | 4.3 | 36 | 311.6 | 5.0 |
| 37 | 224.7 | 4.0 | 37 | 378.7 | 3.8 | 37 | 238.7 | 4.1 | 37 | 237.0 | 4.5 | 37 | 162.2 | 4.8 | 37 | 151.3 | 4.6 | 37 | 233.9 | 4.1 | 37 | 240.8 | 4.3 |
| 38 | 293.2 | 3.9 | 38 | 261.0 | 4.0 | 38 | 260.5 | 4.0 | 38 | 229.0 | 4.4 | 38 | 234.2 | 4.9 | 38 | 216.6 | 4.3 | 38 | 316.9 | 4.1 | 38 | 326.9 | 4.5 |
| 39 | 253.5 | 4.1 | 39 | 398.7 | 4.1 | 39 | 281.4 | 4.3 | 39 | 224.2 | 4.9 | 39 | 229.7 | 5.4 | 39 | 211.2 | 4.4 | 39 | 258.7 | 4.8 | 39 | 306.3 | 4.8 |
| 40 | 266.5 | 3.8 | 40 | 316.1 | 4.2 | 40 | 272.0 | 3.9 | 40 | 252.6 | 4.1 | 40 | 204.5 | 4.8 | 40 | 297.2 | 4.0 | 40 | 249.3 | 4.3 | 40 | 333.8 | 4.7 |
| 41 | 408.6 | 4.3 | 41 | 306.0 | 3.8 | 41 | 225.0 | 3.9 | 41 | 213.1 | 4.2 | 41 | 206.6 | 4.8 | 41 | 279.1 | 4.3 | 41 | 189.2 | 4.7 | 41 | 301.5 | 4.8 |
| 42 | 278.7 | 4.5 | 42 | 302.3 | 4.2 | 42 | 234.7 | 4.3 | 42 | 217.3 | 4.5 | 42 | 249.7 | 4.7 | 42 | 128.1 | 4.4 | 42 | 192.6 | 4.8 | 42 | 319.3 | 4.7 |
| 43 | 333.9 | 4.4 | 43 | 346.7 | 4.0 | 43 | 237.7 | 4.0 | 43 | 208.6 | 4.2 | 43 | 111.5 | 4.8 | 43 | 180.2 | 4.2 | 43 | 233.1 | 4.3 | 43 | 270.8 | 5.0 |
| 44 | 379.5 | 4.6 | 44 | 373.1 | 4.2 | 44 | 318.1 | 4.1 | 44 | 283.9 | 4.4 | 44 | 216.8 | 4.4 | 44 | 216.2 | 4.2 | 44 | 246.2 | 4.5 | 44 | 305.5 | 4.6 |
| 45 | 270.8 | 3.9 | 45 | 295.1 | 3.7 | 45 | 216.0 | 4.4 | 45 | 210.3 | 4.3 | 45 | 243.4 | 4.7 | 45 | 259.6 | 4.3 | 45 | 254.2 | 4.2 | 45 | 309.7 | 4.9 |
| 46 | 201.1 | 4.0 | 46 | 359.1 | 4.2 | 46 | 280.6 | 4.1 | 46 | 239.2 | 4.6 | 46 | 170.1 | 4.5 | 46 | 263.8 | 4.2 | 46 | 127.6 | 4.3 | 46 | 304.0 | 4.8 |
| 47 | 280.5 | 4.2 | 47 | 358.4 | 4.2 | 47 | 193.1 | 4.0 | 47 | 182.9 | 4.2 | 47 | 202.0 | 4.8 | 47 | 223.2 | 4.2 | 47 | 221.6 | 4.2 | 47 | 208.8 | 4.7 |
| 48 | 263.1 | 4.4 | 48 | 391.2 | 4.0 | 48 | 171.0 | 4.3 | 48 | 150.7 | 4.3 | 48 | 149.3 | 4.8 | 48 | 252.8 | 4.4 | 48 | 170.0 | 4.4 | 48 | 277.3 | 4.9 |
| 49 | 283.8 | 4.3 | 49 | 285.1 | 4.2 | 49 | 294.3 | 4.2 | 49 | 193.3 | 4.3 | 49 | 281.4 | 4.7 | 49 | 265.7 | 4.2 | 49 | 312.3 | 4.4 | 49 | 240.0 | 5.1 |
| 50 | 279.1 | 4.4 | 50 | 346.1 | 4.4 | 50 | 262.7 | 4.5 | 50 | 278.1 | 4.2 | 50 | 211.4 | 4.6 | 50 | 238.2 | 4.4 | 50 | 239.7 | 4.7 | 50 | 295.2 | 5.0 |
| 51 | 236.4 | 4.4 | 51 | 353.1 | 3.9 | 51 | 327.9 | 4.3 | 51 | 194.6 | 4.2 | 51 | 224.3 | 4.8 | 51 | 220.0 | 4.1 | 51 | 165.4 | 4.5 | 51 | 346.9 | 4.6 |
| 52 | 246.6 | 4.2 | 52 | 378.5 | 4.2 | 52 | 234.2 | 4.5 | 52 | 239.6 | 4.3 | 52 | 121.2 | 4.9 | 52 | 227.7 | 4.3 | 52 | 197.8 | 4.6 | 52 | 310.4 | 4.8 |
| 53 f | 209.8 | 1.8 | 53 f | 409.1 | 1.8 | 53 f | 226.0 | 1.5 | 53 f | 170.2 | 1.7 | 53 f | 237.8 | 1.8 | 53 f | 268.7 | 1.5 | 53 f | 187.8 | 1.6 | 53 f | 312.4 | 1.7 |
| 54 | 352.1 | 4.4 | 54 | 379.5 | 4.2 | 54 | 180.5 | 4.1 | 54 | 207.5 | 4.4 | 54 | 253.9 | 5.0 | 54 | 272.7 | 4.4 | 54 | 223.7 | 4.4 | 54 | 324.8 | 4.9 |
| 55 | 282.2 | 4.4 | 55 | 348.6 | 4.0 | 55 | 248.6 | 4.7 | 55 | 241.3 | 4.5 | 55 | 302.0 | 4.8 | 55 | 163.9 | 4.1 | 55 | 198.4 | 4.5 | 55 | 306.9 | 4.7 |
| 56 | 264.8 | 4.1 | 56 | 275.9 | 4.0 | 56 | 249.6 | 3.8 | 56 | 274.9 | 4.3 | 56 | 205.6 | 4.3 | 56 | 149.0 | 4.1 | 56 | 227.2 | 4.5 | 56 | 313.6 | 4.7 |
| 57 | 206.4 | 4.5 | 57 | 348.8 | 4.1 | 57 | 347.3 | 4.3 | 57 | 200.1 | 4.3 | 57 | 164.2 | 4.6 | 57 | 179.7 | 4.2 | 57 | 255.2 | 4.4 | 57 | 312.9 | 4.8 |
| 58 | 247.8 | 4.3 | 58 | 406.0 | 4.0 | 58 | 2 | | | | | | | | | | | | | | | | |

Pedestal after centermean.

| CHIP 0 | | |
|--------|-----|-----|
| CH | M | STD |
| 0r | 0.0 | 0.0 |
| 1r | 0.0 | 0.0 |
| 2r | 0.0 | 0.0 |
| 3 | 0.0 | 0.0 |
| 4 | 0.0 | 0.0 |
| 5 | 0.0 | 0.0 |
| 6 | 0.0 | 0.0 |
| 7 | 0.0 | 0.0 |
| 8 | 0.0 | 0.0 |
| 9 | 0.0 | 0.0 |
| 10 | 0.0 | 0.0 |
| 11 | 0.0 | 0.0 |
| 12 | 0.0 | 0.0 |
| 13 | 0.0 | 0.0 |
| 14 | 0.0 | 0.0 |
| 15f | 0.0 | 0.0 |
| 16 | 0.0 | 0.0 |
| 17 | 0.0 | 0.0 |
| 18 | 0.0 | 0.0 |
| 19 | 0.0 | 0.0 |
| 20 | 0.0 | 0.0 |
| 21 | 0.0 | 0.0 |
| 22 | 0.0 | 0.0 |
| 23 | 0.0 | 0.0 |
| 24 | 0.0 | 0.0 |
| 25 | 0.0 | 0.0 |
| 26 | 0.0 | 0.0 |
| 27 | 0.0 | 0.0 |
| 28f | 0.0 | 0.0 |
| 29 | 0.0 | 0.0 |
| 30 | 0.0 | 0.0 |
| 31 | 0.0 | 0.0 |
| 32 | 0.0 | 0.0 |
| 33 | 0.0 | 0.0 |
| 34 | 0.0 | 0.0 |
| 35 | 0.0 | 0.0 |
| 36 | 0.0 | 0.0 |
| 37 | 0.0 | 0.0 |
| 38 | 0.0 | 0.0 |
| 39 | 0.0 | 0.0 |
| 40 | 0.0 | 0.0 |
| 41 | 0.0 | 0.0 |
| 42 | 0.0 | 0.0 |
| 43 | 0.0 | 0.0 |
| 44 | 0.0 | 0.0 |
| 45 | 0.0 | 0.0 |
| 46 | 0.0 | 0.0 |
| 47 | 0.0 | 0.0 |
| 48 | 0.0 | 0.0 |
| 49 | 0.0 | 0.0 |
| 50 | 0.0 | 0.0 |
| 51 | 0.0 | 0.0 |
| 52 | 0.0 | 0.0 |
| 53f | 0.0 | 0.0 |
| 54 | 0.0 | 0.0 |
| 55 | 0.0 | 0.0 |
| 56 | 0.0 | 0.0 |
| 57 | 0.0 | 0.0 |
| 58 | 0.0 | 0.0 |
| 59 | 0.0 | 0.0 |
| 60 | 0.0 | 0.0 |
| 61 | 0.0 | 0.0 |
| 62 | 0.0 | 0.0 |
| 63 | 0.0 | 0.0 |
| 64 | 0.0 | 0.0 |
| 65 | 0.0 | 0.0 |
| 66f | 0.0 | 0.0 |
| 67 | 0.0 | 0.0 |
| 68 | 0.0 | 0.0 |
| 69 | 0.0 | 0.0 |
| 70 | 0.0 | 0.0 |
| 71 | 0.0 | 0.0 |
| 72 | 0.0 | 0.0 |
| 73 | 0.0 | 0.0 |
| 74 | 0.0 | 0.0 |
| 75 | 0.0 | 0.0 |
| 76 | 0.0 | 0.0 |
| 77 | 0.0 | 0.0 |
| 78 | 0.0 | 0.0 |

| CHIP 1 | | |
|--------|-----|-----|
| CH | M | STD |
| 0r | 0.0 | 0.0 |
| 1r | 0.0 | 0.0 |
| 2r | 0.0 | 0.0 |
| 3 | 0.0 | 0.0 |
| 4 | 0.0 | 0.0 |
| 5 | 0.0 | 0.0 |
| 6 | 0.0 | 0.0 |
| 7 | 0.0 | 0.0 |
| 8 | 0.0 | 0.0 |
| 9 | 0.0 | 0.0 |
| 10 | 0.0 | 0.0 |
| 11 | 0.0 | 0.0 |
| 12 | 0.0 | 0.0 |
| 13 | 0.0 | 0.0 |
| 14 | 0.0 | 0.0 |
| 15f | 0.0 | 0.0 |
| 16 | 0.0 | 0.0 |
| 17 | 0.0 | 0.0 |
| 18 | 0.0 | 0.0 |
| 19 | 0.0 | 0.0 |
| 20 | 0.0 | 0.0 |
| 21 | 0.0 | 0.0 |
| 22 | 0.0 | 0.0 |
| 23 | 0.0 | 0.0 |
| 24 | 0.0 | 0.0 |
| 25 | 0.0 | 0.0 |
| 26 | 0.0 | 0.0 |
| 27 | 0.0 | 0.0 |
| 28f | 0.0 | 0.0 |
| 29 | 0.0 | 0.0 |
| 30 | 0.0 | 0.0 |
| 31 | 0.0 | 0.0 |
| 32 | 0.0 | 0.0 |
| 33 | 0.0 | 0.0 |
| 34 | 0.0 | 0.0 |
| 35 | 0.0 | 0.0 |
| 36 | 0.0 | 0.0 |
| 37 | 0.0 | 0.0 |
| 38 | 0.0 | 0.0 |
| 39 | 0.0 | 0.0 |
| 40 | 0.0 | 0.0 |
| 41 | 0.0 | 0.0 |
| 42 | 0.0 | 0.0 |
| 43 | 0.0 | 0.0 |
| 44 | 0.0 | 0.0 |
| 45 | 0.0 | 0.0 |
| 46 | 0.0 | 0.0 |
| 47 | 0.0 | 0.0 |
| 48 | 0.0 | 0.0 |
| 49 | 0.0 | 0.0 |
| 50 | 0.0 | 0.0 |
| 51 | 0.0 | 0.0 |
| 52 | 0.0 | 0.0 |
| 53f | 0.0 | 0.0 |
| 54 | 0.0 | 0.0 |
| 55 | 0.0 | 0.0 |
| 56 | 0.0 | 0.0 |
| 57 | 0.0 | 0.0 |
| 58 | 0.0 | 0.0 |
| 59 | 0.0 | 0.0 |
| 60 | 0.0 | 0.0 |
| 61 | 0.0 | 0.0 |
| 62 | 0.0 | 0.0 |
| 63 | 0.0 | 0.0 |
| 64 | 0.0 | 0.0 |
| 65 | 0.0 | 0.0 |
| 66f | 0.0 | 0.0 |
| 67 | 0.0 | 0.0 |
| 68 | 0.0 | 0.0 |
| 69 | 0.0 | 0.0 |