

Fec test report:

Date: 2022-02-24 16:53:29

Tester name: Vlada

Test#1 Monitoring values

Passed

| | | | |
|---|--------------------------------|------------------|----|
| 0 | FEC label | 065 | OK |
| 1 | FEC DC2438 ID | 750000024d97f626 | OK |
| 2 | FEC_T (to 35°C) | 22.469 | OK |
| 3 | FEC_Vdd (3.2V to 3.4V) | 3.290 | OK |
| 4 | FEC_I (ref 1.592A , high 2.0A) | 1.592 | OK |
| 5 | FEC_Vad (1.9V to 2.0V) | 1.950 | OK |

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

| | | | | |
|---|---------------|---------|-----------|----|
| 0 | After chip #0 | Mean OK | STDDEV OK | OK |
| 1 | After chip #1 | Mean OK | STDDEV OK | OK |
| 2 | After chip #2 | Mean OK | STDDEV OK | OK |
| 3 | After chip #3 | Mean OK | STDDEV OK | OK |
| 4 | After chip #4 | Mean OK | STDDEV OK | OK |
| 5 | After chip #5 | Mean OK | STDDEV OK | OK |
| 6 | After chip #6 | Mean OK | STDDEV OK | OK |
| 7 | After chip #7 | Mean OK | STDDEV OK | OK |

Test#4 AD9637 test patterns

Passed

| | | | | |
|---|----------------|----------------------------------------|-------------------|----|
| 0 | ADC channel #0 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 1 | ADC channel #1 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 2 | ADC channel #2 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 3 | ADC channel #3 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |
| 4 | ADC channel #4 | P#1 (Midscale short 2048) | MAX 2048 MIN 2048 | OK |
| 5 | ADC channel #5 | P#2 (+Full-scale short 4095) | MAX 4095 MIN 4095 | OK |
| 6 | ADC channel #6 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 7 | ADC channel #7 | P#7 (One/zero-word toggle) | MAX 4095 MIN 0 | OK |

Test#5 Pulser run

Passed

| | | | | |
|---|---------------|-----------------------------------|----------------|----|
| 0 | After chip #0 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3115 | OK |
| 1 | After chip #1 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3057 | OK |
| 2 | After chip #2 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2995 | OK |
| 3 | After chip #3 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3077 | OK |
| 4 | After chip #4 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3108 | OK |
| 5 | After chip #5 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3001 | OK |
| 6 | After chip #6 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3037 | OK |
| 7 | After chip #7 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3021 | OK |

FEC test final result:

Passed

| Monitoring test | | | |
|-----------------|---------------------------|-------|------------------------------------------------|
| NO | Command | Error | Response |
| 0 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 1 | fe 0 moni T 0 | 0 | 0 Tdcm(2) Fem(00) FEC_T: 22.469 degC |
| 2 | fe 0 moni V 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V |
| 3 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 4 | fe 0 pulser 0 base 0x3FFF | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 5 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 6 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 7 | fe 0 moni I 0 | 0 | 0 Tdcm(2) Fem(00) FEC_I: 0.796 A |
| 8 | fe 0 moni S 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Serial: 750000024d97f626 |

| Slow control registers test | | | |
|-----------------------------|----------------------------------------|-------|------------------------------------------------------------------------|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe fec_enable 1 | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x40000 |
| 2 | fe fec_enable | 0 | 0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1 |
| 3 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 4 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 5 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 6 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 7 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 8 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 9 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 10 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 11 | fe 0 after 0 wrchk 3 0x0 0x0101 0x0101 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified) |
| 12 | fe 0 after 1 wrchk 3 0x0 0x0202 0x0202 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified) |
| 13 | fe 0 after 2 wrchk 3 0x0 0x0303 0x0303 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified) |
| 14 | fe 0 after 3 wrchk 3 0x0 0x0404 0x0404 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified) |
| 15 | fe 0 after 4 wrchk 3 0x0 0x0505 0x0505 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified) |
| 16 | fe 0 after 5 wrchk 3 0x0 0x0606 0x0606 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified) |
| 17 | fe 0 after 6 wrchk 3 0x0 0x0707 0x0707 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified) |
| 18 | fe 0 after 7 wrchk 3 0x0 0x0808 0x0808 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified) |
| 19 | fe 0 after 0 read 3 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101 |
| 20 | fe 0 after 1 read 3 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202 |
| 21 | fe 0 after 2 read 3 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303 |
| 22 | fe 0 after 3 read 3 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404 |
| 23 | fe 0 after 4 read 3 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505 |
| 24 | fe 0 after 5 read 3 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606 |
| 25 | fe 0 after 6 read 3 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707 |
| 26 | fe 0 after 7 read 3 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808 |
| 27 | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 28 | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 29 | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 30 | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 31 | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 32 | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 33 | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |
| 34 | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified) |

| ADC pattern test | | | |
|------------------|--------------------------|-------|-----------------------------------------------------------------------------------|
| NO | Command | Error | Response |
| 0 | fe 0 mode after | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x400 |
| 1 | fe 0 test_mode | 0 | 0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0 |
| 2 | be 0 state eb | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current |
| 3 | be 0 state tg | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG) |
| 4 | be 0 state pm | 0 | 0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 5 | fe 0 state | 0 | 0 Tdcm(2) Fem(00) State = 0x3 (Aligned SCA_Write) |
| 6 | daq 0xFFFF F | 0 | 0 Tdcm(2): daq paused |
| 7 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 8 | fe 0 emit_empty_ch 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdcm(2) Fem(00) Reg(5) <- 0x0 |
| 10 | fe 0 keep_rst 0 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x0 |
| 11 | fe 0 skip_rst 2 | 0 | 0 Tdcm(2) Fem(00) Reg(0) <- 0x40000 |
| 12 | fe adc 0 model AD9637 | 0 | 0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637) |
| 13 | fe adc 0 write 0x14 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0) |
| 14 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 15 | fe adc 0 write 0x5 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1) |
| 16 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 17 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 18 | fe adc 0 write 0x5 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2) |
| 19 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 20 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |

| | | | |
|----|-------------------------|---|------------------------------------------------------------------------------------|
| 21 | fe adc 0 write 0x5 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4) |
| 22 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 23 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0) |
| 24 | fe adc 0 write 0x5 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8) |
| 25 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 26 | fe adc 0 write 0x4 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1) |
| 27 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 28 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1) |
| 29 | fe adc 0 write 0x4 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2) |
| 30 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 31 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2) |
| 32 | fe adc 0 write 0x4 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4) |
| 33 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 34 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4) |
| 35 | fe adc 0 write 0x4 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8) |
| 36 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0) |
| 37 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7) |
| 38 | fe 0 subtract_ped 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 39 | fe 0 zero_suppress 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 40 | fe 0 zs_pre_post 4 8 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0xc4 |
| 41 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 42 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 43 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 44 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 45 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 46 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 47 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 48 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 49 | be 0 trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x1000 |
| 50 | be 0 trig_ena 0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 51 | be 0 state eb | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current) |
| 52 | be 0 state tg | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS) |
| 53 | be 0 state pm | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE) |
| 54 | fe 0 state | 0 | 0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready) |
| 55 | fe adc 0 write 0x4 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15) |
| 56 | fe adc 0 write 0x5 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15) |
| 57 | fe adc 0 write 0xD 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0) |

| Pulser test | | | |
|-------------|------------------------------------|-------|---------------------------------------------------------------------|
| NO | Command | Error | Response |
| 0 | daq 0xFFFFF F | 0 | 0 Tdc(2): daq paused |
| 1 | fe 0 after 0:7 wrchk 3 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 2 | fe 0 after 0:7 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 3 | fe 0 emit_hit_cnt 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 4 | fe 0 emit_empty_ch 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 5 | fe 0 emit_lst_cell_rd 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 6 | fe 0 keep_rst 0 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0 |
| 7 | fe 0 skip_rst 2 | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000 |
| 8 | fe 0 test_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 9 | fe 0 test_mode 1 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x400 |
| 10 | fe 0 tdata A 0x1FF | 0 | 0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510 |
| 11 | fe 0 test_zbt 0 | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0x0 |
| 12 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 13 | fe 0 asic_mask | 0 | 0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0 |
| 14 | fe 0 pulser 0 enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 15 | fe 0 pulser 0 ft_enable 0 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x0 |
| 16 | fe 0 pulser 0 model T2K2 | 0 | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2) |
| 17 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 18 | fe 0 pulser 0 ampl 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff |
| 19 | fe 0 pulser 0 delay 3000 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0xbb8 |
| 20 | fe pulser load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 21 | fe 0 pulser 0 enable 1 | 0 | 0 Tdc(2) Fem(00) Reg(3) <- 0x10000 |
| 22 | be 0 eb keep_fem_soe 0 | 0 | 0 Tdc(2) Reg(0) <- 0x0 |
| 23 | be 0 eb check_ev_nb 1 | 0 | 0 Tdc(2) Reg(0) <- 0x800000 |
| 24 | be 0 eb check_ev_ts 1 | 0 | 0 Tdc(2) Reg(0) <- 0x1000000 |
| 25 | be 0 eb ts_tolerance 0 | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0 |
| 26 | be 0 event_limit 0x0 | 0 | 0 Tdc(2) Reg(6) <- 0x0 |
| 27 | be 0 trig_rate 0 50 | 0 | 0 Tdc(2) Reg(6) <- 0x32 |
| 28 | be 0 trig_delay 0 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 29 | be 0 trig_delay 1 0 | 0 | 0 Tdc(2) Reg(8) <- 0x0 |
| 30 | be 0 trig_delay 2 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 31 | be 0 trig_delay 3 0 | 0 | 0 Tdc(2) Reg(9) <- 0x0 |
| 32 | be 0 ss_trig_delay 0x4 | 0 | 0 Tdc(2) Reg(14) <- 0x4 |
| 33 | be 0 ss_trig_ena 1 | 0 | 0 Tdc(2) Reg(6) <- 0x10000 |
| 34 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 35 | be 0 restart | 0 | 0 Tdc(2) Reg(5) <- restart done |
| 36 | be 0 isobus 0x0C | 0 | 0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear) |

| | | | |
|-----|------------------------------------------|---|-----------------------------------------------------------------------|
| 37 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 38 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 39 | fe 0 asic_mask 0xfffe | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000 |
| 40 | fe 0 after 0 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration |
| 41 | fe 0 after 0 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 42 | fe 0 after 0 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 43 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 44 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 45 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 46 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 47 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 48 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 49 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 50 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 51 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 52 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 53 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 54 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 55 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 56 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 57 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 58 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 59 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 60 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 61 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 62 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 63 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 64 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 65 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 66 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 67 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 68 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 69 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 70 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 71 | fe 0 asic_mask 0xfffd | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000 |
| 72 | fe 0 after 1 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration |
| 73 | fe 0 after 1 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 74 | fe 0 after 1 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 75 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 76 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 77 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 78 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 79 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 80 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 81 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 82 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 83 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 84 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 85 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 86 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 87 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 88 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 89 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 90 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 91 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 92 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 93 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 94 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 95 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 96 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 97 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 98 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 99 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 100 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 101 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 102 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 103 | fe 0 asic_mask 0xfffb | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000 |
| 104 | fe 0 after 2 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration |
| 105 | fe 0 after 2 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 106 | fe 0 after 2 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 107 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 108 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 109 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 110 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 111 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 112 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 113 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 114 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |

| | | | |
|-----|------------------------------------------|---|-----------------------------------------------------------------------|
| 115 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 116 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 117 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 118 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 119 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 120 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 121 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 122 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 123 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 124 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 125 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 126 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 127 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 128 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 129 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 130 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 131 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 132 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 133 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 134 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 135 | fe 0 asic_mask 0xffff | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000 |
| 136 | fe 0 after 3 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration |
| 137 | fe 0 after 3 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 138 | fe 0 after 3 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 139 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 140 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 141 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 142 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 143 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 144 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 145 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 146 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 147 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 148 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 149 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 150 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 151 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 152 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 153 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 154 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 155 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 156 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 157 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 158 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 159 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 160 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 161 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 162 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 163 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 164 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 165 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 166 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 167 | fe 0 asic_mask 0xffef | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000 |
| 168 | fe 0 after 4 test_mode 0x1 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration |
| 169 | fe 0 after 4 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 170 | fe 0 after 4 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 171 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 172 | fe pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0 |

| | | | |
|-----|------------------------------------------|---|----------------------------------------------------------------------|
| 193 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 194 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 195 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 196 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 197 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 198 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 199 | fe 0 asic_mask 0xffdf | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000 |
| 200 | fe 0 after 5 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration |
| 201 | fe 0 after 5 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 202 | fe 0 after 5 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 203 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 204 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 205 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 206 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 207 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 208 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 209 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 210 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 211 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 212 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 213 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 214 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 215 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 216 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 217 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 218 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 219 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 220 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 221 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 222 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 223 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 224 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 225 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 226 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 227 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 228 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 229 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 230 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 231 | fe 0 asic_mask 0xffbf | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000 |
| 232 | fe 0 after 6 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration |
| 233 | fe 0 after 6 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 234 | fe 0 after 6 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 235 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 236 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 237 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 238 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 239 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 240 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 241 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 242 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 243 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 244 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 245 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 246 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 247 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 248 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 249 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 250 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 251 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 252 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 253 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 254 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 255 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 256 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 257 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 258 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 259 | be 0 isobus 0x60 | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 260 | fe 0 asic_mask 0x0 | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0 |
| 261 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 262 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 263 | fe 0 asic_mask 0xff7f | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000 |
| 264 | fe 0 after 7 test_mode 0x1 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration |
| 265 | fe 0 after 7 wrchk 3 0x0 0x1000 0x0 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 266 | fe 0 after 7 wrchk 4 0x0 0x0 0x0 | 0 | 0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified) |
| 267 | fe 0 pulser 0 base 16383 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff |
| 268 | fe pulser 0 load | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 269 | fe 0 moni A 0 | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V |
| 270 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c |

| | | | |
|-----|--------------------------|---|------------------------------------------------------------------|
| 271 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 272 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 273 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 274 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 275 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 276 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 277 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 278 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 279 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 280 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 281 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 282 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 283 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 284 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 285 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 286 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 287 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff |
| 288 | fe 0 pulser 0 load | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed |
| 289 | fe 0 moni A 0 | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V |
| 290 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c |
| 291 | be 0 isobus 0x60 | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear) |
| 292 | fe 0 asic_mask 0x0 | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0 |
| 293 | be 0 trig_ena 0 | 0 | 0 Tdcm(2) Reg(6) <- 0x0 |

Pedestal data before centermean

| CHIP 0 | | | CHIP 1 | | | CHIP 2 | | | CHIP 3 | | | CHIP 4 | | | CHIP 5 | | | CHIP 6 | | | CHIP 7 | | |
|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|------|--------|-------|-----|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 | 0 r | 0.0 | 0.0 |
| 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 510.1 | 2.1 | 1 r | 508.7 | 4.3 | 1 r | 511.0 | 0.0 | 1 r | 511.0 | 0.0 | 1 r | 495.7 | 10.0 | 1 r | 511.0 | 0.0 |
| 2 r | 267.7 | 0.7 | 2 r | 329.7 | 0.7 | 2 r | 282.1 | 0.7 | 2 r | 289.1 | 0.7 | 2 r | 302.4 | 0.7 | 2 r | 275.4 | 0.7 | 2 r | 285.2 | 0.7 | 2 r | 268.5 | 0.7 |
| 3 | 238.5 | 5.0 | 3 | 370.2 | 4.9 | 3 | 223.2 | 4.8 | 3 | 221.4 | 5.1 | 3 | 325.0 | 5.7 | 3 | 272.5 | 5.1 | 3 | 228.1 | 5.1 | 3 | 221.1 | 5.1 |
| 4 | 262.0 | 4.5 | 4 | 367.5 | 4.3 | 4 | 277.9 | 4.3 | 4 | 233.9 | 4.7 | 4 | 222.2 | 5.3 | 4 | 206.8 | 4.9 | 4 | 214.2 | 4.9 | 4 | 313.5 | 4.8 |
| 5 | 294.6 | 5.0 | 5 | 260.1 | 4.5 | 5 | 230.8 | 4.5 | 5 | 201.1 | 5.1 | 5 | 293.1 | 5.4 | 5 | 226.6 | 4.8 | 5 | 276.8 | 5.0 | 5 | 295.0 | 5.1 |
| 6 | 274.1 | 4.7 | 6 | 252.1 | 4.3 | 6 | 208.4 | 4.6 | 6 | 280.6 | 4.7 | 6 | 219.1 | 5.1 | 6 | 202.6 | 4.7 | 6 | 246.8 | 4.6 | 6 | 231.0 | 4.9 |
| 7 | 248.9 | 4.7 | 7 | 292.2 | 4.6 | 7 | 264.9 | 4.3 | 7 | 174.1 | 4.9 | 7 | 204.5 | 5.1 | 7 | 243.4 | 5.0 | 7 | 300.0 | 4.7 | 7 | 301.3 | 5.1 |
| 8 | 285.9 | 4.7 | 8 | 310.6 | 4.4 | 8 | 183.0 | 4.6 | 8 | 265.2 | 4.7 | 8 | 229.6 | 5.1 | 8 | 231.4 | 4.6 | 8 | 228.6 | 4.7 | 8 | 195.8 | 4.8 |
| 9 | 283.5 | 5.1 | 9 | 340.5 | 4.6 | 9 | 248.6 | 4.5 | 9 | 310.5 | 5.0 | 9 | 143.8 | 5.0 | 9 | 245.9 | 4.7 | 9 | 208.9 | 4.9 | 9 | 199.6 | 4.9 |
| 10 | 212.9 | 4.2 | 10 | 358.6 | 4.3 | 10 | 230.4 | 4.2 | 10 | 227.8 | 4.4 | 10 | 151.6 | 5.0 | 10 | 181.7 | 4.8 | 10 | 258.9 | 4.7 | 10 | 163.3 | 4.7 |
| 11 | 264.4 | 4.8 | 11 | 400.5 | 4.7 | 11 | 320.3 | 4.3 | 11 | 254.0 | 4.6 | 11 | 174.0 | 5.0 | 11 | 213.1 | 4.6 | 11 | 229.9 | 4.8 | 11 | 225.0 | 5.1 |
| 12 | 212.0 | 4.5 | 12 | 270.3 | 4.5 | 12 | 199.0 | 4.2 | 12 | 294.8 | 4.5 | 12 | 248.6 | 4.9 | 12 | 213.7 | 4.7 | 12 | 244.4 | 4.6 | 12 | 265.3 | 4.9 |
| 13 | 232.0 | 4.9 | 13 | 343.4 | 4.2 | 13 | 242.3 | 4.5 | 13 | 222.8 | 4.7 | 13 | 187.2 | 5.1 | 13 | 233.7 | 4.7 | 13 | 273.1 | 4.8 | 13 | 227.6 | 4.7 |
| 14 | 181.0 | 4.6 | 14 | 306.9 | 4.5 | 14 | 232.9 | 4.5 | 14 | 240.3 | 4.3 | 14 | 177.4 | 5.2 | 14 | 187.6 | 4.9 | 14 | 202.0 | 4.7 | 14 | 170.0 | 4.9 |
| 15 f | 216.2 | 1.7 | 15 f | 291.6 | 1.7 | 15 f | 289.2 | 1.7 | 15 f | 253.2 | 1.6 | 15 f | 203.8 | 1.6 | 15 f | 263.0 | 1.7 | 15 f | 302.2 | 1.7 | 15 f | 246.6 | 1.7 |
| 16 | 166.7 | 4.8 | 16 | 281.2 | 4.5 | 16 | 266.5 | 4.5 | 16 | 189.5 | 4.8 | 16 | 206.8 | 4.8 | 16 | 282.6 | 4.5 | 16 | 255.4 | 4.6 | 16 | 214.0 | 4.8 |
| 17 | 244.9 | 4.2 | 17 | 317.8 | 4.4 | 17 | 241.4 | 4.3 | 17 | 233.6 | 4.6 | 17 | 195.2 | 5.0 | 17 | 186.5 | 4.5 | 17 | 254.2 | 4.6 | 17 | 263.3 | 4.8 |
| 18 | 269.3 | 4.6 | 18 | 350.6 | 4.7 | 18 | 271.3 | 4.5 | 18 | 163.1 | 4.8 | 18 | 305.4 | 4.9 | 18 | 222.2 | 4.5 | 18 | 248.7 | 4.5 | 18 | 168.3 | 4.3 |
| 19 | 230.8 | 4.4 | 19 | 381.2 | 4.4 | 19 | 230.2 | 4.0 | 19 | 235.3 | 4.7 | 19 | 267.2 | 5.1 | 19 | 245.1 | 4.6 | 19 | 224.9 | 4.7 | 19 | 222.4 | 4.5 |
| 20 | 236.6 | 4.7 | 20 | 284.8 | 4.3 | 20 | 311.1 | 4.4 | 20 | 236.0 | 4.6 | 20 | 199.5 | 4.8 | 20 | 221.6 | 4.4 | 20 | 241.4 | 4.9 | 20 | 213.8 | 4.8 |
| 21 | 272.0 | 4.5 | 21 | 279.9 | 4.2 | 21 | 238.3 | 4.3 | 21 | 251.8 | 4.5 | 21 | 260.6 | 5.0 | 21 | 249.1 | 4.5 | 21 | 277.2 | 4.5 | 21 | 224.5 | 4.8 |
| 22 | 179.9 | 4.7 | 22 | 326.7 | 4.3 | 22 | 284.3 | 4.3 | 22 | 246.2 | 4.7 | 22 | 132.7 | 4.9 | 22 | 181.0 | 4.7 | 22 | 223.4 | 4.4 | 22 | 160.1 | 4.7 |
| 23 | 249.2 | 4.5 | 23 | 348.6 | 4.2 | 23 | 261.7 | 4.1 | 23 | 270.1 | 4.4 | 23 | 267.9 | 4.8 | 23 | 321.3 | 4.6 | 23 | 257.6 | 4.6 | 23 | 226.8 | 4.7 |
| 24 | 243.0 | 5.1 | 24 | 323.7 | 4.5 | 24 | 176.1 | 4.5 | 24 | 235.0 | 4.4 | 24 | 244.4 | 4.8 | 24 | 250.2 | 4.8 | 24 | 295.2 | 4.7 | 24 | 260.5 | 4.7 |
| 25 | 254.8 | 4.7 | 25 | 319.9 | 4.4 | 25 | 260.5 | 4.2 | 25 | 216.4 | 4.6 | 25 | 194.4 | 5.0 | 25 | 354.7 | 4.6 | 25 | 205.4 | 4.6 | 25 | 213.1 | 4.8 |
| 26 | 193.5 | 4.4 | 26 | 289.5 | 4.3 | 26 | 208.2 | 4.2 | 26 | 215.1 | 4.5 | 26 | 208.5 | 4.6 | 26 | 306.9 | 4.7 | 26 | 204.8 | 4.4 | 26 | 293.6 | 4.6 |
| 27 | 269.5 | 4.3 | 27 | 339.0 | 4.3 | 27 | 276.0 | 4.3 | 27 | 204.1 | 4.5 | 27 | 227.2 | 4.8 | 27 | 271.4 | 4.4 | 27 | 261.0 | 4.5 | 27 | 160.4 | 4.8 |
| 28 f | 180.5 | 1.8 | 28 f | 284.0 | 1.8 | 28 f | 201.6 | 1.7 | 28 f | 211.6 | 1.7 | 28 f | 172.9 | 1.7 | 28 f | 229.9 | 1.7 | 28 f | 263.9 | 1.9 | 28 f | 180.5 | 1.8 |
| 29 | 261.4 | 4.7 | 29 | 355.3 | 4.4 | 29 | 329.1 | 4.3 | 29 | 304.0 | 4.5 | 29 | 213.4 | 4.9 | 29 | 275.4 | 4.7 | 29 | 187.0 | 4.7 | 29 | 182.1 | 4.7 |
| 30 | 194.9 | 4.3 | 30 | 332.6 | 4.2 | 30 | 147.0 | 4.1 | 30 | 266.9 | 4.3 | 30 | 231.3 | 4.8 | 30 | 218.9 | 4.6 | 30 | 204.3 | 4.6 | 30 | 186.6 | 5.0 |
| 31 | 270.3 | 4.7 | 31 | 400.6 | 4.7 | 31 | 200.7 | 4.4 | 31 | 194.3 | 4.9 | 31 | 226.2 | 4.8 | 31 | 236.6 | 4.4 | 31 | 245.4 | 4.4 | 31 | 235.2 | 4.7 |
| 32 | 173.7 | 4.4 | 32 | 281.2 | 4.3 | 32 | 258.6 | 4.0 | 32 | 293.2 | 4.2 | 32 | 203.8 | 5.0 | 32 | 311.7 | 4.7 | 32 | 264.6 | 4.5 | 32 | 129.8 | 4.9 |
| 33 | 215.6 | 4.7 | 33 | 269.4 | 4.3 | 33 | 242.5 | 4.3 | 33 | 239.3 | 4.6 | 33 | 243.1 | 4.8 | 33 | 261.4 | 4.5 | 33 | 241.0 | 4.7 | 33 | 188.3 | 4.6 |
| 34 | 192.0 | 4.4 | 34 | 279.3 | 4.1 | 34 | 258.5 | 4.2 | 34 | 219.6 | 4.6 | 34 | 200.0 | 4.8 | 34 | 269.1 | 4.6 | 34 | 193.8 | 4.4 | 34 | 150.4 | 4.7 |
| 35 | 154.9 | 4.5 | 35 | 334.1 | 5.1 | 35 | 238.8 | 4.2 | 35 | 223.7 | 4.6 | 35 | 199.1 | 4.8 | 35 | 220.2 | 4.5 | 35 | 110.4 | 4.9 | 35 | 232.8 | 4.7 |
| 36 | 256.1 | 4.1 | 36 | 294.3 | 4.2 | 36 | 288.8 | 4.1 | 36 | 221.6 | 4.4 | 36 | 140.9 | 5.0 | 36 | 198.0 | 4.6 | 36 | 298.0 | 4.7 | 36 | 191.5 | 5.0 |
| 37 | 291.6 | 4.5 | 37 | 255.9 | 4.5 | 37 | 240.5 | 4.9 | 37 | 224.8 | 4.5 | 37 | 229.4 | 4.8 | 37 | 291.4 | 4.6 | 37 | 187.4 | 4.5 | 37 | 232.1 | 4.5 |
| 38 | 163.1 | 4.4 | 38 | 265.5 | 4.1 | 38 | 203.9 | 4.2 | 38 | 184.9 | 4.4 | 38 | 236.4 | 4.9 | 38 | 189.9 | 4.8 | 38 | 200.9 | 4.6 | 38 | 210.4 | 4.9 |
| 39 | 195.8 | 4.6 | 39 | 381.2 | 4.7 | 39 | 292.3 | 4.3 | 39 | 303.4 | 4.9 | 39 | 230.6 | 5.2 | 39 | 215.6 | 4.8 | 39 | 281.1 | 5.3 | 39 | 210.6 | 5.2 |
| 40 | 284.0 | 4.7 | 40 | 395.3 | 4.2 | 40 | 260.4 | 4.0 | 40 | 246.4 | 4.3 | 40 | 244.5 | 5.0 | 40 | 282.6 | 4.7 | 40 | 214.1 | 4.6 | 40 | 130.6 | 4.9 |
| 41 | 239.9 | 4.1 | 41 | 266.2 | 3.9 | 41 | 255.2 | 3.8 | 41 | 259.6 | 4.0 | 41 | 247.3 | 4.2 | 41 | 252.4 | 4.2 | 41 | 203.5 | 4.2 | 41 | 287.7 | 4.3 |
| 42 | 267.8 | 4.4 | 42 | 304.9 | 4.1 | 42 | 243.4 | 4.2 | 42 | 337.4 | 4.2 | 42 | 298.4 | 4.4 | 42 | 207.3 | 4.1 | 42 | 182.6 | 4.2 | 42 | 187.6 | 4.8 |
| 43 | 267.1 | 4.1 | 43 | 312.6 | 4.0 | 43 | 333.3 | 4.1 | 43 | 278.4 | 4.1 | 43 | 230.0 | 4.2 | 43 | 244.6 | 4.1 | 43 | 286.1 | 4.1 | 43 | 224.5 | 4.4 |
| 44 | 231.3 | 4.4 | 44 | 307.1 | 4.0 | 44 | 323.2 | 3.9 | 44 | 301.6 | 4.1 | 44 | 276.2 | 4.4 | 44 | 261.2 | 4.2 | 44 | 250.0 | 4.0 | 44 | 196.1 | 4.6 |
| 45 | 188.0 | 4.1 | 45 | 400.5 | 3.9 | 45 | 236.7 | 3.8 | 45 | 263.9 | 4.0 | 45 | 226.4 | 4.3 | 45 | 185.1 | 4.1 | 45 | 271.0 | 4.1 | 45 | 192.5 | 4.5 |
| 46 | 274.9 | 4.2 | 46 | 346.6 | 4.1 | 46 | 190.2 | 3.9 | 46 | 238.0 | 4.1 | 46 | 244.8 | 4.3 | 46 | 237.8 | 4.3 | 46 | 185.7 | 4.4 | 46 | 223.7 | 4.6 |
| 47 | 237.1 | 4.1 | 47 | 328.3 | 4.1 | 47 | 303.2 | 4.1 | 47 | 309.5 | 4.0 | 47 | 204.9 | 4.2 | 47 | 236.3 | 4.2 | 47 | 234.1 | 3.9 | 47 | 214.1 | 4.4 |
| 48 | 159.8 | 4.4 | 48 | 357.8 | 4.0 | 48 | 258.3 | 4.0 | 48 | 265.2 | 3.9 | 48 | 171.3 | 4.4 | 48 | 169.2 | 4.0 | 48 | 203.5 | 4.2 | 48 | 184.8 | 4.8 |
| 49 | 284.1 | 4.3 | 49 | 258.0 | 3.9 | 49 | 252.6 | 4.0 | 49 | 210.5 | 4.0 | 49 | 183.9 | 4.3 | 49 | 229.4 | 4.0 | 49 | 238.7 | 4.2 | 49 | 218.0 | 4.4 |
| 50 | 187.6 | 4.5 | 50 | 311.5 | 4.0 | 50 | 215.3 | 3.9 | 50 | 235.9 | 4.2 | 50 | 142.1 | 4.3 | 50 | 285.2 | 4.2 | 50 | 237.8 | 4.5 | 50 | 190.8 | 4.4 |
| 51 | 198.5 | 4.3 | 51 | 293.4 | 3.7 | 51 | 244.1 | 3.8 | 51 | 217.7 | 4.0 | 51 | 197.6 | 4.3 | 51 | 223.8 | 4.0 | 51 | 271.1 | 4.2 | 51 | 234.3 | 4.5 |
| 52 | 181.2 | 4.3 | 52 | 256.0 | 3.9 | 52 | 248.0 | 4.3 | 52 | 233.2 | 4.0 | 52 | 246.8 | 4.5 | 52 | 177.4 | 4.0 | 52 | 285.2 | 4.1 | 52 | 300.0 | 4.5 |
| 53 f | 236.4 | 1.6 | 53 f | 347.9 | 1.4 | 53 f | 274.7 | 1.5 | 53 f | 257.9 | 1.6 | 53 f | 285.6 | 1.5 | 53 f | 247.3 | 1.4 | 53 f | 282.7 | 1.5 | 53 f | 127.0 | 1.5 |
| 54 | 216.9 | 4.4 | 54 | 338.4 | 3.8 | 54 | 233.3 | 4.0 | 54 | 243.4 | 4.3 | 54 | 226.1 | 4.3 | 54 | 160.1 | 4.0 | 54 | 190.9 | 4.1 | 54 | 165.2 | 4.1 |
| 55 | 260.1 | 4.3 | 55 | 280.3 | 3.9 | 55 | 260.6 | 4.2 | 55 | 278.4 | 4.0 | 55 | 188.3 | 4.3 | 55 | 255.6 | 4.2 | 55 | 310.2 | 4.3 | 55 | 271.1 | 4.4 |
| 56 | 150.8 | 4.1 | 56 | 254.9 | 4.1 | 56 | 206.8 | 4.1 | 56 | 215.4 | 4.0 | 56 | 230.8 | 4.2 | 56 | 221.5 | 4.1 | 56 | 200.6 | 4.3 | 56 | 218.3 | 4.3 |
| 57 | 273.2 | 4.5 | 57 | 365.6 | 4.0 | 57 | 272.2 | 4.2 | 57 | 233.4 | 4.2 | 57 | 237.8 | 4.2 | 57 | 278.0 | 4.2 | 57 | 225.0 | 4.1 | 57 | 176.9 | 4.6 |
| 58 | 260.5 | 4.1 | 58 | 352.3 | 3.8 | 58 | 254.3 | 3.9 | 58 | 211.6 | 4.0 | 58 | 132.5 | 4. | | | | | | | | | |

Pedestal after centermean.

| CHIP 0 | | | CHIP 1 | | | CHIP 2 | | | CHIP 3 | | | CHIP 4 | | | CHIP 5 | | | CHIP 6 | | | CHIP 7 | | |
|--------|-------|------|--------|-------|-----|--------|-------|-----|--------|-------|------|--------|-------|-----|--------|-------|-----|--------|-------|------|--------|-------|-----|
| CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD | CH | M | STD |
| 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 | 0 r | 250.0 | 0.0 |
| 1 r | 326.4 | 10.6 | 1 r | 416.6 | 8.9 | 1 r | 262.8 | 9.7 | 1 r | 263.5 | 12.6 | 1 r | 504.4 | 4.7 | 1 r | 319.2 | 8.9 | 1 r | 250.5 | 11.2 | 1 r | 283.3 | 9.8 |
| 2 r | 249.9 | 0.7 | 2 r | 249.7 | 0.6 | 2 r | 250.0 | 0.6 | 2 r | 250.3 | 0.7 | 2 r | 250.1 | 0.7 | 2 r | 250.2 | 0.7 | 2 r | 250.2 | 0.7 | 2 r | 250.7 | 0.7 |
| 3 | 249.4 | 5.5 | 3 | 250.1 | 5.1 | 3 | 249.7 | 4.9 | 3 | 252.2 | 5.6 | 3 | 248.9 | 6.5 | 3 | 248.6 | 5.5 | 3 | 250.0 | 5.5 | 3 | 250.8 | 5.6 |
| 4 | 250.5 | 4.6 | 4 | 250.4 | 4.2 | 4 | 250.1 | 4.4 | 4 | 250.1 | 4.9 | 4 | 250.8 | 6.1 | 4 | 249.6 | 4.9 | 4 | 249.8 | 5.2 | 4 | 249.5 | 5.0 |
| 5 | 249.4 | 5.2 | 5 | 250.9 | 4.8 | 5 | 249.7 | 4.7 | 5 | 250.2 | 5.4 | 5 | 248.6 | 6.0 | 5 | 249.8 | 5.1 | 5 | 250.2 | 5.0 | 5 | 250.7 | 5.4 |
| 6 | 250.9 | 4.7 | 6 | 249.9 | 4.3 | 6 | 250.8 | 4.2 | 6 | 250.4 | 4.9 | 6 | 249.4 | 5.7 | 6 | 249.2 | 4.9 | 6 | 248.1 | 4.9 | 6 | 249.3 | 5.3 |
| 7 | 250.9 | 5.3 | 7 | 251.5 | 4.8 | 7 | 248.3 | 4.5 | 7 | 249.4 | 5.5 | 7 | 250.1 | 6.0 | 7 | 249.7 | 4.8 | 7 | 250.8 | 5.2 | 7 | 250.7 | 5.3 |
| 8 | 248.7 | 4.5 | 8 | 248.8 | 4.4 | 8 | 250.5 | 4.6 | 8 | 250.2 | 4.7 | 8 | 248.9 | 5.6 | 8 | 250.0 | 4.8 | 8 | 249.4 | 4.9 | 8 | 249.6 | 4.9 |
| 9 | 250.9 | 5.1 | 9 | 250.8 | 4.6 | 9 | 249.2 | 4.9 | 9 | 249.7 | 5.1 | 9 | 250.7 | 5.5 | 9 | 249.5 | 5.1 | 9 | 250.2 | 5.0 | 9 | 249.8 | 5.3 |
| 10 | 250.5 | 4.5 | 10 | 249.7 | 4.5 | 10 | 251.2 | 4.1 | 10 | 250.2 | 4.6 | 10 | 251.2 | 5.8 | 10 | 248.8 | 4.9 | 10 | 249.8 | 5.1 | 10 | 250.8 | 5.3 |
| 11 | 250.0 | 5.0 | 11 | 251.7 | 4.8 | 11 | 249.8 | 4.6 | 11 | 250.0 | 5.0 | 11 | 249.2 | 5.7 | 11 | 250.1 | 4.8 | 11 | 249.3 | 4.8 | 11 | 250.8 | 5.0 |
| 12 | 249.6 | 4.6 | 12 | 250.9 | 4.2 | 12 | 251.2 | 4.1 | 12 | 250.4 | 4.6 | 12 | 250.5 | 5.7 | 12 | 249.3 | 4.8 | 12 | 251.5 | 4.7 | 12 | 251.6 | 5.2 |
| 13 | 250.9 | 5.1 | 13 | 253.2 | 4.7 | 13 | 250.6 | 4.6 | 13 | 250.5 | 5.0 | 13 | 251.8 | 5.7 | 13 | 250.4 | 5.2 | 13 | 250.8 | 5.0 | 13 | 250.8 | 5.3 |
| 14 | 251.3 | 4.4 | 14 | 249.9 | 4.6 | 14 | 250.2 | 4.2 | 14 | 250.4 | 4.7 | 14 | 250.7 | 5.6 | 14 | 249.3 | 5.1 | 14 | 251.2 | 5.0 | 14 | 250.6 | 5.0 |
| 15 f | 250.2 | 1.7 | 15 f | 249.0 | 1.7 | 15 f | 250.5 | 1.7 | 15 f | 250.5 | 1.8 | 15 f | 250.0 | 1.7 | 15 f | 249.6 | 1.7 | 15 f | 250.0 | 1.6 | 15 f | 250.2 | 1.6 |
| 16 | 250.8 | 5.0 | 16 | 251.2 | 4.6 | 16 | 250.1 | 4.3 | 16 | 250.1 | 4.9 | 16 | 250.5 | 5.3 | 16 | 249.4 | 4.8 | 16 | 251.0 | 5.0 | 16 | 250.7 | 5.1 |
| 17 | 250.3 | 4.5 | 17 | 249.7 | 4.3 | 17 | 249.8 | 4.5 | 17 | 251.3 | 4.6 | 17 | 250.5 | 5.6 | 17 | 251.2 | 4.9 | 17 | 250.8 | 4.8 | 17 | 250.1 | 5.0 |
| 18 | 251.0 | 4.8 | 18 | 248.8 | 4.6 | 18 | 250.8 | 4.5 | 18 | 251.5 | 5.0 | 18 | 250.2 | 5.4 | 18 | 249.4 | 4.8 | 18 | 250.3 | 5.1 | 18 | 250.5 | 4.9 |
| 19 | 251.9 | 4.5 | 19 | 250.6 | 4.4 | 19 | 251.0 | 4.3 | 19 | 250.9 | 4.7 | 19 | 251.4 | 5.5 | 19 | 251.0 | 5.0 | 19 | 249.2 | 4.8 | 19 | 251.2 | 4.8 |
| 20 | 250.7 | 4.5 | 20 | 251.2 | 4.5 | 20 | 250.7 | 4.5 | 20 | 250.5 | 5.0 | 20 | 249.7 | 5.2 | 20 | 251.2 | 4.7 | 20 | 249.2 | 4.8 | 20 | 249.9 | 4.9 |
| 21 | 250.4 | 4.7 | 21 | 251.3 | 4.4 | 21 | 250.7 | 4.2 | 21 | 249.8 | 4.7 | 21 | 250.4 | 5.5 | 21 | 249.8 | 4.9 | 21 | 249.4 | 4.8 | 21 | 250.6 | 5.0 |
| 22 | 250.7 | 4.8 | 22 | 248.4 | 4.4 | 22 | 249.9 | 4.7 | 22 | 250.3 | 4.7 | 22 | 250.8 | 5.5 | 22 | 249.4 | 4.9 | 22 | 251.1 | 4.8 | 22 | 251.0 | 4.8 |
| 23 | 251.2 | 4.4 | 23 | 249.6 | 4.3 | 23 | 250.0 | 4.0 | 23 | 249.8 | 4.5 | 23 | 250.2 | 5.4 | 23 | 249.8 | 4.7 | 23 | 249.7 | 4.8 | 23 | 249.7 | 5.2 |
| 24 | 250.6 | 4.6 | 24 | 250.1 | 4.4 | 24 | 250.7 | 4.3 | 24 | 250.9 | 4.7 | 24 | 250.2 | 5.3 | 24 | 250.3 | 4.9 | 24 | 249.5 | 5.0 | 24 | 251.0 | 5.1 |
| 25 | 249.0 | 4.6 | 25 | 249.4 | 4.1 | 25 | 250.4 | 4.3 | 25 | 251.6 | 4.7 | 25 | 250.8 | 5.4 | 25 | 249.9 | 4.6 | 25 | 250.6 | 4.8 | 25 | 250.6 | 5.0 |
| 26 | 252.2 | 4.8 | 26 | 249.6 | 4.6 | 26 | 251.0 | 4.5 | 26 | 250.2 | 4.8 | 26 | 249.6 | 5.2 | 26 | 250.3 | 5.0 | 26 | 250.6 | 4.8 | 26 | 249.4 | 5.0 |
| 27 | 250.5 | 4.5 | 27 | 250.0 | 4.2 | 27 | 249.8 | 4.4 | 27 | 249.8 | 4.7 | 27 | 250.6 | 5.3 | 27 | 250.0 | 5.0 | 27 | 250.5 | 4.8 | 27 | 251.2 | 5.2 |
| 28 f | 249.7 | 1.8 | 28 f | 250.1 | 1.8 | 28 f | 250.0 | 1.8 | 28 f | 250.0 | 1.7 | 28 f | 249.8 | 1.8 | 28 f | 249.3 | 1.7 | 28 f | 250.1 | 1.8 | 28 f | 250.2 | 1.8 |
| 29 | 251.7 | 4.8 | 29 | 251.9 | 4.5 | 29 | 250.2 | 4.5 | 29 | 249.2 | 4.9 | 29 | 249.4 | 5.2 | 29 | 251.7 | 5.0 | 29 | 251.4 | 4.5 | 29 | 249.5 | 4.8 |
| 30 | 250.4 | 4.6 | 30 | 250.1 | 4.2 | 30 | 250.9 | 4.4 | 30 | 249.8 | 4.6 | 30 | 250.3 | 5.4 | 30 | 249.4 | 4.9 | 30 | 250.3 | 4.9 | 30 | 248.7 | 5.0 |
| 31 | 250.9 | 5.0 | 31 | 249.7 | 4.6 | 31 | 249.3 | 4.5 | 31 | 250.7 | 5.1 | 31 | 250.3 | 5.3 | 31 | 248.7 | 4.8 | 31 | 250.7 | 4.8 | 31 | 250.4 | 4.8 |
| 32 | 250.2 | 4.7 | 32 | 249.7 | 4.4 | 32 | 248.7 | 4.3 | 32 | 250.9 | 4.6 | 32 | 250.1 | 5.5 | 32 | 249.8 | 4.8 | 32 | 249.2 | 4.8 | 32 | 249.2 | 5.4 |
| 33 | 251.6 | 4.5 | 33 | 250.6 | 4.4 | 33 | 251.1 | 4.6 | 33 | 250.3 | 4.5 | 33 | 249.8 | 5.4 | 33 | 250.4 | 4.8 | 33 | 249.5 | 4.7 | 33 | 250.4 | 5.0 |
| 34 | 251.5 | 4.4 | 34 | 250.0 | 4.1 | 34 | 251.2 | 4.3 | 34 | 250.0 | 4.5 | 34 | 251.0 | 5.3 | 34 | 249.6 | 4.8 | 34 | 251.2 | 5.0 | 34 | 251.6 | 5.2 |
| 35 | 251.0 | 4.8 | 35 | 249.9 | 5.0 | 35 | 249.3 | 4.5 | 35 | 249.6 | 4.8 | 35 | 251.5 | 5.4 | 35 | 251.4 | 4.8 | 35 | 250.7 | 4.9 | 35 | 250.0 | 5.2 |
| 36 | 251.0 | 4.3 | 36 | 252.4 | 4.4 | 36 | 250.1 | 4.0 | 36 | 249.8 | 4.3 | 36 | 249.7 | 5.6 | 36 | 250.2 | 4.9 | 36 | 249.5 | 4.9 | 36 | 250.7 | 5.4 |
| 37 | 250.6 | 4.5 | 37 | 249.8 | 4.5 | 37 | 252.0 | 4.3 | 37 | 249.7 | 4.7 | 37 | 250.8 | 5.2 | 37 | 249.9 | 4.8 | 37 | 250.6 | 4.8 | 37 | 250.3 | 4.9 |
| 38 | 250.6 | 4.5 | 38 | 251.0 | 4.1 | 38 | 249.2 | 4.2 | 38 | 249.2 | 4.6 | 38 | 250.3 | 5.5 | 38 | 250.5 | 5.0 | 38 | 249.9 | 5.0 | 38 | 251.2 | 5.2 |
| 39 | 249.6 | 5.0 | 39 | 251.3 | 4.6 | 39 | 250.2 | 4.5 | 39 | 250.4 | 4.8 | 39 | 249.8 | 5.9 | 39 | 250.2 | 5.4 | 39 | 250.3 | 5.5 | 39 | 250.7 | 5.6 |
| 40 | 251.2 | 4.6 | 40 | 249.9 | 4.4 | 40 | 250.1 | 4.2 | 40 | 249.9 | 4.5 | 40 | 251.3 | 5.5 | 40 | 249.9 | 5.0 | 40 | 250.0 | 4.9 | 40 | 249.3 | 5.5 |
| 41 | 251.4 | 4.3 | 41 | 250.0 | 3.9 | 41 | 251.7 | 3.9 | 41 | 248.8 | 4.0 | 41 | 252.4 | 4.6 | 41 | 251.0 | 4.2 | 41 | 248.6 | 4.2 | 41 | 249.3 | 4.8 |
| 42 | 251.2 | 4.5 | 42 | 251.3 | 4.0 | 42 | 250.7 | 4.1 | 42 | 251.8 | 4.3 | 42 | 250.2 | 4.7 | 42 | 251.2 | 4.4 | 42 | 249.0 | 4.5 | 42 | 248.6 | 4.8 |
| 43 | 249.9 | 4.2 | 43 | 249.3 | 3.9 | 43 | 250.3 | 4.0 | 43 | 250.2 | 4.0 | 43 | 249.6 | 4.7 | 43 | 249.1 | 4.2 | 43 | 249.4 | 4.4 | 43 | 250.5 | 4.4 |
| 44 | 251.7 | 4.6 | 44 | 249.9 | 4.0 | 44 | 249.7 | 4.0 | 44 | 248.8 | 4.4 | 44 | 250.5 | 4.7 | 44 | 250.0 | 4.6 | 44 | 250.8 | 4.5 | 44 | 251.1 | 5.0 |
| 45 | 250.3 | 4.3 | 45 | 250.1 | 3.8 | 45 | 249.9 | 3.8 | 45 | 250.7 | 4.2 | 45 | 250.5 | 4.4 | 45 | 249.0 | 4.2 | 45 | 250.2 | 4.5 | 45 | 249.1 | 4.6 |
| 46 | 250.7 | 4.4 | 46 | 249.6 | 3.8 | 46 | 250.6 | 4.0 | 46 | 249.6 | 4.2 | 46 | 250.8 | 4.8 | 46 | 248.8 | 4.2 | 46 | 249.3 | 4.6 | 46 | 249.4 | 4.7 |
| 47 | 251.4 | 4.2 | 47 | 250.9 | 3.8 | 47 | 250.3 | 3.8 | 47 | 251.3 | 4.3 | 47 | 251.0 | 4.5 | 47 | 249.8 | 4.2 | 47 | 250.5 | 4.4 | 47 | 249.2 | 4.4 |
| 48 | 249.7 | 4.6 | 48 | 250.0 | 4.2 | 48 | 252.0 | 4.1 | 48 | 250.9 | 4.2 | 48 | 250.6 | 4.9 | 48 | 250.7 | 4.1 | 48 | 251.1 | 4.3 | 48 | 249.7 | 4.8 |
| 49 | 249.2 | 4.3 | 49 | 249.0 | 4.1 | 49 | 249.1 | 3.8 | 49 | 251.2 | 4.0 | 49 | 250.1 | 4.6 | 49 | 248.5 | 4.1 | 49 | 249.6 | 4.2 | 49 | 250.5 | 4.9 |
| 50 | 251.8 | 4.5 | 50 | 249.1 | 4.2 | 50 | 250.1 | 4.3 | 50 | 249.6 | 4.2 | 50 | 250.5 | 4.8 | 50 | 250.0 | 4.7 | 50 | 250.3 | 4.5 | 50 | 248.8 | 4.8 |
| 51 | 250.0 | 4.2 | 51 | 251.1 | 3.9 | 51 | 250.0 | 4.0 | 51 | 249.9 | 4.0 | 51 | 250.7 | 4.6 | 51 | 250.0 | 4.1 | 51 | 251.0 | 4.4 | 51 | 250.5 | 4.8 |
| 52 | 250.5 | 4.5 | 52 | 250.1 | 4.0 | 52 | 251.4 | 4.0 | 52 | 251.6 | 4.3 | 52 | 250.2 | 4.4 | 52 | 250.9 | 4.2 | 52 | 250.8 | 4.5 | 52 | 250.8 | 5.1 |
| 53 f | 250.8 | 1.7 | 53 f | 249.8 | 1.4 | 53 f | 249.0 | 1.5 | 53 f | 250.0 | 1.7 | 53 f | 249.6 | 1.6 | 53 f | 250.2 | 1.6 | 53 f | 250.2 | 1.6 | 53 f | 250.4 | 1.5 |
| 54 | 249.8 | 4.3 | 54 | 251.1 | 3.9 | 54 | 250.2 | 3.8 | 54 | 250.3 | 4.1 | 54 | 249.4 | 5.4 | 54 | 250.1 | 4.0 | 54 | 250.3 | 4.2 | 54 | 251.9 | 4.5 |
| 55 | 250.3 | 4.7 | 55 | 250.0 | 4.1 | 55 | 249.7 | 4.1 | 55 | 252.4 | 4.4 | 55 | 250.5 | 4.6 | 55 | 250.5 | 4.3 | 55 | 249.7 | 4.6 | 55 | 248.1 | 4.9 |
| 56 | 250.7 | 4.2 | 56 | 248.6 | 3.9 | 56 | 249.9 | 3.8 | 56 | 250.9 | 4.1 | 56 | 250.6 | 4.3 | 56 | 250.4 | 4.0 | 56 | 250.4 | 4.4 | 56 | 249.4 | 4.5 |
| 57 | 250.3 | 4.6 | 57 | 249.4 | 4.0 | 57 | 249.3 | 4.3 | 57 | 250.9 | 4.2 | 57 | 250.6 | 4.5 | 57 | 250.7 | 4.4 | 57 | 249.8 | 4.4 | 57 | 250.5 | 5.1 |
| 58 | 251.6 | 4.3 | 58 | 251.8 | 3.8 | 58 | 250.2 | 3.7 | 58 | 249.0 | 4.2 | | | | | | | | | | | | |