

## Fec test report:

Date: 2021-03-31 15:42:30

Tester name: lc

### Test#1 Monitoring values

Failed

0	FEC label	061	OK
1	FEC DC2438 ID	ad0000024d9e0526	OK
2	FEC_T (to 35°C)	24.094	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.69	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3011	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3098	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3009	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3111	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3070	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3041	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3037	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3029	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 24.094 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.845 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: ad0000024d9e0526

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	510.8	1.0	1 r	511.0	0.0	1 r	509.7	3.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	298.9	0.7	2 r	284.2	0.7	2 r	315.2	0.7	2 r	339.5	0.7	2 r	263.5	0.7	2 r	355.0	0.6	2 r	271.9	0.7	2 r	338.2	0.7
3	238.5	5.2	3	182.9	5.2	3	227.3	5.7	3	243.7	6.7	3	172.7	5.4	3	300.6	5.0	3	218.2	5.7	3	348.9	6.2
4	201.2	4.6	4	269.8	4.5	4	308.9	4.4	4	268.7	4.7	4	235.5	5.0	4	293.2	4.6	4	222.7	4.9	4	343.9	5.0
5	226.1	5.0	5	181.2	5.0	5	218.5	5.5	5	294.1	6.2	5	114.3	5.0	5	246.9	4.9	5	228.8	5.4	5	209.8	5.6
6	241.2	4.6	6	248.3	4.4	6	234.4	4.5	6	264.6	4.9	6	157.9	5.2	6	319.9	4.5	6	179.5	4.7	6	217.2	5.1
7	159.5	4.9	7	221.6	5.0	7	285.3	5.4	7	210.2	6.2	7	215.7	5.0	7	174.3	4.8	7	149.4	5.2	7	298.5	5.6
8	161.6	4.3	8	195.8	4.3	8	166.2	4.3	8	339.5	4.5	8	153.7	5.0	8	285.4	4.5	8	122.5	4.7	8	296.5	5.0
9	180.8	4.8	9	139.1	5.1	9	239.2	5.3	9	189.6	5.8	9	193.7	4.8	9	162.6	4.8	9	172.0	5.2	9	341.9	5.9
10	204.7	4.3	10	163.7	4.3	10	274.9	4.4	10	316.1	4.7	10	113.1	4.9	10	188.6	4.5	10	152.2	4.8	10	261.9	5.1
11	230.6	4.6	11	184.4	4.7	11	283.3	5.1	11	217.0	6.0	11	231.6	5.0	11	246.6	4.6	11	185.9	5.1	11	259.9	5.4
12	155.6	4.4	12	201.2	4.5	12	251.5	4.3	12	261.9	4.8	12	168.8	5.0	12	350.4	4.6	12	241.9	4.9	12	287.4	5.2
13	213.3	4.8	13	214.3	4.9	13	273.2	5.2	13	281.5	5.7	13	179.4	5.0	13	224.6	4.5	13	198.1	5.0	13	220.1	5.7
14	240.7	4.5	14	170.2	4.4	14	189.4	4.4	14	177.0	4.6	14	187.6	5.1	14	306.5	4.6	14	182.2	4.8	14	322.0	5.0
15 f	157.5	1.7	15 f	226.1	1.6	15 f	301.5	1.5	15 f	185.2	1.6	15 f	137.3	1.8	15 f	248.4	1.6	15 f	129.8	1.6	15 f	294.9	1.7
16	242.3	4.9	16	249.1	4.6	16	268.3	5.0	16	209.2	5.7	16	77.8	5.0	16	241.5	4.7	16	188.2	4.8	16	305.9	5.6
17	186.0	4.2	17	117.4	4.2	17	279.1	4.4	17	217.5	4.6	17	118.7	4.9	17	279.8	4.7	17	199.2	4.5	17	277.6	5.1
18	202.3	4.8	18	288.1	4.7	18	241.9	4.9	18	231.5	5.6	18	43.1	4.8	18	305.8	4.9	18	135.8	5.4	18	296.9	5.3
19	180.6	4.3	19	116.9	4.5	19	323.4	4.3	19	266.5	4.5	19	167.4	5.1	19	264.5	4.3	19	239.2	4.8	19	337.8	5.1
20	213.4	4.6	20	204.6	4.9	20	265.3	4.8	20	267.1	5.6	20	113.7	4.9	20	269.2	4.5	20	109.0	4.8	20	333.7	5.2
21	232.7	4.2	21	226.3	4.4	21	306.3	4.3	21	254.3	4.7	21	190.8	5.0	21	247.2	4.6	21	191.9	4.5	21	264.8	5.1
22	156.6	4.6	22	228.8	4.8	22	228.7	4.8	22	201.9	5.5	22	164.6	4.9	22	273.9	4.7	22	174.2	5.0	22	270.2	5.4
23	232.8	4.2	23	145.4	4.5	23	255.2	4.2	23	255.9	4.5	23	181.5	4.8	23	249.7	4.3	23	134.8	4.5	23	251.7	5.0
24	229.7	4.6	24	230.0	4.6	24	218.8	4.9	24	193.0	5.5	24	189.4	5.1	24	286.8	4.8	24	93.9	4.8	24	337.8	5.3
25	268.1	4.4	25	149.8	4.5	25	251.3	4.2	25	258.4	4.6	25	102.9	4.6	25	226.4	4.3	25	189.1	4.6	25	268.4	4.9
26	276.0	4.6	26	159.2	4.7	26	325.4	4.7	26	326.2	5.3	26	216.9	4.9	26	283.7	4.4	26	134.1	4.8	26	339.8	5.6
27	220.6	4.3	27	248.6	4.6	27	287.2	4.6	27	208.1	4.5	27	204.0	4.9	27	276.4	4.6	27	167.4	4.5	27	221.1	4.9
28 f	157.6	1.8	28 f	151.4	1.8	28 f	303.4	1.7	28 f	230.3	1.6	28 f	230.7	1.9	28 f	247.2	1.8	28 f	120.2	1.8	28 f	351.6	1.8
29	276.3	4.5	29	243.1	4.6	29	243.1	4.8	29	198.9	5.4	29	194.8	4.7	29	227.4	4.7	29	188.9	4.8	29	319.1	5.5
30	257.8	4.2	30	128.7	4.4	30	303.2	4.3	30	224.5	4.6	30	243.9	4.7	30	215.4	4.6	30	103.5	4.8	30	199.4	5.0
31	170.2	4.5	31	227.9	4.7	31	222.8	4.8	31	157.3	5.1	31	199.4	4.9	31	228.2	4.7	31	166.7	4.9	31	232.8	5.5
32	270.8	4.7	32	166.5	4.2	32	243.9	4.5	32	266.1	4.6	32	153.1	4.8	32	230.4	4.3	32	185.4	4.7	32	295.3	5.4
33	271.8	4.5	33	196.5	4.4	33	226.6	4.6	33	168.1	5.1	33	222.2	5.2	33	243.0	4.6	33	162.3	4.8	33	220.9	5.4
34	175.7	4.4	34	204.8	4.3	34	267.5	4.3	34	258.4	4.4	34	167.6	4.9	34	293.9	4.6	34	169.3	4.6	34	276.2	5.1
35	206.3	4.7	35	232.8	4.5	35	174.6	4.7	35	309.0	5.1	35	174.3	5.1	35	363.3	4.5	35	151.3	4.9	35	341.7	5.3
36	323.0	4.5	36	229.6	4.3	36	242.0	4.2	36	294.0	4.6	36	126.3	4.7	36	277.0	4.7	36	244.6	4.9	36	283.0	5.2
37	243.1	4.5	37	144.7	4.5	37	283.2	4.5	37	205.6	5.1	37	191.9	4.7	37	242.8	4.7	37	167.0	4.8	37	302.5	5.2
38	223.0	4.3	38	120.4	4.2	38	186.2	4.2	38	226.1	4.4	38	160.9	4.8	38	231.3	4.5	38	204.8	5.0	38	214.5	5.1
39	169.9	4.7	39	196.8	4.6	39	298.0	4.6	39	258.7	5.0	39	258.8	4.9	39	271.6	5.0	39	169.5	5.2	39	231.9	5.7
40	146.6	4.4	40	235.9	4.3	40	245.7	4.0	40	304.1	4.4	40	250.6	4.9	40	222.5	4.5	40	271.3	4.6	40	184.1	5.3
41	301.2	4.0	41	202.8	4.0	41	223.8	4.1	41	173.3	4.0	41	238.8	4.3	41	323.0	3.9	41	163.4	4.2	41	250.7	4.6
42	233.1	4.0	42	208.9	4.2	42	298.1	4.2	42	186.6	4.5	42	195.4	4.5	42	290.7	4.3	42	213.3	4.8	42	299.2	5.6
43	251.6	4.0	43	262.7	3.9	43	290.0	4.2	43	292.1	4.0	43	118.1	4.5	43	210.3	3.9	43	225.0	4.3	43	201.6	4.6
44	223.5	4.2	44	216.7	4.2	44	306.7	4.0	44	334.9	4.8	44	202.1	4.3	44	260.4	4.5	44	180.6	4.8	44	307.4	5.5
45	242.5	3.7	45	230.2	4.1	45	270.8	4.1	45	246.9	4.0	45	182.6	4.3	45	338.0	3.9	45	145.6	4.3	45	258.4	4.7
46	191.3	4.2	46	152.3	4.3	46	283.6	4.4	46	321.6	4.7	46	157.2	4.7	46	287.9	4.3	46	186.0	4.6	46	226.6	5.4
47	238.2	3.8	47	220.4	4.0	47	201.0	4.1	47	188.9	4.1	47	79.0	4.1	47	171.5	3.9	47	196.7	4.2	47	275.9	4.7
48	190.3	4.2	48	123.8	4.5	48	350.9	4.4	48	285.1	4.7	48	195.7	4.8	48	271.9	4.5	48	156.3	4.7	48	242.8	5.4
49	212.4	3.9	49	227.3	3.8	49	326.5	3.8	49	241.6	3.9	49	256.6	4.6	49	249.0	4.0	49	210.3	4.5	49	246.9	4.6
50	185.3	4.2	50	133.7	4.3	50	256.5	4.2	50	304.2	4.7	50	178.9	4.6	50	343.7	4.5	50	73.0	4.5	50	292.7	5.4
51	251.8	4.2	51	176.1	4.0	51	237.6	3.8	51	295.9	3.9	51	174.5	4.1	51	264.1	4.3	51	106.5	4.1	51	268.2	4.5
52	167.6	4.2	52	208.8	4.3	52	228.0	4.5	52	234.3	4.6	52	129.7	4.6	52	190.4	4.3	52	130.8	5.0	52	266.8	5.5
53 f	250.3	1.5	53 f	222.4	1.5	53 f	231.4	1.5	53 f	211.6	1.5	53 f	178.8	1.5	53 f	279.4	1.4	53 f	179.6	1.4	53 f	268.2	1.6
54	209.7	3.9	54	175.9	3.9	54	169.7	4.1	54	204.9	3.9	54	84.7	4.7	54	270.2	4.2	54	112.1	4.4	54	375.4	4.7
55	225.9	3.9	55	228.0	4.5	55	254.3	4.4	55	224.1	4.5	55	164.9	4.4	55	181.9	4.5	55	221.7	4.8	55	263.3	5.5
56	166.1	3.9	56	139.6	4.0	56	310.9	3.9	56	253.8	3.9	56	142.0	4.2	56	184.5	3.9	56	133.7	4.1	56	176.2	4.6
57	195.7	4.0	57	172.5	4.3	57	368.1	4.4	57	269.0	4.6	57	143.7	4.4	57	230.8	4.4	57	236.4	4.7	57	314.8	5.5
58	254.0	3.9	58	207.9	4.0	58	277.4	3.8	58	217.8	3.9	58	145.1	4.2	5								



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	374.2	7.9	1 r	268.2	10.4	1 r	370.9	9.1	1 r	262.7	11.5	1 r	286.8	9.4	1 r	441.3	8.1	1 r	335.2	8.9	1 r	352.9	12.5
2 r	250.2	0.7	2 r	250.4	0.7	2 r	250.6	0.7	2 r	249.8	0.7	2 r	249.9	0.7	2 r	250.1	0.7	2 r	250.1	0.7	2 r	250.4	0.7
3	251.5	5.0	3	251.2	4.9	3	250.6	5.0	3	249.3	5.5	3	249.6	5.2	3	251.3	4.7	3	250.7	5.2	3	250.9	5.3
4	250.2	4.4	4	248.9	4.5	4	249.3	4.3	4	250.2	4.6	4	249.5	4.9	4	249.7	4.9	4	250.0	4.8	4	251.0	4.7
5	250.2	4.8	5	251.5	4.8	5	251.0	4.8	5	250.5	5.4	5	249.4	5.0	5	250.2	4.6	5	252.2	5.0	5	249.3	4.9
6	251.5	4.3	6	250.9	4.1	6	251.7	4.4	6	249.7	4.5	6	249.9	4.8	6	249.6	4.6	6	251.0	4.7	6	251.1	4.9
7	249.9	4.4	7	250.8	4.7	7	250.9	4.7	7	250.6	5.3	7	249.9	5.1	7	249.6	4.4	7	250.0	4.9	7	249.2	5.1
8	249.3	4.2	8	250.4	4.3	8	249.6	4.2	8	250.2	4.7	8	250.7	4.9	8	250.1	4.5	8	249.2	4.5	8	251.0	4.8
9	249.9	4.8	9	247.8	4.7	9	251.4	4.6	9	249.9	5.1	9	250.3	4.7	9	248.9	4.4	9	249.1	5.0	9	251.1	5.2
10	249.9	4.5	10	250.2	4.6	10	250.2	4.2	10	250.3	4.5	10	250.1	4.8	10	249.2	4.6	10	250.1	4.8	10	248.8	4.7
11	249.4	4.4	11	250.1	4.4	11	252.2	4.9	11	250.2	4.9	11	250.0	4.8	11	249.6	4.8	11	249.9	4.8	11	251.5	4.9
12	249.6	4.3	12	251.8	4.3	12	250.0	4.2	12	249.9	4.3	12	249.9	4.8	12	251.2	4.7	12	249.8	4.4	12	251.4	4.7
13	249.6	4.2	13	251.2	4.5	13	251.6	4.5	13	249.8	5.0	13	248.9	4.9	13	249.9	4.5	13	250.7	4.9	13	248.4	4.9
14	249.2	4.7	14	251.5	4.4	14	250.5	4.1	14	249.9	4.2	14	250.4	4.9	14	250.0	4.5	14	250.5	4.5	14	250.1	4.7
15 f	249.3	1.7	15 f	249.6	1.6	15 f	250.9	1.6	15 f	250.2	1.6	15 f	250.7	1.7	15 f	249.9	1.6	15 f	249.9	1.6	15 f	250.5	1.6
16	249.7	4.3	16	250.4	4.4	16	250.5	4.4	16	250.6	4.8	16	250.7	4.7	16	250.5	4.2	16	251.6	4.9	16	249.0	5.0
17	250.6	4.4	17	249.1	4.2	17	249.7	4.2	17	250.0	4.3	17	250.4	4.7	17	248.4	4.5	17	250.7	4.6	17	249.8	4.7
18	252.2	4.4	18	249.5	4.6	18	250.3	4.5	18	249.1	4.7	18	251.8	4.7	18	248.4	4.3	18	249.0	4.6	18	248.6	4.8
19	249.8	4.3	19	251.3	4.0	19	250.4	4.1	19	250.7	4.2	19	250.4	5.0	19	250.3	4.6	19	250.6	4.6	19	248.8	4.7
20	250.9	4.2	20	249.3	4.2	20	252.1	4.5	20	249.2	4.8	20	250.6	4.6	20	249.4	4.4	20	249.1	4.5	20	249.4	4.6
21	250.0	4.2	21	251.4	4.2	21	249.8	4.4	21	250.2	4.3	21	251.2	4.8	21	250.7	4.4	21	249.7	4.6	21	249.5	4.6
22	248.8	4.3	22	250.2	4.3	22	250.9	4.7	22	249.0	4.6	22	249.0	4.9	22	250.1	4.3	22	250.8	4.6	22	250.5	4.7
23	250.8	4.1	23	251.6	4.2	23	249.6	4.1	23	251.5	4.0	23	249.2	4.9	23	250.3	4.3	23	249.9	4.4	23	250.7	4.6
24	248.8	4.3	24	249.9	4.2	24	251.6	4.4	24	248.8	4.7	24	252.2	4.8	24	249.2	4.5	24	252.0	4.4	24	250.0	4.8
25	248.8	4.3	25	249.7	4.1	25	250.9	4.1	25	250.0	4.1	25	250.6	5.0	25	251.3	4.2	25	249.1	4.4	25	251.1	4.5
26	250.3	4.1	26	250.5	4.3	26	249.7	4.4	26	251.3	4.6	26	251.0	4.5	26	249.3	4.4	26	249.9	4.6	26	250.5	4.7
27	247.8	4.2	27	250.3	4.1	27	252.3	4.4	27	250.6	4.2	27	250.5	4.7	27	251.0	4.3	27	250.2	4.5	27	250.7	4.7
28 f	249.9	1.8	28 f	251.0	1.9	28 f	251.0	1.8	28 f	250.6	1.6	28 f	249.6	1.8	28 f	250.3	1.8	28 f	249.9	1.7	28 f	249.5	1.7
29	250.6	4.5	29	252.7	4.2	29	250.2	4.2	29	249.9	4.5	29	250.1	4.6	29	250.5	4.5	29	250.0	4.6	29	250.3	4.8
30	250.8	4.3	30	250.4	4.2	30	249.7	4.1	30	249.9	4.2	30	250.4	4.8	30	250.2	4.4	30	251.6	4.4	30	250.2	4.8
31	250.3	4.3	31	249.8	4.3	31	249.9	4.5	31	250.4	4.5	31	250.9	4.5	31	250.3	4.4	31	249.9	4.4	31	249.8	4.6
32	249.5	4.3	32	250.0	4.1	32	250.3	4.3	32	250.5	4.6	32	251.7	4.8	32	251.1	4.5	32	249.9	4.4	32	250.6	4.8
33	251.7	4.2	33	248.7	4.3	33	250.9	4.3	33	250.8	4.5	33	250.9	4.4	33	249.7	4.2	33	250.2	4.5	33	250.4	5.0
34	250.9	4.5	34	249.7	4.2	34	249.5	4.1	34	251.8	4.1	34	249.9	4.6	34	250.6	4.5	34	250.2	4.6	34	248.8	4.7
35	249.8	4.4	35	250.4	4.3	35	251.8	4.5	35	249.9	4.4	35	249.3	4.7	35	250.5	4.1	35	251.1	4.5	35	250.7	4.8
36	250.4	4.0	36	250.6	4.3	36	250.7	4.2	36	250.2	4.1	36	250.5	4.7	36	252.5	4.6	36	249.7	4.4	36	249.8	4.7
37	249.3	4.2	37	249.4	4.3	37	252.2	4.2	37	249.6	4.5	37	249.0	4.5	37	250.7	4.7	37	250.4	4.3	37	250.6	4.7
38	251.1	4.1	38	250.5	4.2	38	249.9	4.0	38	251.9	4.0	38	250.5	4.9	38	249.1	4.2	38	250.6	4.6	38	248.9	4.6
39	250.0	4.5	39	250.2	4.8	39	250.5	4.4	39	251.1	4.5	39	248.9	4.8	39	249.6	4.7	39	249.4	4.8	39	251.0	4.9
40	250.1	4.3	40	248.7	4.3	40	249.9	3.9	40	250.4	4.2	40	249.5	4.9	40	250.9	4.4	40	250.4	4.6	40	250.9	4.8
41	250.6	4.0	41	250.5	4.1	41	250.3	4.1	41	249.3	3.9	41	250.3	4.2	41	250.3	4.0	41	251.6	4.2	41	249.7	4.4
42	250.2	4.0	42	249.0	4.1	42	250.0	4.3	42	251.2	4.2	42	251.7	4.5	42	249.9	4.1	42	249.9	4.6	42	251.0	5.1
43	251.3	4.1	43	251.9	4.0	43	249.9	3.9	43	250.1	3.9	43	250.6	4.3	43	251.9	3.7	43	251.8	4.1	43	248.9	4.4
44	249.2	3.9	44	249.9	4.0	44	249.9	4.2	44	249.6	4.3	44	251.1	4.5	44	250.7	4.2	44	249.2	4.4	44	250.2	4.9
45	250.9	4.0	45	251.4	3.8	45	249.5	3.9	45	249.5	3.8	45	248.9	4.3	45	251.1	4.2	45	250.1	4.2	45	251.5	4.4
46	251.5	4.1	46	251.3	4.2	46	250.7	4.3	46	250.9	4.3	46	250.5	4.4	46	249.5	4.0	46	250.0	4.5	46	250.5	5.2
47	250.0	4.1	47	250.3	4.0	47	250.5	3.9	47	250.3	3.9	47	251.5	4.4	47	250.8	4.0	47	251.0	4.1	47	250.5	4.3
48	250.7	4.0	48	250.6	4.2	48	248.7	4.2	48	250.5	4.4	48	251.8	4.5	48	249.4	4.1	48	251.2	4.3	48	250.7	5.0
49	249.6	3.9	49	249.1	4.0	49	250.1	3.8	49	250.3	3.8	49	250.6	4.3	49	250.7	3.9	49	249.3	4.2	49	249.5	4.5
50	250.4	4.1	50	249.4	4.2	50	250.9	4.0	50	251.3	4.3	50	250.6	4.2	50	249.9	4.5	50	249.4	4.6	50	249.3	5.0
51	250.7	4.0	51	249.7	3.9	51	248.0	3.9	51	249.7	3.9	51	250.1	4.1	51	250.7	4.1	51	249.8	4.3	51	249.7	4.3
52	250.8	4.2	52	249.2	4.3	52	250.5	4.2	52	250.3	4.3	52	251.1	4.2	52	249.6	4.2	52	250.1	4.6	52	249.0	5.0
53 f	250.4	1.5	53 f	250.6	1.6	53 f	251.2	1.5	53 f	249.8	1.4	53 f	250.2	1.6	53 f	249.9	1.5	53 f	249.9	1.5	53 f	250.6	1.5
54	250.2	4.0	54	251.4	4.0	54	249.9	3.8	54	250.3	4.0	54	251.1	4.4	54	249.2	4.0	54	250.4	4.1	54	251.5	4.7
55	250.5	3.9	55	249.6	4.2	55	250.1	4.0	55	249.4	4.2	55	251.8	4.6	55	249.8	4.2	55	249.7	4.6	55	250.2	5.0
56	249.8	4.0	56	250.3	4.0	56	251.6	4.0	56	250.8	4.1	56	249.5	4.2	56	250.0	3.9	56	249.7	4.2	56	249.7	4.4
57	250.5	4.0	57	250.6	4.2	57	250.1	4.2	57	250.7	4.3	57	251.2	4.7	57	250.0	4.2	57	250.0	4.5	57	249.6	5.0
58	251.8	3.9	58	251.2	4.3	58	251.1	3.9	58	250.8	3.9												