

Fec test report:

Date: 2021-09-21 11:14:08

Tester name: lc

Test#1 Monitoring values

Passed

0	FEC label	045	OK
1	FEC DC2438 ID	470000024d98d326	OK
2	FEC_T (to 35°C)	28.719	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.2A to 1.6A)	1.274	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3083	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3050	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3118	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2984	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3057	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3067	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3006	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 28.719 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.637 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 470000024d98d326

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE_WAIT_FEM_PKT_Current)
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x0 (0) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 TdcM(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 TdcM(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 TdcM(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	321.7	0.7	2 r	287.0	0.7	2 r	344.6	0.7	2 r	344.6	0.7	2 r	317.3	0.7	2 r	347.8	0.7	2 r	327.3	0.7	2 r	362.4	0.7
3	298.4	5.1	3	301.9	5.0	3	313.0	4.8	3	312.8	5.0	3	278.8	5.7	3	239.7	4.8	3	278.9	4.8	3	241.6	5.0
4	361.0	4.6	4	285.3	4.7	4	330.7	4.4	4	343.3	4.8	4	347.4	5.2	4	223.5	4.7	4	321.5	4.7	4	265.5	4.9
5	356.4	5.0	5	218.8	4.9	5	229.3	5.2	5	258.0	5.1	5	317.0	5.6	5	262.8	5.0	5	256.3	5.0	5	304.5	4.9
6	217.3	4.7	6	288.7	4.6	6	313.7	4.4	6	303.2	4.8	6	251.8	5.3	6	179.5	4.7	6	295.1	4.5	6	356.6	4.9
7	330.2	4.7	7	182.6	4.6	7	306.4	4.5	7	245.8	5.0	7	236.6	5.3	7	304.4	4.9	7	226.6	4.9	7	327.3	4.5
8	281.4	4.3	8	232.6	4.3	8	296.1	4.2	8	238.5	4.5	8	196.4	5.1	8	243.0	4.6	8	189.5	4.6	8	332.2	5.1
9	316.3	4.7	9	277.6	4.9	9	283.2	4.7	9	286.4	4.8	9	216.0	5.2	9	234.4	4.8	9	303.6	5.0	9	330.6	4.6
10	290.8	4.5	10	226.3	4.1	10	292.5	4.4	10	256.4	4.8	10	243.2	5.0	10	170.2	4.8	10	273.0	4.6	10	357.9	4.9
11	249.6	5.0	11	277.5	4.8	11	301.2	4.5	11	181.0	5.0	11	355.8	4.8	11	258.4	5.0	11	280.2	4.7	11	291.2	4.8
12	270.3	4.4	12	199.5	4.4	12	362.8	4.2	12	214.7	4.7	12	302.3	4.9	12	221.1	4.8	12	205.0	4.6	12	361.2	4.6
13	277.3	4.8	13	218.1	4.6	13	269.9	4.5	13	299.5	4.8	13	260.1	5.2	13	181.8	4.9	13	304.3	4.4	13	339.2	4.8
14	240.3	4.5	14	223.7	4.6	14	271.9	4.4	14	263.1	4.5	14	294.6	4.8	14	235.4	4.8	14	227.2	4.6	14	322.6	4.7
15 f	291.1	1.6	15 f	265.1	1.7	15 f	263.5	1.6	15 f	246.5	1.6	15 f	254.7	1.7	15 f	287.4	1.7	15 f	219.0	1.9	15 f	308.0	1.8
16	284.9	4.8	16	233.2	4.5	16	305.3	4.6	16	225.4	4.6	16	287.1	4.9	16	273.7	4.5	16	312.7	4.5	16	285.4	4.6
17	384.7	4.2	17	161.7	4.5	17	285.6	4.4	17	268.4	4.5	17	354.8	4.9	17	250.1	4.6	17	268.4	4.6	17	268.6	4.7
18	324.9	4.6	18	196.5	4.4	18	228.4	4.7	18	300.4	4.7	18	286.7	4.8	18	246.7	4.7	18	233.4	4.7	18	247.2	4.4
19	271.4	4.5	19	270.6	4.4	19	301.7	4.4	19	309.9	4.6	19	232.9	5.2	19	217.3	4.7	19	260.3	4.5	19	245.2	4.6
20	271.1	4.8	20	325.6	4.5	20	294.4	4.4	20	316.6	4.5	20	283.9	5.1	20	193.3	4.5	20	302.6	4.5	20	303.4	4.6
21	369.7	4.5	21	189.2	4.4	21	254.6	4.7	21	321.8	4.7	21	262.9	4.9	21	300.9	4.6	21	275.9	4.6	21	379.0	4.7
22	277.8	4.7	22	244.3	4.4	22	265.1	4.5	22	282.1	4.7	22	280.1	4.6	22	316.2	4.9	22	246.5	4.6	22	274.6	4.6
23	287.5	4.6	23	254.2	4.3	23	287.4	4.4	23	322.2	4.4	23	317.3	5.1	23	237.1	4.8	23	170.5	4.7	23	336.1	4.6
24	259.6	4.5	24	267.0	4.5	24	240.8	4.3	24	295.4	4.4	24	202.8	5.2	24	189.9	4.6	24	215.8	4.8	24	351.9	4.8
25	334.3	4.4	25	260.2	4.2	25	224.2	4.4	25	253.5	4.6	25	237.4	4.8	25	364.2	4.5	25	244.4	4.5	25	389.9	4.5
26	271.9	4.3	26	250.2	4.6	26	148.7	4.5	26	290.4	4.7	26	225.7	4.9	26	253.0	4.5	26	275.3	4.6	26	316.1	4.7
27	320.6	4.5	27	245.2	4.4	27	293.3	4.3	27	214.0	4.8	27	321.0	5.0	27	231.2	4.5	27	232.3	4.6	27	342.7	4.6
28 f	342.6	1.7	28 f	232.2	1.7	28 f	293.7	1.8	28 f	287.4	1.8	28 f	228.2	1.8	28 f	222.4	1.7	28 f	219.0	1.8	28 f	216.2	1.7
29	268.6	4.7	29	235.7	4.6	29	250.6	4.3	29	295.8	4.4	29	271.7	4.8	29	323.8	4.8	29	256.5	4.7	29	347.0	4.5
30	260.5	4.3	30	199.4	4.2	30	303.0	4.4	30	270.7	4.5	30	244.6	4.9	30	303.3	4.6	30	286.4	4.8	30	335.2	4.6
31	322.6	4.5	31	235.2	4.7	31	302.7	4.3	31	214.6	4.7	31	290.0	5.1	31	332.3	4.7	31	238.5	4.6	31	367.6	4.6
32	277.3	4.2	32	228.9	4.5	32	316.8	4.2	32	215.4	4.4	32	312.6	4.9	32	243.5	4.7	32	327.5	4.5	32	321.5	4.5
33	278.4	4.5	33	244.4	4.6	33	310.4	4.3	33	266.4	4.6	33	280.1	5.0	33	317.5	4.8	33	176.4	4.5	33	276.9	4.5
34	249.7	4.4	34	281.1	4.3	34	268.1	4.3	34	270.7	4.3	34	249.8	5.1	34	276.2	4.5	34	340.2	4.5	34	313.2	5.1
35	353.5	4.5	35	212.0	4.3	35	273.5	4.4	35	233.1	4.5	35	260.9	5.0	35	202.8	4.8	35	209.2	4.4	35	257.5	4.7
36	256.3	4.3	36	230.9	4.3	36	234.1	4.1	36	311.3	4.5	36	220.7	4.9	36	247.2	4.7	36	211.5	4.5	36	301.8	4.6
37	297.1	4.7	37	108.1	4.5	37	249.4	4.4	37	244.0	4.8	37	269.5	4.7	37	244.8	4.6	37	287.5	4.9	37	266.7	4.5
38	336.5	4.4	38	218.2	4.3	38	186.8	4.3	38	252.8	4.5	38	234.8	4.9	38	257.5	4.7	38	269.1	5.1	38	310.9	4.8
39	247.5	4.7	39	316.8	4.4	39	356.3	4.8	39	323.9	4.9	39	233.0	5.4	39	289.7	5.0	39	267.2	5.0	39	351.3	5.0
40	345.9	4.3	40	229.9	4.2	40	269.7	3.9	40	232.1	4.2	40	265.8	4.9	40	285.7	4.7	40	278.4	4.6	40	315.6	4.7
41	278.1	4.2	41	201.8	4.0	41	171.8	3.9	41	282.7	4.0	41	220.7	4.4	41	266.3	4.2	41	286.0	4.2	41	316.3	4.3
42	318.0	4.3	42	222.5	4.0	42	348.4	4.1	42	277.0	4.0	42	238.0	4.5	42	301.0	4.2	42	286.1	4.4	42	334.4	4.6
43	308.3	4.1	43	242.7	4.1	43	224.5	4.0	43	210.7	3.8	43	213.5	4.2	43	302.8	3.9	43	187.6	4.2	43	258.4	4.2
44	288.1	4.5	44	165.8	4.1	44	314.9	4.2	44	236.9	4.1	44	264.2	4.2	44	319.6	4.1	44	271.3	4.1	44	339.0	4.5
45	231.7	4.0	45	245.2	4.1	45	325.7	4.2	45	272.9	3.9	45	293.8	4.2	45	198.8	4.1	45	252.2	4.0	45	227.1	4.4
46	266.2	4.2	46	225.6	4.2	46	244.3	3.9	46	308.7	4.2	46	282.2	4.4	46	307.2	4.3	46	268.7	4.3	46	307.4	4.7
47	269.3	4.0	47	224.1	3.9	47	351.3	4.4	47	289.9	4.1	47	302.6	4.3	47	290.5	4.1	47	286.5	4.2	47	375.2	4.3
48	298.6	4.4	48	308.8	4.3	48	303.6	4.0	48	280.1	4.2	48	292.1	4.4	48	210.1	4.2	48	200.5	4.3	48	331.8	4.6
49	248.2	4.2	49	200.4	4.4	49	350.9	4.2	49	242.7	3.9	49	218.1	4.3	49	265.2	4.1	49	224.4	4.1	49	309.9	4.4
50	276.4	4.5	50	266.6	4.2	50	257.7	4.2	50	295.6	3.9	50	321.4	4.6	50	333.5	4.5	50	273.7	4.2	50	264.3	4.4
51	274.9	4.3	51	314.0	4.0	51	278.0	3.8	51	295.4	3.8	51	253.8	4.4	51	260.6	4.0	51	271.9	4.1	51	223.5	4.5
52	278.1	4.5	52	253.6	4.2	52	301.5	4.1	52	265.1	3.9	52	233.7	4.3	52	214.1	4.3	52	306.5	4.3	52	261.0	4.2
53 f	277.1	1.6	53 f	234.6	1.5	53 f	247.9	1.4	53 f	204.6	1.5	53 f	285.8	1.5	53 f	212.2	1.4	53 f	218.4	1.5	53 f	292.7	1.4
54	324.1	4.3	54	223.6	3.9	54	246.1	3.9	54	291.3	3.8	54	233.7	4.3	54	370.2	4.1	54	245.6	4.1	54	311.0	4.4
55	328.9	4.5	55	271.6	4.5	55	289.9	4.8	55	301.2	4.3	55	270.1	4.1	55	241.6	4.4	55	264.4	4.5	55	394.2	4.2
56	201.9	4.2	56	294.5	4.0	56	295.1	3.9	56	317.6	3.8	56	155.1	4.8	56	266.3	4.2	56	243.8	4.2	56	346.8	4.6
57	336.0	4.3	57	285.1	4.2	57	226.8	4.2	57	237.0	3.9	57	224.6	4.5	57	349.6	4.2	57	211.7	4.3	57	264.3	4.5
58	296.4	4.3	58	263.0	3.9	58	354.5	4.2	58	208.2	4.0	58	288.5	4.3									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	397.9	10.0	1 r	457.1	8.9	1 r	375.2	9.3	1 r	462.0	7.5	1 r	370.7	10.9	1 r	392.8	7.3	1 r	445.8	7.3	1 r	339.8	9.2
2 r	249.7	0.7	2 r	250.2	0.7	2 r	249.7	0.7	2 r	249.8	0.7	2 r	250.3	0.7	2 r	249.8	0.7	2 r	250.5	0.7	2 r	250.4	0.7
3	250.4	5.2	3	250.2	4.8	3	249.6	4.9	3	248.4	5.3	3	250.3	5.8	3	249.7	4.9	3	250.8	4.9	3	249.2	4.9
4	249.7	4.5	4	250.5	4.5	4	250.1	4.6	4	249.6	5.0	4	249.4	5.5	4	248.7	4.7	4	251.1	4.6	4	251.5	4.7
5	249.6	4.9	5	250.5	4.7	5	251.0	4.8	5	250.3	5.1	5	249.3	5.6	5	249.5	4.7	5	250.6	4.8	5	249.8	4.8
6	249.1	4.6	6	250.1	4.5	6	249.3	4.6	6	250.0	4.8	6	249.8	5.2	6	249.8	4.9	6	251.7	4.9	6	249.5	4.6
7	249.7	5.0	7	250.3	4.6	7	250.3	4.6	7	249.5	4.9	7	250.4	5.2	7	250.4	4.8	7	248.8	4.7	7	251.1	4.9
8	250.3	4.4	8	250.3	4.5	8	249.1	4.3	8	249.9	4.6	8	251.8	5.3	8	250.9	4.5	8	250.4	4.8	8	250.0	4.7
9	249.9	4.8	9	250.4	4.9	9	249.8	4.7	9	249.1	5.1	9	249.7	5.2	9	251.7	4.8	9	249.0	4.9	9	247.8	4.5
10	249.2	4.6	10	249.2	4.6	10	250.7	4.5	10	251.2	4.7	10	250.7	5.3	10	249.8	4.6	10	250.9	5.0	10	250.1	5.1
11	248.6	4.8	11	249.9	4.6	11	249.3	4.5	11	250.9	5.1	11	249.2	5.0	11	250.0	4.6	11	250.1	4.6	11	250.1	4.7
12	248.2	4.7	12	251.0	4.4	12	249.2	4.4	12	249.5	4.8	12	250.8	5.1	12	250.8	4.7	12	249.3	4.6	12	250.2	4.8
13	251.3	4.9	13	250.0	4.6	13	249.9	4.3	13	251.4	4.9	13	251.4	5.2	13	249.9	4.5	13	251.1	4.5	13	250.0	5.0
14	249.3	4.3	14	249.7	4.4	14	251.5	4.4	14	250.4	4.5	14	249.5	5.3	14	251.0	4.7	14	250.1	4.7	14	250.1	4.8
15 f	249.6	1.6	15 f	250.1	1.6	15 f	250.0	1.7	15 f	250.7	1.7	15 f	250.0	1.6	15 f	249.9	1.8	15 f	250.3	1.7	15 f	250.1	1.6
16	251.4	4.9	16	251.8	4.5	16	250.5	4.5	16	250.7	4.6	16	250.4	5.0	16	249.1	4.5	16	250.3	4.7	16	250.3	4.9
17	249.2	4.7	17	249.8	4.4	17	247.9	4.3	17	251.5	4.5	17	248.4	5.0	17	249.1	4.4	17	251.2	4.6	17	250.5	4.6
18	251.9	4.8	18	250.2	4.6	18	252.5	4.5	18	250.5	4.4	18	248.4	5.2	18	249.2	4.7	18	250.5	4.8	18	250.5	4.6
19	251.4	4.5	19	248.2	4.3	19	249.3	4.2	19	251.2	4.6	19	249.9	4.8	19	249.9	4.8	19	250.8	4.4	19	251.2	4.7
20	250.3	4.6	20	250.7	4.6	20	249.9	4.7	20	250.2	4.6	20	250.8	4.7	20	249.0	4.8	20	250.8	4.4	20	249.8	4.5
21	248.4	4.4	21	250.8	4.3	21	250.5	4.4	21	248.9	4.3	21	250.3	5.0	21	249.5	4.5	21	249.6	4.7	21	250.7	4.9
22	249.1	4.7	22	250.3	4.7	22	250.2	4.2	22	249.3	4.6	22	249.7	4.8	22	249.1	4.7	22	248.8	4.6	22	250.3	4.6
23	250.5	4.4	23	250.8	4.4	23	250.2	4.6	23	250.5	4.5	23	250.4	5.2	23	249.8	4.5	23	250.0	4.4	23	250.6	4.7
24	249.4	4.5	24	250.0	4.6	24	249.6	4.3	24	250.7	4.5	24	249.3	5.0	24	248.4	4.6	24	250.0	4.5	24	249.2	4.7
25	251.7	4.4	25	251.1	4.3	25	251.1	4.3	25	250.9	4.3	25	251.3	4.6	25	251.4	4.5	25	249.8	4.7	25	250.5	4.6
26	250.2	4.6	26	250.2	4.5	26	250.7	4.2	26	250.2	4.5	26	250.0	4.7	26	251.2	4.8	26	249.2	4.5	26	249.9	4.3
27	249.7	4.4	27	251.3	4.1	27	249.3	4.3	27	249.8	4.3	27	251.0	4.7	27	251.0	4.7	27	250.5	4.5	27	249.8	4.7
28 f	249.4	1.6	28 f	250.8	1.8	28 f	249.6	1.7	28 f	250.3	1.9	28 f	250.0	1.8	28 f	250.8	1.9	28 f	249.9	1.9	28 f	250.6	1.8
29	249.6	4.7	29	250.9	4.7	29	249.2	4.6	29	250.8	4.4	29	249.6	4.8	29	250.6	4.7	29	248.7	4.5	29	249.8	4.8
30	250.6	4.5	30	250.8	4.5	30	249.1	4.3	30	251.3	4.4	30	250.2	5.0	30	250.2	4.5	30	250.3	4.7	30	249.9	4.8
31	249.7	4.6	31	249.6	4.7	31	249.6	4.2	31	249.3	4.7	31	250.8	4.9	31	249.7	4.5	31	250.9	4.5	31	248.9	4.6
32	249.4	4.4	32	250.4	4.5	32	248.9	4.1	32	248.9	4.6	32	249.2	4.8	32	251.1	4.5	32	250.2	4.5	32	249.7	4.6
33	251.2	4.5	33	250.7	4.5	33	251.2	4.3	33	250.9	4.5	33	251.7	5.1	33	250.1	4.4	33	251.3	4.6	33	250.1	4.6
34	249.7	4.3	34	251.2	4.2	34	252.1	4.1	34	250.5	4.5	34	249.8	4.9	34	249.6	4.5	34	250.9	4.5	34	249.7	5.0
35	248.9	4.6	35	249.8	4.6	35	251.3	4.4	35	250.8	4.3	35	250.3	4.9	35	249.1	4.7	35	250.3	4.5	35	251.1	4.4
36	250.8	4.5	36	250.5	4.5	36	250.9	4.2	36	251.7	4.6	36	247.8	5.0	36	251.3	4.7	36	249.9	4.6	36	250.0	4.9
37	250.0	4.5	37	249.0	4.6	37	250.0	4.5	37	250.5	4.6	37	251.1	4.9	37	249.9	4.7	37	251.1	4.5	37	249.2	4.6
38	250.1	4.2	38	250.8	4.5	38	248.7	4.3	38	249.2	4.4	38	248.4	5.1	38	250.7	4.7	38	249.1	4.6	38	250.5	4.8
39	250.7	4.6	39	251.2	4.8	39	251.0	4.5	39	250.4	4.7	39	249.8	5.4	39	247.9	4.9	39	250.3	5.0	39	250.2	4.8
40	250.8	4.3	40	248.8	4.2	40	251.2	4.3	40	250.6	4.3	40	248.5	5.1	40	248.9	4.8	40	250.4	4.5	40	248.1	5.0
41	251.3	4.3	41	249.8	4.0	41	249.8	3.9	41	251.6	4.0	41	249.2	4.6	41	249.8	4.0	41	249.2	4.2	41	251.5	4.4
42	249.9	4.4	42	250.5	4.2	42	251.2	4.3	42	251.1	4.2	42	249.4	4.6	42	249.0	4.3	42	249.3	4.2	42	250.4	4.3
43	250.8	4.3	43	250.0	3.9	43	250.4	4.2	43	250.9	3.8	43	248.9	4.3	43	248.6	4.2	43	250.0	4.0	43	249.8	4.2
44	250.7	4.2	44	249.8	4.4	44	249.3	4.0	44	249.5	4.2	44	250.0	4.4	44	249.9	4.3	44	250.2	4.3	44	250.1	4.4
45	248.6	4.5	45	249.9	3.9	45	249.9	3.9	45	249.8	4.0	45	251.3	4.3	45	248.5	4.0	45	251.4	4.2	45	251.3	4.4
46	249.8	4.3	46	249.6	4.1	46	250.6	4.2	46	249.7	4.2	46	249.8	4.6	46	251.5	4.3	46	250.7	4.2	46	250.4	4.4
47	250.6	4.2	47	249.1	4.0	47	249.7	4.2	47	250.4	3.9	47	249.7	4.2	47	248.6	4.0	47	248.0	4.1	47	249.3	4.7
48	250.0	4.5	48	249.3	4.3	48	249.9	3.9	48	250.3	4.4	48	251.1	4.3	48	250.0	4.3	48	251.0	4.2	48	250.4	4.7
49	249.4	4.2	49	250.6	4.1	49	250.5	3.9	49	250.6	3.8	49	249.3	4.3	49	251.0	4.1	49	250.9	4.6	49	250.4	4.4
50	250.3	4.3	50	249.5	4.3	50	249.5	4.2	50	249.9	4.1	50	249.9	4.6	50	250.7	4.5	50	251.5	4.2	50	248.4	4.5
51	249.8	4.3	51	250.2	4.0	51	250.7	3.9	51	250.4	3.9	51	251.0	4.3	51	249.2	4.3	51	250.4	4.2	51	250.9	4.1
52	251.2	4.5	52	250.6	4.2	52	250.1	4.1	52	249.8	4.4	52	250.9	4.3	52	249.6	4.3	52	248.1	4.4	52	248.5	4.5
53 f	250.4	1.5	53 f	249.8	1.5	53 f	249.9	1.4	53 f	249.6	1.4	53 f	250.2	1.5	53 f	250.0	1.5	53 f	249.9	1.5	53 f	249.1	1.4
54	250.5	4.2	54	249.4	4.0	54	249.5	3.9	54	250.2	3.9	54	250.4	4.1	54	249.3	3.9	54	249.3	4.2	54	250.1	4.3
55	249.8	4.5	55	250.7	4.3	55	249.8	4.2	55	251.4	4.3	55	249.8	4.5	55	248.8	4.5	55	249.8	4.3	55	249.5	4.6
56	250.3	4.1	56	248.9	4.2	56	250.5	4.0	56	250.9	3.9	56	250.4	4.3	56	251.1	4.2	56	250.2	4.1	56	249.9	4.4
57	249.8	4.5	57	251.2	4.3	57	250.1	4.2	57	252.0	4.0	57	248.3	4.4	57	250.8	4.2	57	251.2	4.3	57	250.8	4.5
58	250.6	4.2	58	250.2	3.9	58	251.1	4.1	58	249.5	4.1												