

## Fec test report:

Date: 2021-10-07 15:25:45

Tester name: Boris

### Test#1 Monitoring values

Passed

0	FEC label	034	OK
1	FEC DC2438 ID	aa0000024ddea326	OK
2	FEC_T (to 35°C)	23.406	OK
3	FEC_Vdd (3.2V to 3.4V)	3.300	OK
4	FEC_I (1.2A to 1.6A)	1.28	OK
5	FEC_Vad (1.9V to 2.0V)	1.960	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean FAILED	STDDEV OK	FAIL
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2956	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3115	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2955	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3033	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3080	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2989	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3006	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3001	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 23.406 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.300 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.640 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: aa0000024ddea326

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 ( Aligned SCA_Write )
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xffffd	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xffffb	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	477.2	10.4	1 r	511.0	0.0
2 r	463.6	0.7	2 r	354.4	0.6	2 r	384.5	0.7	2 r	396.5	0.7	2 r	327.6	0.7	2 r	381.2	0.7	2 r	339.1	0.7	2 r	307.0	0.7
3	481.3	4.8	3	287.7	4.9	3	318.2	4.7	3	348.4	5.3	3	346.0	5.9	3	371.0	5.2	3	217.6	5.2	3	405.6	5.5
4	493.8	4.3	4	345.1	4.7	4	315.6	4.4	4	288.7	4.6	4	249.2	5.4	4	261.8	5.4	4	364.3	5.0	4	283.2	5.3
5	429.9	4.5	5	267.3	4.7	5	323.6	4.7	5	246.7	4.9	5	232.4	5.8	5	385.2	5.0	5	261.8	5.1	5	329.2	5.3
6	418.6	4.0	6	266.3	4.5	6	241.3	4.3	6	285.5	4.8	6	308.7	5.7	6	346.2	4.7	6	314.1	5.3	6	240.8	5.0
7	422.3	4.3	7	261.5	4.7	7	360.7	4.5	7	334.5	4.9	7	226.3	5.5	7	442.9	4.9	7	249.3	4.6	7	281.7	5.8
8	391.3	4.1	8	349.2	4.4	8	285.6	4.2	8	335.1	4.7	8	255.7	5.3	8	321.0	4.9	8	210.1	4.7	8	290.3	5.3
9	430.5	4.5	9	341.0	4.5	9	204.3	4.5	9	279.2	4.9	9	294.0	5.6	9	385.3	4.8	9	252.0	4.8	9	283.0	5.1
10	462.8	4.3	10	287.9	4.1	10	266.9	4.2	10	348.7	4.5	10	266.6	5.7	10	350.0	5.0	10	289.6	4.7	10	321.3	5.1
11	509.9	2.1	11	280.2	4.7	11	338.5	4.5	11	243.5	4.8	11	306.1	5.5	11	312.0	5.2	11	293.3	4.8	11	368.8	5.1
12	466.6	4.5	12	213.9	4.4	12	264.1	4.4	12	356.7	4.6	12	199.3	5.5	12	340.4	4.8	12	285.7	4.8	12	201.0	5.3
13	448.0	4.3	13	248.7	4.7	13	362.9	4.5	13	235.5	4.5	13	241.0	5.5	13	355.6	4.6	13	275.1	4.9	13	246.1	4.9
14	461.9	4.1	14	243.1	4.3	14	242.3	4.0	14	399.5	4.6	14	287.1	5.3	14	338.7	4.9	14	257.6	4.8	14	372.9	5.2
15 f	378.7	1.5	15 f	287.1	1.6	15 f	255.8	1.6	15 f	336.9	1.5	15 f	230.2	1.8	15 f	352.9	1.7	15 f	349.8	1.7	15 f	238.1	1.7
16	481.6	4.3	16	329.7	4.5	16	284.3	4.2	16	357.2	4.9	16	269.9	5.3	16	346.3	4.5	16	226.2	4.9	16	231.8	5.0
17	402.8	4.2	17	240.1	4.4	17	310.4	4.1	17	225.4	4.7	17	275.3	5.2	17	404.1	4.9	17	260.2	4.5	17	278.5	4.9
18	405.7	4.4	18	282.2	4.7	18	287.7	4.3	18	287.6	4.7	18	278.9	5.3	18	336.7	4.6	18	243.1	4.7	18	285.6	4.9
19	480.2	4.1	19	341.1	4.0	19	282.3	4.0	19	300.4	4.5	19	266.0	5.4	19	340.5	4.7	19	233.3	4.9	19	334.8	5.4
20	430.9	4.2	20	315.2	4.2	20	260.9	4.5	20	342.9	4.6	20	339.4	5.3	20	440.1	4.8	20	349.9	4.7	20	305.1	4.9
21	377.8	3.8	21	326.3	4.4	21	209.4	4.1	21	272.4	4.8	21	289.9	5.2	21	412.0	5.2	21	354.3	4.9	21	211.9	5.1
22	455.8	4.3	22	190.3	4.4	22	300.6	4.2	22	249.9	4.8	22	269.2	5.2	22	348.6	4.7	22	256.2	5.0	22	327.8	4.9
23	441.1	4.0	23	308.1	4.5	23	294.8	4.3	23	220.3	4.3	23	276.4	5.3	23	411.9	4.7	23	203.8	4.9	23	299.7	5.1
24	411.6	4.2	24	320.7	4.4	24	331.5	4.3	24	271.6	4.6	24	305.5	5.6	24	298.5	5.0	24	208.5	5.0	24	180.7	5.3
25	454.3	4.0	25	277.2	4.3	25	324.9	4.4	25	249.0	4.6	25	293.0	5.1	25	363.9	4.9	25	304.0	5.0	25	284.6	5.2
26	472.2	4.4	26	270.1	4.4	26	279.3	4.1	26	319.9	4.6	26	257.1	5.1	26	381.3	4.8	26	315.6	4.7	26	282.6	5.0
27	392.7	4.2	27	327.1	4.2	27	301.1	4.3	27	346.3	4.6	27	271.8	5.5	27	361.0	4.7	27	242.7	4.9	27	264.9	5.4
28 f	495.2	1.5	28 f	208.8	1.7	28 f	345.1	1.6	28 f	292.3	1.7	28 f	228.1	1.8	28 f	314.7	1.9	28 f	301.4	1.8	28 f	232.1	1.8
29	411.3	4.3	29	320.0	4.2	29	361.0	4.4	29	287.9	4.6	29	253.4	5.2	29	382.8	4.6	29	201.6	4.7	29	297.2	5.0
30	458.2	4.2	30	321.3	4.1	30	319.4	4.1	30	283.8	4.4	30	256.3	5.1	30	324.8	4.9	30	304.8	5.0	30	269.1	4.9
31	414.5	4.3	31	218.5	4.6	31	266.4	4.3	31	289.3	4.4	31	227.0	5.0	31	343.0	4.7	31	268.8	5.1	31	276.4	4.9
32	471.6	3.9	32	263.3	4.2	32	258.0	4.3	32	345.6	4.5	32	376.0	5.2	32	395.8	4.8	32	253.5	4.7	32	266.6	5.7
33	380.1	4.1	33	294.1	4.5	33	302.9	4.4	33	321.9	4.7	33	313.2	4.9	33	433.1	4.7	33	325.9	4.8	33	343.6	5.0
34	413.5	4.2	34	231.8	4.0	34	292.4	4.2	34	281.8	4.5	34	340.9	5.2	34	293.4	5.3	34	312.7	4.7	34	225.3	5.0
35	392.0	4.1	35	282.1	4.4	35	328.3	4.3	35	283.4	4.7	35	255.3	5.2	35	271.0	4.7	35	275.6	5.0	35	307.8	4.9
36	416.6	4.0	36	259.2	4.2	36	253.7	4.0	36	292.1	4.6	36	361.0	5.5	36	317.5	4.8	36	302.2	4.9	36	316.3	5.3
37	435.9	4.2	37	257.0	4.6	37	328.9	4.2	37	367.6	4.6	37	294.1	5.1	37	383.5	4.7	37	261.5	4.5	37	261.9	5.1
38	363.2	4.0	38	219.0	4.3	38	378.1	3.7	38	351.8	4.4	38	265.4	5.3	38	394.2	4.9	38	343.0	4.8	38	294.2	5.3
39	373.3	4.3	39	249.6	4.5	39	359.1	4.3	39	344.6	4.8	39	232.8	5.5	39	355.7	5.4	39	242.6	5.2	39	286.5	5.5
40	422.4	4.2	40	226.0	4.5	40	290.6	4.4	40	372.6	4.5	40	217.1	5.4	40	328.5	4.9	40	204.2	4.8	40	339.3	5.4
41	482.0	4.0	41	270.2	4.1	41	359.4	4.0	41	301.6	4.1	41	321.0	4.4	41	402.6	4.1	41	240.8	4.4	41	388.2	5.0
42	420.8	4.2	42	317.5	4.2	42	321.9	4.1	42	367.3	4.1	42	309.4	4.9	42	415.0	4.4	42	326.6	4.6	42	224.6	4.9
43	437.1	4.2	43	223.7	4.2	43	289.6	4.3	43	337.3	4.1	43	201.9	4.7	43	390.4	4.3	43	257.1	4.5	43	282.2	4.7
44	411.9	4.1	44	247.4	4.2	44	293.0	4.2	44	366.9	4.2	44	260.4	4.6	44	371.1	4.4	44	266.9	4.6	44	250.5	4.9
45	410.6	4.1	45	241.2	4.4	45	300.5	3.9	45	220.7	4.2	45	243.6	4.8	45	298.4	4.4	45	289.9	4.5	45	239.0	5.0
46	461.7	4.2	46	249.2	4.4	46	379.3	3.9	46	284.7	4.2	46	315.7	4.9	46	384.1	4.4	46	259.3	4.3	46	359.4	4.9
47	474.0	4.0	47	313.3	4.1	47	363.8	4.1	47	385.7	4.2	47	280.9	4.8	47	396.7	4.2	47	293.7	4.3	47	268.3	5.1
48	460.5	4.1	48	287.6	4.2	48	327.8	4.1	48	216.3	4.3	48	322.5	4.5	48	377.1	4.5	48	256.7	4.6	48	288.6	4.9
49	390.8	3.9	49	314.6	4.4	49	302.1	4.0	49	313.4	4.3	49	194.5	4.7	49	373.8	4.3	49	249.9	4.4	49	324.3	4.6
50	457.7	4.2	50	317.9	4.5	50	313.8	4.0	50	261.9	4.1	50	263.2	4.8	50	411.9	4.4	50	259.0	4.6	50	256.4	4.9
51	422.7	4.2	51	248.7	4.0	51	371.9	4.0	51	297.0	4.1	51	278.0	4.4	51	464.6	4.2	51	289.5	4.4	51	290.9	4.7
52	420.7	4.3	52	327.2	4.2	52	370.2	4.1	52	326.8	4.4	52	330.7	4.8	52	317.7	4.5	52	304.3	4.6	52	210.3	4.7
53 f	394.6	1.5	53 f	283.6	1.7	53 f	307.6	1.6	53 f	327.8	1.6	53 f	299.8	1.7	53 f	328.6	1.6	53 f	339.2	1.5	53 f	295.6	1.5
54	435.3	4.4	54	295.9	4.1	54	220.6	3.8	54	299.8	4.0	54	294.7	4.7	54	363.8	4.2	54	323.7	4.4	54	300.6	4.6
55	450.1	4.4	55	238.5	4.1	55	337.6	4.1	55	220.4	4.0	55	294.1	4.6	55	394.5	4.7	55	209.2	4.3	55	343.3	4.9
56	437.1	4.1	56	273.7	4.0	56	310.7	3.9	56	300.9	4.1	56	314.2	4.4	56	315.7	4.4	56	323.4	4.4	56	250.2	4.8
57	478.4	4.6	57	317.0	4.3	57	299.8	4.3	57	248.4	4.4	57	279.0	5.0	57	368.0	4.4	57	307.1	4.7	57	301.1	5.0
58	453.3	4.0	58	328.9	4.4	58	325.0	4.0	58	260.6	4.1	58	303.6	4.5</									



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	486.2	10.9	1 r	362.7	9.6	1 r	339.1	9.3	1 r	510.7	1.1	1 r	462.2	10.0	1 r	435.7	9.6	1 r	250.8	10.3	1 r	440.5	9.2
2 r	249.5	0.7	2 r	250.3	0.6	2 r	250.8	0.7	2 r	249.8	0.7	2 r	249.6	0.7	2 r	250.4	0.7	2 r	250.4	0.7	2 r	250.4	0.7
3	249.5	4.8	3	250.0	4.9	3	250.9	4.9	3	250.8	5.3	3	250.2	6.1	3	250.0	5.0	3	250.0	5.2	3	249.1	5.3
4	250.1	4.2	4	250.7	4.4	4	249.3	4.2	4	250.6	4.6	4	248.8	5.8	4	250.3	5.1	4	251.9	5.2	4	251.0	5.2
5	249.9	4.6	5	249.6	4.7	5	250.7	4.7	5	250.2	5.2	5	251.5	5.8	5	250.9	5.1	5	251.6	5.1	5	251.0	5.0
6	250.2	4.5	6	249.9	4.5	6	250.4	4.5	6	251.6	4.8	6	251.1	5.5	6	251.0	4.8	6	251.0	4.7	6	249.3	5.3
7	249.7	4.6	7	249.4	4.7	7	249.2	4.6	7	249.4	4.9	7	250.4	5.8	7	248.5	4.9	7	249.5	4.8	7	250.3	5.1
8	249.8	4.2	8	251.7	4.3	8	250.9	4.1	8	250.7	4.7	8	250.2	5.7	8	251.3	4.8	8	251.1	5.1	8	250.7	5.0
9	249.6	4.7	9	249.9	4.7	9	253.1	4.4	9	249.8	4.8	9	250.3	5.5	9	251.4	5.3	9	250.8	4.8	9	250.2	5.2
10	249.2	4.1	10	250.0	4.4	10	251.6	4.2	10	249.4	4.6	10	249.3	5.6	10	251.5	5.0	10	249.8	4.6	10	250.9	5.3
11	256.9	4.6	11	249.3	4.6	11	249.8	4.5	11	251.0	4.8	11	249.7	5.7	11	251.1	4.7	11	251.8	4.8	11	250.2	5.3
12	249.5	4.2	12	250.2	4.3	12	250.6	4.2	12	249.6	4.5	12	250.6	5.6	12	251.3	4.7	12	249.8	5.0	12	249.7	5.0
13	249.4	4.5	13	249.3	4.8	13	251.6	4.4	13	250.1	4.8	13	249.7	5.7	13	249.4	4.7	13	250.3	4.7	13	249.7	5.0
14	249.4	4.2	14	250.4	4.3	14	252.7	4.0	14	250.1	4.7	14	250.9	5.4	14	249.2	4.9	14	249.8	4.9	14	250.8	4.9
15 f	249.6	1.6	15 f	249.9	1.8	15 f	250.8	1.7	15 f	250.7	1.5	15 f	250.9	1.7	15 f	250.2	1.9	15 f	250.4	1.6	15 f	250.9	1.7
16	249.4	4.5	16	249.1	4.5	16	251.7	4.3	16	251.1	4.5	16	250.4	5.7	16	250.5	4.6	16	251.0	4.8	16	250.9	4.9
17	249.8	4.3	17	249.8	4.2	17	251.5	4.1	17	249.7	4.8	17	253.1	5.4	17	250.9	4.8	17	251.3	4.7	17	249.4	5.2
18	250.4	4.5	18	250.6	4.6	18	249.9	4.6	18	249.9	4.7	18	250.3	5.4	18	249.7	4.7	18	249.9	4.8	18	251.2	4.9
19	250.2	4.2	19	249.2	4.4	19	251.3	4.0	19	250.6	4.5	19	250.6	5.5	19	249.5	5.0	19	250.9	4.6	19	251.1	5.0
20	249.8	4.5	20	249.7	4.5	20	251.0	4.4	20	250.6	4.7	20	249.1	5.3	20	250.6	4.7	20	251.2	4.8	20	250.8	4.8
21	251.1	4.1	21	248.9	4.1	21	251.8	4.1	21	251.2	4.3	21	251.6	5.3	21	249.9	4.8	21	250.2	4.5	21	250.6	5.1
22	248.8	4.4	22	249.8	4.6	22	250.0	4.2	22	251.2	4.8	22	250.6	5.6	22	249.6	4.7	22	250.3	4.5	22	250.1	4.9
23	249.3	4.1	23	252.3	4.4	23	250.1	3.9	23	252.2	4.5	23	251.3	5.3	23	251.2	4.6	23	249.7	4.8	23	250.1	5.1
24	249.5	4.5	24	248.9	4.2	24	250.9	4.4	24	250.0	4.6	24	250.5	5.3	24	250.6	4.9	24	250.7	4.7	24	249.8	5.1
25	251.8	4.0	25	249.7	4.0	25	249.6	4.3	25	250.1	4.5	25	250.1	5.5	25	249.8	4.7	25	251.2	4.8	25	249.5	5.0
26	250.4	4.3	26	251.2	4.5	26	249.5	4.1	26	248.9	4.8	26	249.8	5.0	26	250.0	4.8	26	250.3	4.8	26	250.6	5.0
27	249.1	4.2	27	249.8	4.3	27	250.8	4.2	27	250.7	4.5	27	248.6	5.2	27	251.0	4.8	27	250.2	4.9	27	250.8	5.1
28 f	250.5	1.4	28 f	249.8	1.7	28 f	250.1	1.4	28 f	250.1	1.7	28 f	249.2	1.8	28 f	249.7	1.8	28 f	250.8	1.8	28 f	250.4	1.8
29	250.6	4.3	29	250.3	4.4	29	251.5	4.5	29	250.3	4.5	29	249.6	5.2	29	249.6	4.7	29	249.5	4.6	29	250.3	5.2
30	251.9	4.2	30	249.9	4.2	30	251.4	4.1	30	248.9	4.3	30	250.3	5.5	30	250.2	5.0	30	250.2	5.0	30	249.5	5.1
31	250.1	4.3	31	250.4	4.5	31	251.0	4.4	31	250.5	4.6	31	250.0	5.2	31	251.5	4.7	31	249.6	4.7	31	248.8	4.7
32	249.7	4.1	32	250.7	4.2	32	251.6	3.9	32	248.9	4.4	32	250.2	5.5	32	249.8	4.8	32	251.9	4.8	32	248.9	5.1
33	250.8	4.5	33	250.3	4.5	33	250.4	4.4	33	250.9	4.6	33	250.8	5.5	33	250.2	4.7	33	250.6	4.8	33	249.3	5.1
34	248.9	3.9	34	249.3	4.1	34	250.4	4.0	34	250.7	4.6	34	249.6	5.3	34	251.7	4.9	34	250.8	4.9	34	250.5	5.2
35	249.7	4.2	35	250.1	4.3	35	251.3	4.5	35	251.5	4.5	35	250.2	5.2	35	250.0	4.9	35	251.7	4.7	35	250.2	5.0
36	249.1	4.3	36	250.7	4.0	36	250.9	4.3	36	251.4	4.8	36	251.6	5.3	36	252.2	4.7	36	251.5	5.2	36	250.7	5.1
37	249.2	4.4	37	250.4	4.6	37	251.2	4.2	37	249.4	4.4	37	251.5	5.0	37	250.6	5.1	37	251.2	4.7	37	250.9	4.9
38	250.0	4.1	38	249.2	4.4	38	250.6	4.0	38	249.2	4.6	38	251.4	5.5	38	249.7	5.0	38	249.5	4.8	38	250.5	5.3
39	250.9	4.5	39	250.2	4.4	39	250.8	4.2	39	251.0	4.8	39	250.3	5.8	39	250.2	5.2	39	249.2	5.2	39	251.6	5.5
40	251.5	4.0	40	250.1	4.2	40	250.3	4.0	40	249.9	4.6	40	249.9	5.6	40	250.7	4.8	40	250.8	5.0	40	249.5	5.1
41	249.9	4.1	41	251.0	4.3	41	251.4	4.2	41	250.3	4.0	41	250.7	4.6	41	250.1	4.6	41	249.8	4.7	41	251.0	5.0
42	249.9	4.1	42	249.6	4.2	42	251.0	4.3	42	250.1	4.6	42	250.1	4.8	42	249.9	4.8	42	249.3	4.8	42	249.9	4.9
43	248.5	4.0	43	249.2	4.1	43	249.5	4.0	43	250.5	4.2	43	249.7	4.7	43	250.2	4.2	43	250.1	4.3	43	252.0	4.8
44	250.8	4.2	44	250.9	4.2	44	249.7	4.2	44	250.0	4.1	44	249.7	4.5	44	250.7	4.7	44	249.4	4.4	44	250.2	5.0
45	249.8	4.2	45	250.3	3.9	45	251.3	3.9	45	249.4	4.3	45	249.3	4.6	45	249.6	4.3	45	250.9	4.3	45	251.6	4.6
46	249.8	4.2	46	250.1	4.2	46	251.6	4.1	46	250.4	4.2	46	249.9	4.7	46	250.4	4.4	46	250.4	4.5	46	251.5	4.8
47	248.8	4.1	47	249.4	4.2	47	250.6	4.3	47	250.7	4.0	47	250.4	4.8	47	249.9	4.3	47	250.6	4.4	47	250.4	5.1
48	249.7	4.4	48	249.9	4.2	48	251.1	4.2	48	252.5	4.2	48	248.0	4.7	48	251.3	4.4	48	249.2	4.5	48	248.9	4.7
49	249.4	4.0	49	250.5	4.2	49	251.0	4.1	49	250.8	4.3	49	249.6	4.5	49	250.3	4.6	49	250.8	4.5	49	250.8	4.8
50	249.7	4.6	50	250.5	4.3	50	248.7	4.1	50	251.1	4.1	50	250.5	5.2	50	249.9	4.4	50	251.5	4.6	50	252.3	4.7
51	250.4	4.0	51	250.1	4.2	51	249.8	3.9	51	249.8	3.9	51	251.3	4.6	51	250.0	4.3	51	250.3	4.3	51	250.1	4.7
52	250.3	4.4	52	251.0	4.3	52	250.2	4.3	52	249.1	4.3	52	249.0	5.0	52	249.1	4.5	52	250.4	4.4	52	250.3	4.8
53 f	249.1	1.5	53 f	249.1	1.7	53 f	250.3	1.6	53 f	250.3	1.5	53 f	249.9	1.7	53 f	250.0	1.6	53 f	250.9	1.6	53 f	250.0	1.5
54	250.7	4.1	54	250.8	4.1	54	250.5	3.8	54	249.7	4.0	54	249.4	4.5	54	250.1	4.4	54	248.2	4.3	54	250.6	4.7
55	249.7	4.5	55	249.2	4.4	55	250.2	4.3	55	251.3	4.4	55	250.3	4.7	55	249.7	4.3	55	251.1	4.4	55	249.7	5.0
56	249.9	4.2	56	251.9	4.4	56	250.4	3.9	56	249.4	4.0	56	250.3	4.6	56	251.1	4.3	56	252.2	4.3	56	250.0	5.0
57	250.6	4.4	57	249.8	4.4	57	249.8	4.1	57	251.6	4.3	57	250.1	4.7	57	250.4	4.5	57	251.1	4.5	57	250.4	4.7
58	250.2	4.1	58	250.3	4.2	58	251.2	4.1	58	250.3	3.9												