

Fec test report:

Date: 2021-09-29 09:46:11

Tester name: lc

Test#1 Monitoring values

Passed

0	FEC label	034	OK
1	FEC DC2438 ID	aa0000024ddea326	OK
2	FEC_T (to 35°C)	22.562	OK
3	FEC_Vdd (3.2V to 3.4V)	3.300	OK
4	FEC_I (1.2A to 1.6A)	1.28	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean FAILED	STDDEV OK	FAIL
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2982	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3099	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2964	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3032	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3102	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2997	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3018	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2993	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 22.562 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.300 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.640 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: aa0000024ddea326

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 TdcM(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.960 V
66	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 TdcM(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.960 V
88	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.960 V
98	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 TdcM(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.960 V
110	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff0000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.960 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	477.4	10.3	1 r	511.0	0.0
2 r	462.1	0.7	2 r	355.9	0.6	2 r	384.8	0.7	2 r	396.9	0.7	2 r	327.7	0.7	2 r	381.2	0.7	2 r	340.4	0.7	2 r	307.1	0.7
3	479.3	4.6	3	289.4	5.0	3	318.6	4.6	3	347.1	4.8	3	346.9	5.8	3	370.8	5.0	3	218.8	4.9	3	405.1	5.2
4	492.0	4.1	4	347.2	4.4	4	315.1	4.1	4	288.3	4.6	4	248.1	5.6	4	262.0	4.8	4	365.8	4.9	4	282.4	4.9
5	429.0	4.6	5	267.3	4.5	5	323.9	4.8	5	247.9	4.9	5	232.4	5.8	5	385.1	4.7	5	263.8	5.1	5	328.7	5.0
6	418.5	4.1	6	267.2	4.3	6	240.3	4.5	6	284.9	4.8	6	308.1	5.5	6	345.9	4.8	6	315.5	5.0	6	239.5	4.9
7	419.9	4.4	7	261.5	4.5	7	359.5	4.6	7	334.8	4.7	7	226.5	5.5	7	441.0	4.9	7	249.2	4.5	7	281.3	5.0
8	389.1	4.2	8	350.1	4.4	8	285.6	4.3	8	336.2	4.5	8	255.5	5.6	8	321.4	4.7	8	211.1	5.2	8	289.6	4.9
9	428.2	4.3	9	342.1	4.6	9	204.3	4.4	9	278.7	4.5	9	294.7	5.2	9	385.9	4.8	9	252.7	4.8	9	282.5	4.9
10	461.4	4.1	10	288.6	4.3	10	267.2	4.2	10	349.1	4.7	10	266.1	5.6	10	350.9	4.7	10	288.6	4.8	10	321.2	5.0
11	509.5	2.5	11	280.0	4.4	11	338.1	4.4	11	243.9	4.8	11	306.0	5.3	11	310.1	4.7	11	294.2	4.6	11	368.7	4.8
12	464.0	4.0	12	215.8	4.3	12	265.2	4.2	12	354.9	4.5	12	199.4	5.5	12	340.3	4.8	12	285.9	5.1	12	199.9	4.8
13	445.1	4.3	13	249.8	4.5	13	363.2	4.1	13	236.6	4.6	13	239.8	5.4	13	355.6	4.7	13	275.1	4.8	13	245.4	4.9
14	459.9	4.1	14	243.5	4.4	14	243.0	4.1	14	399.4	4.5	14	286.1	5.3	14	337.4	4.7	14	257.9	4.8	14	372.9	4.9
15 f	376.9	1.5	15 f	287.7	1.8	15 f	256.1	1.6	15 f	337.1	1.5	15 f	230.4	1.7	15 f	352.8	1.7	15 f	252.8	1.6	15 f	238.5	1.7
16	479.2	4.6	16	330.6	4.2	16	283.9	4.4	16	357.5	4.5	16	270.3	5.2	16	346.5	4.5	16	227.9	4.5	16	232.3	4.5
17	400.8	4.1	17	240.8	4.4	17	310.3	4.1	17	224.8	4.4	17	276.2	5.3	17	403.3	4.7	17	261.2	4.8	17	277.7	5.0
18	404.4	4.2	18	283.1	4.4	18	287.5	4.4	18	287.3	4.4	18	279.4	5.4	18	335.6	4.6	18	244.8	4.6	18	285.7	4.6
19	478.4	4.2	19	341.1	4.4	19	280.9	3.8	19	300.3	4.5	19	265.1	5.5	19	339.8	4.8	19	235.2	4.7	19	335.1	4.8
20	429.2	4.0	20	316.7	4.2	20	260.8	4.3	20	342.9	4.8	20	338.7	5.4	20	439.3	4.6	20	351.9	4.6	20	304.6	4.8
21	376.6	4.1	21	325.6	4.2	21	208.1	4.1	21	272.2	4.5	21	290.3	5.5	21	412.3	4.6	21	355.1	4.5	21	211.4	4.8
22	453.6	4.1	22	190.8	4.2	22	300.7	4.1	22	250.0	4.6	22	268.0	5.4	22	349.1	4.8	22	258.2	4.4	22	326.9	4.5
23	438.8	4.2	23	310.9	4.3	23	295.9	4.2	23	221.7	4.2	23	276.7	5.6	23	410.9	4.5	23	204.0	4.8	23	299.5	4.8
24	409.7	4.1	24	321.9	4.3	24	329.2	4.1	24	271.0	4.3	24	304.1	5.1	24	298.7	4.5	24	208.6	4.5	24	180.3	4.8
25	452.1	3.9	25	278.0	4.2	25	325.1	4.1	25	250.0	4.5	25	292.8	5.2	25	364.0	4.5	25	305.0	4.7	25	284.2	4.9
26	471.7	4.1	26	270.7	4.2	26	279.3	4.3	26	319.8	4.3	26	256.3	4.7	26	381.7	4.7	26	316.6	4.5	26	282.6	4.8
27	390.2	4.1	27	328.4	4.1	27	300.9	4.2	27	345.8	4.2	27	270.3	5.6	27	361.8	4.7	27	243.9	4.6	27	264.2	4.8
28 f	494.2	1.6	28 f	209.6	1.8	28 f	345.5	1.5	28 f	292.3	1.7	28 f	227.3	1.9	28 f	314.6	1.8	28 f	302.1	1.8	28 f	231.8	1.9
29	409.3	4.0	29	322.8	4.2	29	361.4	4.3	29	287.8	4.5	29	254.1	5.0	29	383.6	4.5	29	202.4	4.7	29	296.3	4.8
30	456.8	4.3	30	323.6	4.1	30	320.4	4.1	30	283.5	4.5	30	255.8	5.3	30	324.6	4.8	30	305.6	4.5	30	268.5	5.0
31	412.7	4.1	31	217.9	4.4	31	266.5	4.1	31	289.9	4.5	31	227.1	5.0	31	343.1	4.5	31	270.2	4.8	31	276.3	4.8
32	469.2	4.1	32	264.2	4.1	32	258.2	4.0	32	345.2	4.0	32	376.5	5.3	32	395.4	4.7	32	254.3	4.6	32	266.4	5.0
33	378.3	4.1	33	295.7	4.3	33	304.2	4.3	33	322.3	4.5	33	311.7	5.1	33	433.7	4.4	33	325.6	4.5	33	343.6	4.9
34	409.8	4.1	34	233.5	4.0	34	292.6	3.9	34	282.2	4.2	34	340.9	5.2	34	294.6	5.0	34	314.2	4.8	34	224.4	4.8
35	388.8	4.2	35	282.4	4.1	35	328.8	4.4	35	283.6	4.4	35	254.8	5.0	35	271.1	4.8	35	277.4	4.5	35	307.4	4.6
36	414.3	3.9	36	260.4	4.1	36	253.2	4.0	36	292.6	4.3	36	361.8	5.5	36	317.5	4.9	36	303.4	5.2	36	317.0	5.0
37	432.3	4.3	37	258.4	4.1	37	329.4	4.3	37	366.6	4.3	37	294.7	5.0	37	383.2	4.5	37	263.4	4.5	37	262.8	4.7
38	361.1	3.9	38	220.3	4.1	38	379.1	3.9	38	351.3	4.5	38	266.7	5.4	38	393.4	4.8	38	344.0	5.0	38	294.4	4.8
39	370.6	4.5	39	250.2	4.3	39	358.2	4.2	39	345.3	4.6	39	231.9	5.4	39	355.3	5.0	39	241.9	5.0	39	286.6	5.6
40	419.9	3.8	40	226.4	4.0	40	290.8	4.1	40	372.1	4.3	40	215.6	5.4	40	328.2	4.6	40	206.5	4.9	40	338.2	5.1
41	479.9	4.0	41	271.8	4.1	41	359.7	3.9	41	301.6	4.1	41	321.2	4.7	41	402.2	4.2	41	241.8	4.3	41	388.5	4.5
42	419.5	4.0	42	318.4	4.2	42	322.6	4.2	42	366.4	4.4	42	308.3	4.7	42	414.3	4.2	42	326.8	4.3	42	224.8	4.4
43	434.5	4.1	43	226.3	3.9	43	290.0	3.9	43	337.0	4.1	43	202.9	4.6	43	390.3	4.4	43	258.5	4.2	43	283.9	4.5
44	411.2	4.1	44	248.0	4.1	44	293.0	4.2	44	366.8	4.2	44	260.8	4.7	44	369.6	4.7	44	267.8	4.2	44	248.8	4.7
45	409.3	4.0	45	242.2	3.8	45	300.3	3.7	45	221.1	4.0	45	242.3	4.4	45	297.8	4.0	45	291.3	4.4	45	239.5	4.4
46	459.5	4.5	46	251.2	4.2	46	380.1	3.7	46	284.7	3.9	46	316.7	4.5	46	383.8	4.2	46	260.5	4.1	46	359.3	4.6
47	471.0	3.9	47	313.3	4.1	47	363.8	3.9	47	386.8	3.9	47	281.0	4.4	47	395.5	4.2	47	295.0	4.4	47	268.6	4.5
48	459.2	4.4	48	288.6	4.1	48	327.0	4.3	48	216.7	4.3	48	322.1	4.6	48	376.5	4.2	48	258.3	4.2	48	287.8	4.4
49	388.9	3.8	49	317.8	4.0	49	303.7	3.9	49	313.8	3.9	49	194.0	4.5	49	373.5	4.3	49	251.0	4.4	49	323.4	4.5
50	455.7	4.4	50	319.9	4.1	50	312.1	3.8	50	262.6	4.0	50	263.3	4.4	50	409.7	4.2	50	261.0	4.7	50	257.7	4.5
51	420.6	4.1	51	249.9	3.9	51	371.0	3.9	51	296.9	3.9	51	277.6	4.4	51	464.0	4.3	51	290.8	4.2	51	291.2	4.4
52	419.8	4.1	52	329.4	4.1	52	369.0	4.1	52	326.0	4.1	52	328.8	4.6	52	316.5	4.1	52	305.1	4.4	52	209.9	4.4
53 f	392.4	1.5	53 f	284.9	1.5	53 f	308.4	1.7	53 f	327.8	1.5	53 f	299.4	1.4	53 f	328.1	1.4	53 f	340.5	1.4	53 f	295.9	1.6
54	433.5	4.2	54	296.7	4.1	54	221.1	3.7	54	299.1	4.0	54	294.3	4.4	54	363.4	4.2	54	324.7	4.4	54	300.5	4.7
55	447.5	4.2	55	239.2	4.3	55	337.8	4.0	55	220.1	4.2	55	294.6	4.5	55	394.6	4.3	55	210.3	4.5	55	342.6	4.4
56	435.6	4.0	56	275.1	3.9	56	310.7	3.6	56	301.9	4.0	56	314.2	4.5	56	315.7	4.4	56	326.0	4.4	56	248.6	4.6
57	476.2	4.3	57	317.1	4.3	57	299.8	4.0	57	249.3	4.0	57	279.7	4.6	57	367.9	4.3	57	308.8	4.3	57	300.7	4.5
58	451.9	4.0	58	331.3	4.0	58	325.3	3.9	58	260.9	4.2	58	302.5	4.3</									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	484.5	11.0	1 r	363.5	9.5	1 r	338.9	9.2	1 r	510.8	0.8	1 r	461.3	10.2	1 r	434.5	9.7	1 r	250.4	10.2	1 r	440.8	9.1
2 r	250.2	0.7	2 r	250.0	0.6	2 r	250.1	0.7	2 r	250.3	0.7	2 r	249.9	0.7	2 r	250.4	0.7	2 r	250.7	0.7	2 r	250.4	0.7
3	250.0	4.8	3	250.7	4.8	3	250.1	4.7	3	251.9	5.3	3	248.7	6.1	3	249.2	5.3	3	249.5	5.1	3	250.6	5.4
4	249.5	4.2	4	249.8	4.6	4	250.6	4.2	4	249.1	4.8	4	250.9	5.8	4	248.7	5.4	4	250.8	5.1	4	252.0	5.0
5	248.9	4.7	5	251.6	4.8	5	250.1	5.0	5	249.7	5.0	5	251.4	6.2	5	250.3	4.9	5	249.7	5.2	5	250.8	5.1
6	249.5	4.1	6	249.3	4.3	6	251.6	4.2	6	251.3	4.7	6	252.3	6.0	6	249.9	4.9	6	251.0	5.0	6	251.0	5.1
7	250.1	4.5	7	251.2	4.6	7	251.7	4.6	7	250.0	4.9	7	250.9	6.2	7	250.6	4.8	7	250.5	5.0	7	250.5	4.9
8	250.1	4.1	8	251.1	4.2	8	250.4	4.2	8	249.2	4.9	8	251.3	5.9	8	249.2	4.9	8	251.3	4.9	8	250.8	5.2
9	250.7	4.7	9	250.7	4.7	9	252.1	4.4	9	250.5	4.9	9	249.5	5.7	9	249.5	4.9	9	249.9	4.8	9	248.9	5.0
10	249.5	4.3	10	249.3	4.3	10	249.8	4.0	10	250.2	4.6	10	250.5	5.9	10	250.1	5.1	10	250.2	5.0	10	250.7	5.0
11	255.0	4.9	11	250.8	4.6	11	250.4	4.5	11	251.0	4.6	11	249.2	5.9	11	251.8	4.6	11	251.6	4.8	11	249.7	5.0
12	250.2	4.2	12	249.9	4.6	12	250.7	4.2	12	251.1	4.6	12	250.9	5.5	12	249.9	5.1	12	250.0	4.8	12	250.0	5.1
13	251.3	4.5	13	249.5	4.5	13	250.4	4.3	13	250.1	4.6	13	250.6	5.9	13	249.2	4.8	13	251.8	4.8	13	250.8	5.0
14	250.4	3.9	14	252.4	4.4	14	250.5	4.1	14	250.7	4.6	14	250.5	5.6	14	250.4	5.0	14	249.7	4.9	14	249.8	5.1
15 f	250.5	1.5	15 f	250.0	1.8	15 f	250.4	1.6	15 f	250.2	1.5	15 f	251.0	1.7	15 f	249.4	1.6	15 f	250.4	1.6	15 f	249.4	1.7
16	250.5	4.7	16	249.4	4.3	16	251.1	4.5	16	250.6	4.7	16	251.6	5.8	16	250.7	4.7	16	250.5	4.8	16	250.7	5.0
17	249.2	4.2	17	249.0	4.3	17	250.4	4.2	17	249.8	4.5	17	250.2	5.7	17	250.8	4.7	17	249.9	4.5	17	250.7	5.4
18	251.3	4.5	18	251.3	4.5	18	250.2	4.3	18	251.1	4.8	18	251.0	5.6	18	251.0	4.8	18	249.6	4.9	18	249.3	4.9
19	250.7	4.3	19	250.2	4.2	19	252.6	4.1	19	250.5	4.4	19	251.1	5.9	19	250.9	4.8	19	250.3	5.0	19	250.2	5.1
20	249.4	4.4	20	249.1	4.5	20	250.8	4.6	20	249.5	4.3	20	249.8	5.4	20	251.9	4.5	20	250.2	4.5	20	249.6	5.0
21	250.0	4.2	21	251.6	4.2	21	251.6	4.1	21	251.5	4.5	21	250.1	5.6	21	249.2	5.0	21	249.5	4.7	21	251.1	4.9
22	250.0	4.4	22	250.3	4.8	22	250.9	4.2	22	250.7	4.5	22	251.2	5.8	22	250.1	4.8	22	249.9	4.8	22	250.3	4.8
23	249.9	4.4	23	250.2	4.4	23	249.5	4.2	23	250.5	4.5	23	250.1	5.8	23	250.8	5.0	23	250.6	4.9	23	250.2	5.1
24	250.9	4.4	24	249.6	4.4	24	252.6	4.0	24	250.7	4.5	24	251.3	5.3	24	249.7	4.5	24	251.1	4.6	24	250.3	5.0
25	252.0	4.3	25	250.4	4.2	25	248.7	4.2	25	249.8	4.3	25	249.4	5.5	25	250.2	4.8	25	251.4	5.0	25	251.4	5.4
26	249.6	4.5	26	249.8	4.7	26	251.0	4.2	26	250.4	4.8	26	251.4	5.3	26	248.4	4.8	26	250.5	4.6	26	250.1	5.0
27	251.1	4.1	27	250.7	4.2	27	251.2	4.2	27	249.7	4.6	27	251.1	5.6	27	249.7	4.6	27	251.8	5.0	27	251.3	5.1
28 f	250.2	1.5	28 f	250.6	1.7	28 f	250.4	1.5	28 f	250.1	1.7	28 f	251.0	1.8	28 f	249.7	1.7	28 f	250.9	1.8	28 f	250.5	1.9
29	251.2	4.3	29	249.5	4.1	29	249.6	4.4	29	251.1	4.4	29	249.1	5.4	29	248.8	4.9	29	250.2	4.6	29	251.3	4.8
30	250.7	4.2	30	248.4	4.2	30	250.7	4.1	30	250.0	4.3	30	250.2	5.4	30	248.7	5.0	30	249.3	4.8	30	250.7	5.2
31	249.7	4.2	31	252.7	4.5	31	249.7	4.3	31	251.1	4.5	31	251.2	5.4	31	249.7	4.6	31	250.2	5.0	31	249.7	4.9
32	250.5	4.2	32	251.1	4.2	32	250.3	4.1	32	251.6	4.3	32	248.5	5.4	32	251.0	4.8	32	252.3	4.9	32	249.6	5.4
33	250.1	4.5	33	250.3	4.4	33	250.3	4.2	33	251.3	4.5	33	252.2	5.3	33	250.3	4.5	33	250.5	4.8	33	249.1	4.9
34	250.3	4.0	34	249.3	4.2	34	250.7	4.0	34	250.2	4.3	34	249.9	5.7	34	249.7	4.9	34	250.3	4.7	34	251.4	5.2
35	250.7	4.3	35	251.6	4.4	35	250.2	4.4	35	250.5	4.4	35	250.5	5.2	35	249.7	4.8	35	251.2	4.6	35	250.9	4.7
36	251.1	4.3	36	251.7	4.2	36	250.8	3.9	36	251.3	4.5	36	249.8	5.8	36	250.8	5.1	36	250.6	5.2	36	249.7	5.5
37	251.8	4.3	37	250.4	4.4	37	250.2	4.3	37	251.0	4.3	37	250.2	5.5	37	250.7	4.8	37	250.5	4.6	37	249.4	5.0
38	250.5	3.8	38	250.1	4.5	38	250.2	4.0	38	249.7	4.7	38	250.4	5.7	38	251.1	4.9	38	250.3	4.9	38	251.1	5.2
39	250.2	4.7	39	252.3	4.5	39	251.8	4.2	39	250.3	4.8	39	250.8	6.1	39	250.2	5.3	39	251.0	5.2	39	250.8	5.5
40	250.9	4.1	40	250.9	4.3	40	251.0	4.1	40	250.9	4.5	40	250.6	5.8	40	250.4	5.1	40	250.3	5.1	40	250.9	5.3
41	250.7	4.1	41	250.6	3.9	41	250.1	3.9	41	251.2	3.9	41	250.0	4.6	41	250.6	4.5	41	250.6	4.6	41	250.2	4.9
42	250.6	4.5	42	249.9	4.2	42	249.8	4.2	42	251.5	4.2	42	251.8	4.9	42	251.4	4.6	42	250.7	4.5	42	250.5	4.6
43	249.8	4.2	43	249.3	4.0	43	249.4	4.2	43	250.7	4.0	43	249.5	4.9	43	250.2	4.2	43	250.5	4.6	43	250.4	4.7
44	249.7	4.2	44	249.8	4.6	44	249.9	4.2	44	250.6	4.3	44	249.3	4.7	44	250.7	4.3	44	249.7	4.6	44	251.6	4.8
45	251.5	4.1	45	250.5	3.7	45	251.2	4.0	45	250.1	3.8	45	250.9	4.9	45	249.3	4.5	45	250.6	4.4	45	251.1	4.6
46	250.9	4.2	46	249.7	4.1	46	251.3	4.2	46	249.6	4.4	46	250.1	4.7	46	249.8	4.3	46	250.7	4.4	46	250.5	5.1
47	251.3	4.3	47	251.9	4.3	47	249.4	3.9	47	250.7	3.9	47	251.7	4.5	47	252.6	4.2	47	250.2	4.3	47	248.5	4.5
48	250.4	4.5	48	250.3	4.1	48	250.4	4.0	48	250.4	4.1	48	251.1	4.8	48	249.4	4.7	48	251.2	4.3	48	250.4	4.8
49	250.1	4.0	49	249.6	4.0	49	249.3	3.9	49	251.2	3.8	49	251.0	4.7	49	250.6	4.4	49	250.2	4.2	49	251.4	4.7
50	250.4	4.4	50	250.7	4.1	50	251.9	4.0	50	250.4	4.2	50	251.1	4.7	50	251.2	4.5	50	249.5	4.5	50	250.8	4.7
51	249.7	4.0	51	249.7	4.0	51	250.7	4.0	51	249.9	3.9	51	251.3	4.8	51	251.1	4.4	51	250.0	4.5	51	250.3	4.8
52	250.0	4.5	52	249.7	4.2	52	250.0	4.2	52	250.9	4.3	52	251.1	5.0	52	250.6	4.4	52	251.0	4.5	52	249.9	4.8
53 f	250.9	1.5	53 f	249.8	1.6	53 f	250.7	1.5	53 f	250.9	1.5	53 f	251.7	1.4	53 f	250.4	1.4	53 f	249.3	1.6	53 f	250.4	1.6
54	250.2	4.3	54	250.9	4.0	54	250.8	3.7	54	250.7	4.0	54	250.2	4.6	54	250.2	4.3	54	250.0	4.4	54	252.3	4.7
55	250.1	4.4	55	250.2	4.0	55	249.9	4.1	55	251.5	4.2	55	249.4	4.7	55	251.0	4.6	55	250.8	4.2	55	250.6	4.8
56	249.4	4.2	56	250.7	4.0	56	250.6	3.9	56	248.5	4.1	56	250.5	4.5	56	251.0	4.2	56	250.3	4.4	56	250.7	4.8
57	251.6	4.5	57	251.7	4.2	57	250.1	3.9	57	250.4	4.3	57	250.0	4.8	57	249.8	4.3	57	249.3	4.4	57	249.9	4.6
58	250.3	4.2	58	249.6	4.0	58	250.6	4.0	58	250.4	4.1												