

## Fec test report:

Date: 2021-09-21 08:55:19

Tester name: lc

### Test#1 Monitoring values

Passed

|   |                        |                  |    |
|---|------------------------|------------------|----|
| 0 | FEC label              | 034              | OK |
| 1 | FEC DC2438 ID          | aa0000024ddea326 | OK |
| 2 | FEC_T (to 35°C)        | 22.531           | OK |
| 3 | FEC_Vdd (3.2V to 3.4V) | 3.300            | OK |
| 4 | FEC_I (1.2A to 1.6A)   | 1.284            | OK |
| 5 | FEC_Vad (1.9V to 2.0V) | 1.950            | OK |

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpm 4.0)

|   |               |             |           |      |
|---|---------------|-------------|-----------|------|
| 0 | After chip #0 | Mean FAILED | STDDEV OK | FAIL |
| 1 | After chip #1 | Mean OK     | STDDEV OK | OK   |
| 2 | After chip #2 | Mean OK     | STDDEV OK | OK   |
| 3 | After chip #3 | Mean OK     | STDDEV OK | OK   |
| 4 | After chip #4 | Mean OK     | STDDEV OK | OK   |
| 5 | After chip #5 | Mean OK     | STDDEV OK | OK   |
| 6 | After chip #6 | Mean OK     | STDDEV OK | OK   |
| 7 | After chip #7 | Mean OK     | STDDEV OK | OK   |

### Test#4 AD9637 test patterns

Passed

|   |                |  |                   |    |
|---|----------------|--|-------------------|----|
| 0 | ADC channel #0 | P#1 (Midscale short 2048)              | MAX 2048 MIN 2048 | OK |
| 1 | ADC channel #1 | P#2 (+Full-scale short 4095)           | MAX 4095 MIN 4095 | OK |
| 2 | ADC channel #2 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 3 | ADC channel #3 | P#7 (One/zero-word toggle)             | MAX 4095 MIN 0    | OK |
| 4 | ADC channel #4 | P#1 (Midscale short 2048)              | MAX 2048 MIN 2048 | OK |
| 5 | ADC channel #5 | P#2 (+Full-scale short 4095)           | MAX 4095 MIN 4095 | OK |
| 6 | ADC channel #6 | P#4 (Checkerboard 1365 to 2730 toggle) | MAX 2730 MIN 1365 | OK |
| 7 | ADC channel #7 | P#7 (One/zero-word toggle)             | MAX 4095 MIN 0    | OK |

### Test#5 Pulser run

Passed

|   |               |                                   |                |    |
|---|---------------|-----------------------------------|----------------|----|
| 0 | After chip #0 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2966 | OK |
| 1 | After chip #1 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3096 | OK |
| 2 | After chip #2 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2955 | OK |
| 3 | After chip #3 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3035 | OK |
| 4 | After chip #4 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3077 | OK |
| 5 | After chip #5 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 2992 | OK |
| 6 | After chip #6 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3012 | OK |
| 7 | After chip #7 | DAC: 483 G(120) ADC(2850 to 3200) | ADC AMPL: 3002 | OK |

## FEC test final result:

Failed

| Monitoring test |                           |       |   |
|-----------------|---------------------------|-------|---|
| NO              | Command                   | Error | Response                                      |
| 0               | fe fec_enable 1           | 0     | 0 Tdc(2) Fem(00) Reg(1) <- 0x40000            |
| 1               | fe 0 moni T 0             | 0     | 0 Tdc(2) Fem(00) FEC_T: 22.531 degC           |
| 2               | fe 0 moni V 0             | 0     | 0 Tdc(2) Fem(00) FEC_Vdd: 3.300 V             |
| 3               | fe 0 pulser 0 model T2K2  | 0     | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)       |
| 4               | fe 0 pulser 0 base 0x3FFF | 0     | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff        |
| 5               | fe 0 pulser 0 load        | 0     | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed  |
| 6               | fe 0 moni A 0             | 0     | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V             |
| 7               | fe 0 moni I 0             | 0     | 0 Tdc(2) Fem(00) FEC_I: 0.642 A               |
| 8               | fe 0 moni S 0             | 0     | 0 Tdc(2) Fem(00) FEC_Serial: aa0000024ddea326 |

| Slow control registers test |  |       |   |
|-----------------------------|--|-------|---|
| NO                          | Command                                | Error | Response  |
| 0                           | fe 0 mode after                        | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x400  |
| 1                           | fe fec_enable 1                        | 0     | 0 Tdc(2) Fem(00) Reg(1) <- 0x40000                                      |
| 2                           | fe fec_enable                          | 0     | 0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1          |
| 3                           | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 4                           | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 5                           | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 6                           | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 7                           | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 8                           | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 9                           | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 10                          | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 11                          | fe 0 after 0 wrchk 3 0x0 0x0101 0x0101 | 0     | 0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified) |
| 12                          | fe 0 after 1 wrchk 3 0x0 0x0202 0x0202 | 0     | 0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified) |
| 13                          | fe 0 after 2 wrchk 3 0x0 0x0303 0x0303 | 0     | 0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified) |
| 14                          | fe 0 after 3 wrchk 3 0x0 0x0404 0x0404 | 0     | 0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified) |
| 15                          | fe 0 after 4 wrchk 3 0x0 0x0505 0x0505 | 0     | 0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified) |
| 16                          | fe 0 after 5 wrchk 3 0x0 0x0606 0x0606 | 0     | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified) |
| 17                          | fe 0 after 6 wrchk 3 0x0 0x0707 0x0707 | 0     | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified) |
| 18                          | fe 0 after 7 wrchk 3 0x0 0x0808 0x0808 | 0     | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified) |
| 19                          | fe 0 after 0 read 3                    | 0     | 0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101                       |
| 20                          | fe 0 after 1 read 3                    | 0     | 0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202                       |
| 21                          | fe 0 after 2 read 3                    | 0     | 0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303                       |
| 22                          | fe 0 after 3 read 3                    | 0     | 0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404                       |
| 23                          | fe 0 after 4 read 3                    | 0     | 0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505                       |
| 24                          | fe 0 after 5 read 3                    | 0     | 0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606                       |
| 25                          | fe 0 after 6 read 3                    | 0     | 0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707                       |
| 26                          | fe 0 after 7 read 3                    | 0     | 0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808                       |
| 27                          | fe 0 after 0 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 28                          | fe 0 after 1 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 29                          | fe 0 after 2 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 30                          | fe 0 after 3 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 31                          | fe 0 after 4 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 32                          | fe 0 after 5 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 33                          | fe 0 after 6 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |
| 34                          | fe 0 after 7 wrchk 3 0x0 0x0000 0x0000 | 0     | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)       |

| ADC pattern test |                          |       |  |
|------------------|--------------------------|-------|--|
| NO               | Command                  | Error | Response   |
| 0                | fe 0 mode after          | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x400   |
| 1                | fe 0 test_mode           | 0     | 0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0                      |
| 2                | be 0 state eb            | 0     | 0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current |
| 3                | be 0 state tg            | 0     | 0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )                  |
| 4                | be 0 state pm            | 0     | 0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )                   |
| 5                | fe 0 state               | 0     | 0 Tdc(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )                               |
| 6                | daq 0xFFFF F             | 0     | 0 Tdc(2): daq paused   |
| 7                | fe 0 emit_hit_cnt 0      | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x0   |
| 8                | fe 0 emit_empty_ch 0     | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0   |
| 9                | fe 0 emit_lst_cell_rd 0  | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0   |
| 10               | fe 0 keep_rst 0          | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x0   |
| 11               | fe 0 skip_rst 2          | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000   |
| 12               | fe adc 0 model AD9637    | 0     | 0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)   |
| 13               | fe adc 0 write 0x14 0x00 | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)                                |
| 14               | fe adc 0 write 0x4 0x00  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)                                |
| 15               | fe adc 0 write 0x5 0x01  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)                                |
| 16               | fe adc 0 write 0xD 0x01  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)                                |
| 17               | fe adc 0 write 0x4 0x00  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)                                |
| 18               | fe adc 0 write 0x5 0x02  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)                                |
| 19               | fe adc 0 write 0xD 0x02  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)                                |
| 20               | fe adc 0 write 0x4 0x00  | 0     | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)                                |

|    |                         |   |  |
|----|-------------------------|---|--|
| 21 | fe adc 0 write 0x5 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)                                  |
| 22 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)                                  |
| 23 | fe adc 0 write 0x4 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)                                  |
| 24 | fe adc 0 write 0x5 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)                                  |
| 25 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)                                  |
| 26 | fe adc 0 write 0x4 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)                                  |
| 27 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)                                  |
| 28 | fe adc 0 write 0xD 0x01 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)                                  |
| 29 | fe adc 0 write 0x4 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)                                  |
| 30 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)                                  |
| 31 | fe adc 0 write 0xD 0x02 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)                                  |
| 32 | fe adc 0 write 0x4 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)                                  |
| 33 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)                                  |
| 34 | fe adc 0 write 0xD 0x04 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)                                  |
| 35 | fe adc 0 write 0x4 0x08 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)                                  |
| 36 | fe adc 0 write 0x5 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)                                  |
| 37 | fe adc 0 write 0xD 0x07 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)                                  |
| 38 | fe 0 subtract_ped 0     | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0   |
| 39 | fe 0 zero_suppress 0    | 0 | 0 Tdc(2) Fem(00) Reg(0) <- 0x0   |
| 40 | fe 0 zs_pre_post 4 8    | 0 | 0 Tdc(2) Fem(00) Reg(5) <- 0xc4  |
| 41 | be 0 eb keep_fem_soe 0  | 0 | 0 Tdc(2) Reg(0) <- 0x0   |
| 42 | be 0 eb check_ev_nb 1   | 0 | 0 Tdc(2) Reg(0) <- 0x800000  |
| 43 | be 0 eb check_ev_ts 1   | 0 | 0 Tdc(2) Reg(0) <- 0x1000000   |
| 44 | be 0 eb ts_tolerance 0  | 0 | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0                 |
| 45 | be 0 event_limit 0x0    | 0 | 0 Tdc(2) Reg(6) <- 0x0   |
| 46 | be 0 trig_rate 0 50     | 0 | 0 Tdc(2) Reg(6) <- 0x32  |
| 47 | be 0 restart            | 0 | 0 Tdc(2) Reg(5) <- restart done  |
| 48 | be 0 isobus 0x60        | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)                    |
| 49 | be 0 trig_ena 1         | 0 | 0 Tdc(2) Reg(6) <- 0x1000  |
| 50 | be 0 trig_ena 0         | 0 | 0 Tdc(2) Reg(6) <- 0x0   |
| 51 | be 0 state eb           | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current) |
| 52 | be 0 state tg           | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )          |
| 53 | be 0 state pm           | 0 | 0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )                    |
| 54 | fe 0 state              | 0 | 0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )                                |
| 55 | fe adc 0 write 0x4 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)                                 |
| 56 | fe adc 0 write 0x5 0x0F | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)                                 |
| 57 | fe adc 0 write 0xD 0x00 | 0 | 0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)                                  |

| Pulser test |                                    |       |   |
|-------------|------------------------------------|-------|---|
| NO          | Command                            | Error | Response  |
| 0           | daq 0xFFFF F                       | 0     | 0 Tdc(2): daq paused  |
| 1           | fe 0 after 0:7 wrchk 3 0x0 0x0 0x0 | 0     | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified) |
| 2           | fe 0 after 0:7 wrchk 4 0x0 0x0 0x0 | 0     | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified) |
| 3           | fe 0 emit_hit_cnt 0                | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x0                                      |
| 4           | fe 0 emit_empty_ch 0               | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0                                      |
| 5           | fe 0 emit_lst_cell_rd 0            | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0                                      |
| 6           | fe 0 keep_rst 0                    | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x0                                      |
| 7           | fe 0 skip_rst 2                    | 0     | 0 Tdc(2) Fem(00) Reg(0) <- 0x40000                                  |
| 8           | fe 0 test_enable 0                 | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0                                      |
| 9           | fe 0 test_mode 1                   | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x400                                    |
| 10          | fe 0 tdata A 0x1FF                 | 0     | 0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510                |
| 11          | fe 0 test_zbt 0                    | 0     | 0 Tdc(2) Fem(00) Reg(5) <- 0x0                                      |
| 12          | fe 0 asic_mask 0x0                 | 0     | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                      |
| 13          | fe 0 asic_mask                     | 0     | 0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0                 |
| 14          | fe 0 pulser 0 enable 0             | 0     | 0 Tdc(2) Fem(00) Reg(3) <- 0x0                                      |
| 15          | fe 0 pulser 0 ft_enable 0          | 0     | 0 Tdc(2) Fem(00) Reg(3) <- 0x0                                      |
| 16          | fe 0 pulser 0 model T2K2           | 0     | 0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)                             |
| 17          | fe 0 pulser 0 base 16383           | 0     | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                              |
| 18          | fe 0 pulser 0 ampl 16383           | 0     | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff                         |
| 19          | fe 0 pulser 0 delay 3000           | 0     | 0 Tdc(2) Fem(00) Reg(3) <- 0xbb8                                    |
| 20          | fe pulser load                     | 0     | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                        |
| 21          | fe 0 pulser 0 enable 1             | 0     | 0 Tdc(2) Fem(00) Reg(3) <- 0x10000                                  |
| 22          | be 0 eb keep_fem_soe 0             | 0     | 0 Tdc(2) Reg(0) <- 0x0  |
| 23          | be 0 eb check_ev_nb 1              | 0     | 0 Tdc(2) Reg(0) <- 0x800000   |
| 24          | be 0 eb check_ev_ts 1              | 0     | 0 Tdc(2) Reg(0) <- 0x1000000  |
| 25          | be 0 eb ts_tolerance 0             | 0     | 0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0  |
| 26          | be 0 event_limit 0x0               | 0     | 0 Tdc(2) Reg(6) <- 0x0  |
| 27          | be 0 trig_rate 0 50                | 0     | 0 Tdc(2) Reg(6) <- 0x32   |
| 28          | be 0 trig_delay 0 0                | 0     | 0 Tdc(2) Reg(8) <- 0x0  |
| 29          | be 0 trig_delay 1 0                | 0     | 0 Tdc(2) Reg(8) <- 0x0  |
| 30          | be 0 trig_delay 2 0                | 0     | 0 Tdc(2) Reg(9) <- 0x0  |
| 31          | be 0 trig_delay 3 0                | 0     | 0 Tdc(2) Reg(9) <- 0x0  |
| 32          | be 0 ss_trig_delay 0x4             | 0     | 0 Tdc(2) Reg(14) <- 0x4   |
| 33          | be 0 ss_trig_ena 1                 | 0     | 0 Tdc(2) Reg(6) <- 0x10000  |
| 34          | be 0 restart                       | 0     | 0 Tdc(2) Reg(5) <- restart done                                     |
| 35          | be 0 restart                       | 0     | 0 Tdc(2) Reg(5) <- restart done                                     |
| 36          | be 0 isobus 0x0C                   | 0     | 0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)    |

|     |  |   |  |
|-----|--|---|--|
| 37  | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 38  | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 39  | fe 0 asic_mask 0xfffe                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000                                |
| 40  | fe 0 after 0 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration            |
| 41  | fe 0 after 0 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 42  | fe 0 after 0 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 43  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 44  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 45  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 46  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 47  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 48  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 49  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 50  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 51  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 52  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 53  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 54  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 55  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 56  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 57  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 58  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 59  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 60  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 61  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 62  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 63  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 64  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 65  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 66  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 67  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 68  | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 69  | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 70  | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 71  | fe 0 asic_mask 0xfffd                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffd0000                                |
| 72  | fe 0 after 1 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration            |
| 73  | fe 0 after 1 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 74  | fe 0 after 1 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 75  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 76  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 77  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 78  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 79  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 80  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 81  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 82  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 83  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 84  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 85  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 86  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 87  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 88  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 89  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 90  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 91  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 92  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 93  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 94  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 95  | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 96  | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 97  | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 98  | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 99  | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 100 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 101 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 102 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 103 | fe 0 asic_mask 0xfffb                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xfffb0000                                |
| 104 | fe 0 after 2 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration            |
| 105 | fe 0 after 2 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 106 | fe 0 after 2 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 107 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 108 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 109 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 110 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 111 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 112 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 113 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 114 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |

|     |  |   |  |
|-----|--|---|--|
| 115 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 116 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 117 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 118 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 119 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 120 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 121 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 122 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 123 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 124 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 125 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 126 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 127 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 128 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 129 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 130 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 131 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 132 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 133 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 134 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 135 | fe 0 asic_mask 0xff7                     | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffff0000                                |
| 136 | fe 0 after 3 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration            |
| 137 | fe 0 after 3 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 138 | fe 0 after 3 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 139 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 140 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 141 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 142 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 143 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 144 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 145 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 146 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 147 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 148 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 149 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 150 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 151 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 152 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 153 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 154 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 155 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 156 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 157 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 158 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 159 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 160 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 161 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 162 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 163 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 164 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 165 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 166 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 167 | fe 0 asic_mask 0xffef                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000                                |
| 168 | fe 0 after 4 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration            |
| 169 | fe 0 after 4 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 170 | fe 0 after 4 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 171 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 172 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 173 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 174 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 175 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 176 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 177 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 178 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 179 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 180 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 181 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 182 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 183 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 184 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 185 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 186 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 187 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 188 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 189 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 190 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 191 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 192 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |

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| 193 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 194 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 195 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 196 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 197 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 198 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 199 | fe 0 asic_mask 0xffdf                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000                                |
| 200 | fe 0 after 5 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration            |
| 201 | fe 0 after 5 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 202 | fe 0 after 5 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 203 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 204 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 205 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 206 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 207 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 208 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 209 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 210 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 211 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 212 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 213 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 214 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 215 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 216 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 217 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 218 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 219 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 220 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 221 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 222 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 223 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 224 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 225 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 226 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 227 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 228 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 229 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 230 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 231 | fe 0 asic_mask 0xffbf                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000                                |
| 232 | fe 0 after 6 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration            |
| 233 | fe 0 after 6 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 234 | fe 0 after 6 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 235 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 236 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 237 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 238 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 239 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 240 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 241 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 242 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.950 V                                    |
| 243 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 244 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 245 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 246 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 247 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 248 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 249 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 250 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 251 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 252 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 253 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 254 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 255 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 256 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 257 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 258 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |
| 259 | be 0 isobus 0x60                         | 0 | 0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)      |
| 260 | fe 0 asic_mask 0x0                       | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0x0                                       |
| 261 | fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)  |
| 262 | fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000 | 0 | 0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)  |
| 263 | fe 0 asic_mask 0xff7f                    | 0 | 0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000                                |
| 264 | fe 0 after 7 test_mode 0x1               | 0 | 0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration            |
| 265 | fe 0 after 7 wrchk 3 0x0 0x1000 0x0      | 0 | 0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified) |
| 266 | fe 0 after 7 wrchk 4 0x0 0x0 0x0         | 0 | 0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)    |
| 267 | fe 0 pulser 0 base 16383                 | 0 | 0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff                               |
| 268 | fe pulser 0 load                         | 0 | 0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                         |
| 269 | fe 0 moni A 0                            | 0 | 0 Tdc(2) Fem(00) FEC_Vad: 1.960 V                                    |
| 270 | fe 0 pulser 0 ampl 15900                 | 0 | 0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c                          |

|     |                          |   |  |
|-----|--------------------------|---|--|
| 271 | be 0 isobus 0x60         | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 272 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff                          |
| 273 | fe 0 pulser 0 load       | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                    |
| 274 | fe 0 moni A 0            | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V                               |
| 275 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c                     |
| 276 | be 0 isobus 0x60         | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 277 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff                          |
| 278 | fe 0 pulser 0 load       | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                    |
| 279 | fe 0 moni A 0            | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V                               |
| 280 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c                     |
| 281 | be 0 isobus 0x60         | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 282 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff                          |
| 283 | fe 0 pulser 0 load       | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                    |
| 284 | fe 0 moni A 0            | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V                               |
| 285 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c                     |
| 286 | be 0 isobus 0x60         | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 287 | fe 0 pulser 0 base 16383 | 0 | 0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff                          |
| 288 | fe 0 pulser 0 load       | 0 | 0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed                    |
| 289 | fe 0 moni A 0            | 0 | 0 Tdcm(2) Fem(00) FEC_Vad: 1.960 V                               |
| 290 | fe 0 pulser 0 ampl 15900 | 0 | 0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c                     |
| 291 | be 0 isobus 0x60         | 0 | 0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear) |
| 292 | fe 0 asic_mask 0x0       | 0 | 0 Tdcm(2) Fem(00) Reg(9) <- 0x0                                  |
| 293 | be 0 trig_ena 0          | 0 | 0 Tdcm(2) Reg(6) <- 0x0  |

## Pedestal data before centermean

| CHIP 0 |       |     | CHIP 1 |       |     | CHIP 2 |       |     | CHIP 3 |       |     | CHIP 4 |       |     | CHIP 5 |       |     | CHIP 6 |       |      | CHIP 7 |       |     |
|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|------|--------|-------|-----|
| CH     | M     | STD | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD  | CH     | M     | STD |
| 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0 | 0 r    | 0.0   | 0.0  | 0 r    | 0.0   | 0.0 |
| 1 r    | 511.0 | 0.0 | 1 r    | 511.0 | 0.0 | 1 r    | 511.0 | 0.0 | 1 r    | 511.0 | 0.0 | 1 r    | 511.0 | 0.0 | 1 r    | 511.0 | 0.0 | 1 r    | 476.9 | 10.2 | 1 r    | 511.0 | 0.0 |
| 2 r    | 463.7 | 0.7 | 2 r    | 353.8 | 0.6 | 2 r    | 384.1 | 0.7 | 2 r    | 396.0 | 0.7 | 2 r    | 326.2 | 0.7 | 2 r    | 380.9 | 0.7 | 2 r    | 339.2 | 0.7  | 2 r    | 305.8 | 0.7 |
| 3      | 480.9 | 5.0 | 3      | 287.9 | 4.8 | 3      | 317.3 | 4.5 | 3      | 346.8 | 5.6 | 3      | 345.6 | 6.2 | 3      | 370.2 | 5.1 | 3      | 217.6 | 5.1  | 3      | 403.2 | 5.7 |
| 4      | 491.5 | 4.2 | 4      | 343.9 | 4.5 | 4      | 315.4 | 4.2 | 4      | 287.5 | 4.8 | 4      | 246.8 | 5.8 | 4      | 262.0 | 5.3 | 4      | 365.7 | 5.1  | 4      | 282.4 | 5.2 |
| 5      | 430.5 | 4.8 | 5      | 266.4 | 4.8 | 5      | 323.6 | 4.7 | 5      | 246.7 | 5.1 | 5      | 230.8 | 6.2 | 5      | 384.0 | 5.1 | 5      | 263.1 | 5.2  | 5      | 326.9 | 5.1 |
| 6      | 418.9 | 4.2 | 6      | 263.7 | 4.3 | 6      | 240.4 | 4.5 | 6      | 285.1 | 5.1 | 6      | 308.1 | 5.8 | 6      | 344.3 | 5.1 | 6      | 313.6 | 4.9  | 6      | 238.0 | 5.3 |
| 7      | 421.3 | 4.6 | 7      | 259.6 | 4.8 | 7      | 360.5 | 4.7 | 7      | 333.2 | 4.7 | 7      | 225.6 | 5.7 | 7      | 441.4 | 5.0 | 7      | 248.0 | 5.0  | 7      | 280.2 | 5.1 |
| 8      | 390.1 | 4.0 | 8      | 347.9 | 4.2 | 8      | 285.5 | 4.4 | 8      | 334.1 | 4.7 | 8      | 254.1 | 5.9 | 8      | 321.1 | 4.9 | 8      | 210.9 | 5.1  | 8      | 289.0 | 5.1 |
| 9      | 429.9 | 4.4 | 9      | 340.8 | 4.6 | 9      | 204.7 | 4.6 | 9      | 278.9 | 4.9 | 9      | 291.6 | 5.7 | 9      | 384.5 | 5.5 | 9      | 250.8 | 5.0  | 9      | 282.0 | 5.2 |
| 10     | 461.4 | 4.3 | 10     | 286.1 | 4.4 | 10     | 266.4 | 4.2 | 10     | 348.7 | 4.9 | 10     | 264.6 | 5.9 | 10     | 351.0 | 5.2 | 10     | 288.7 | 5.0  | 10     | 320.4 | 5.2 |
| 11     | 510.0 | 2.0 | 11     | 277.6 | 4.4 | 11     | 337.8 | 4.5 | 11     | 243.8 | 4.6 | 11     | 304.3 | 5.7 | 11     | 310.2 | 4.8 | 11     | 293.1 | 4.9  | 11     | 367.4 | 5.3 |
| 12     | 465.7 | 4.1 | 12     | 212.3 | 4.2 | 12     | 263.7 | 4.2 | 12     | 354.5 | 5.0 | 12     | 197.9 | 5.7 | 12     | 339.4 | 4.9 | 12     | 284.9 | 5.0  | 12     | 197.9 | 5.1 |
| 13     | 447.1 | 4.7 | 13     | 246.4 | 5.0 | 13     | 362.3 | 4.3 | 13     | 234.8 | 5.0 | 13     | 238.8 | 5.6 | 13     | 354.9 | 4.8 | 13     | 274.7 | 5.1  | 13     | 245.3 | 5.0 |
| 14     | 461.4 | 4.1 | 14     | 241.8 | 4.1 | 14     | 242.3 | 4.0 | 14     | 397.6 | 4.7 | 14     | 285.3 | 5.8 | 14     | 336.5 | 4.8 | 14     | 256.2 | 4.7  | 14     | 370.9 | 5.3 |
| 15 f   | 378.9 | 1.5 | 15 f   | 285.6 | 1.8 | 15 f   | 255.2 | 1.6 | 15 f   | 335.9 | 1.5 | 15 f   | 228.7 | 1.8 | 15 f   | 352.3 | 1.7 | 15 f   | 250.5 | 1.7  | 15 f   | 236.9 | 1.7 |
| 16     | 481.6 | 4.5 | 16     | 328.4 | 4.4 | 16     | 284.1 | 4.5 | 16     | 356.9 | 4.7 | 16     | 267.1 | 5.5 | 16     | 346.1 | 4.9 | 16     | 226.7 | 4.7  | 16     | 230.6 | 4.8 |
| 17     | 402.1 | 4.2 | 17     | 238.2 | 4.2 | 17     | 310.0 | 4.2 | 17     | 224.9 | 4.8 | 17     | 274.5 | 5.6 | 17     | 404.3 | 5.0 | 17     | 260.5 | 4.8  | 17     | 277.4 | 5.0 |
| 18     | 405.3 | 4.5 | 18     | 280.1 | 4.6 | 18     | 287.3 | 4.5 | 18     | 285.6 | 4.9 | 18     | 277.1 | 5.5 | 18     | 335.1 | 4.7 | 18     | 242.7 | 5.3  | 18     | 283.8 | 5.0 |
| 19     | 478.4 | 4.2 | 19     | 339.1 | 4.3 | 19     | 281.3 | 4.2 | 19     | 299.5 | 4.6 | 19     | 263.7 | 5.6 | 19     | 339.1 | 5.0 | 19     | 233.0 | 5.0  | 19     | 333.2 | 5.5 |
| 20     | 430.4 | 4.3 | 20     | 313.9 | 4.7 | 20     | 260.4 | 4.5 | 20     | 342.0 | 4.7 | 20     | 336.4 | 5.6 | 20     | 439.2 | 5.0 | 20     | 350.9 | 4.9  | 20     | 303.2 | 4.9 |
| 21     | 377.6 | 4.3 | 21     | 324.7 | 4.2 | 21     | 208.6 | 4.1 | 21     | 271.7 | 4.6 | 21     | 288.4 | 5.6 | 21     | 410.4 | 5.0 | 21     | 353.2 | 4.9  | 21     | 211.2 | 4.9 |
| 22     | 454.8 | 4.2 | 22     | 188.0 | 4.5 | 22     | 300.4 | 4.3 | 22     | 248.6 | 4.7 | 22     | 266.4 | 5.6 | 22     | 348.6 | 4.7 | 22     | 256.0 | 4.7  | 22     | 326.6 | 4.9 |
| 23     | 440.6 | 4.2 | 23     | 308.9 | 4.5 | 23     | 296.2 | 4.2 | 23     | 220.6 | 4.6 | 23     | 274.3 | 5.5 | 23     | 410.6 | 4.9 | 23     | 202.3 | 4.7  | 23     | 297.2 | 5.1 |
| 24     | 411.2 | 4.4 | 24     | 319.2 | 4.7 | 24     | 329.7 | 4.2 | 24     | 269.9 | 4.5 | 24     | 303.2 | 5.3 | 24     | 299.2 | 4.8 | 24     | 208.8 | 4.7  | 24     | 178.2 | 4.8 |
| 25     | 454.7 | 4.2 | 25     | 275.1 | 4.3 | 25     | 324.1 | 4.1 | 25     | 248.3 | 4.8 | 25     | 290.8 | 5.5 | 25     | 362.7 | 5.0 | 25     | 303.9 | 4.8  | 25     | 283.7 | 5.3 |
| 26     | 472.0 | 4.4 | 26     | 269.2 | 4.5 | 26     | 278.1 | 4.3 | 26     | 318.3 | 4.7 | 26     | 254.6 | 5.2 | 26     | 381.5 | 4.9 | 26     | 314.9 | 4.7  | 26     | 281.3 | 5.0 |
| 27     | 392.3 | 4.3 | 27     | 325.6 | 4.2 | 27     | 300.8 | 4.1 | 27     | 345.6 | 4.6 | 27     | 270.1 | 5.6 | 27     | 360.8 | 4.8 | 27     | 243.4 | 5.2  | 27     | 262.9 | 5.2 |
| 28 f   | 495.0 | 1.5 | 28 f   | 207.8 | 1.8 | 28 f   | 344.7 | 1.4 | 28 f   | 291.0 | 1.7 | 28 f   | 225.5 | 1.8 | 28 f   | 314.4 | 1.7 | 28 f   | 301.1 | 2.1  | 28 f   | 230.5 | 1.8 |
| 29     | 410.9 | 4.4 | 29     | 318.8 | 4.3 | 29     | 361.0 | 4.4 | 29     | 287.6 | 4.6 | 29     | 251.2 | 5.5 | 29     | 381.5 | 4.8 | 29     | 200.0 | 4.7  | 29     | 295.4 | 5.2 |
| 30     | 458.2 | 4.0 | 30     | 320.0 | 4.2 | 30     | 319.2 | 4.0 | 30     | 282.6 | 4.7 | 30     | 254.7 | 5.3 | 30     | 324.1 | 4.8 | 30     | 304.7 | 5.1  | 30     | 267.2 | 4.9 |
| 31     | 415.1 | 4.2 | 31     | 216.4 | 4.9 | 31     | 265.4 | 4.0 | 31     | 288.5 | 4.5 | 31     | 226.5 | 5.3 | 31     | 342.7 | 4.8 | 31     | 267.9 | 4.8  | 31     | 274.4 | 4.7 |
| 32     | 470.6 | 4.0 | 32     | 262.7 | 4.3 | 32     | 256.3 | 3.9 | 32     | 344.2 | 4.5 | 32     | 374.8 | 5.6 | 32     | 395.2 | 4.9 | 32     | 253.6 | 4.9  | 32     | 263.6 | 5.2 |
| 33     | 380.2 | 4.2 | 33     | 293.4 | 4.6 | 33     | 302.8 | 4.2 | 33     | 320.9 | 4.7 | 33     | 310.4 | 5.4 | 33     | 432.2 | 4.8 | 33     | 325.9 | 4.8  | 33     | 341.5 | 4.8 |
| 34     | 410.6 | 4.0 | 34     | 230.4 | 4.3 | 34     | 293.4 | 4.1 | 34     | 280.8 | 4.7 | 34     | 338.6 | 5.8 | 34     | 293.0 | 5.1 | 34     | 312.9 | 5.0  | 34     | 224.1 | 5.3 |
| 35     | 391.1 | 4.4 | 35     | 280.3 | 4.3 | 35     | 328.2 | 4.3 | 35     | 282.4 | 4.6 | 35     | 253.1 | 5.0 | 35     | 272.0 | 4.8 | 35     | 277.1 | 4.8  | 35     | 305.4 | 5.0 |
| 36     | 415.1 | 3.9 | 36     | 258.6 | 4.2 | 36     | 252.6 | 4.3 | 36     | 292.0 | 4.7 | 36     | 360.4 | 5.6 | 36     | 317.2 | 4.9 | 36     | 303.4 | 5.2  | 36     | 315.6 | 5.2 |
| 37     | 433.7 | 4.2 | 37     | 256.4 | 4.5 | 37     | 329.2 | 4.2 | 37     | 365.5 | 4.7 | 37     | 293.5 | 5.3 | 37     | 382.9 | 4.8 | 37     | 261.6 | 4.6  | 37     | 261.9 | 4.9 |
| 38     | 362.9 | 4.0 | 38     | 216.6 | 4.4 | 38     | 378.2 | 3.9 | 38     | 349.6 | 4.6 | 38     | 265.1 | 5.6 | 38     | 392.9 | 5.1 | 38     | 342.3 | 4.9  | 38     | 291.9 | 5.3 |
| 39     | 372.4 | 4.6 | 39     | 248.9 | 4.4 | 39     | 357.4 | 4.2 | 39     | 343.6 | 4.9 | 39     | 230.5 | 6.0 | 39     | 355.8 | 5.7 | 39     | 241.2 | 5.4  | 39     | 285.9 | 5.5 |
| 40     | 422.4 | 4.0 | 40     | 224.1 | 4.1 | 40     | 290.5 | 4.2 | 40     | 371.6 | 4.9 | 40     | 214.7 | 5.7 | 40     | 328.1 | 5.0 | 40     | 204.2 | 4.9  | 40     | 337.3 | 5.5 |
| 41     | 480.8 | 4.0 | 41     | 269.2 | 4.0 | 41     | 359.6 | 3.8 | 41     | 300.1 | 4.0 | 41     | 319.7 | 4.7 | 41     | 402.2 | 4.4 | 41     | 240.5 | 4.3  | 41     | 388.0 | 4.7 |
| 42     | 421.0 | 4.2 | 42     | 317.0 | 4.1 | 42     | 321.7 | 4.0 | 42     | 364.9 | 4.5 | 42     | 306.8 | 4.8 | 42     | 414.4 | 4.4 | 42     | 325.8 | 4.7  | 42     | 222.3 | 4.7 |
| 43     | 435.8 | 3.9 | 43     | 223.5 | 4.2 | 43     | 288.7 | 4.0 | 43     | 335.7 | 3.9 | 43     | 201.7 | 4.9 | 43     | 389.7 | 4.6 | 43     | 256.9 | 4.3  | 43     | 281.5 | 4.8 |
| 44     | 411.3 | 4.1 | 44     | 245.3 | 4.2 | 44     | 292.0 | 4.1 | 44     | 365.9 | 4.2 | 44     | 258.0 | 4.8 | 44     | 369.1 | 4.2 | 44     | 264.6 | 4.5  | 44     | 248.5 | 4.8 |
| 45     | 410.9 | 4.1 | 45     | 239.8 | 4.0 | 45     | 299.5 | 3.8 | 45     | 219.3 | 4.0 | 45     | 242.1 | 4.6 | 45     | 297.4 | 4.2 | 45     | 284.8 | 4.3  | 45     | 237.8 | 4.7 |
| 46     | 461.4 | 4.2 | 46     | 249.2 | 4.2 | 46     | 379.0 | 4.1 | 46     | 283.6 | 4.1 | 46     | 315.3 | 4.7 | 46     | 382.9 | 4.5 | 46     | 259.4 | 4.6  | 46     | 357.4 | 4.7 |
| 47     | 473.4 | 4.1 | 47     | 312.0 | 4.1 | 47     | 362.9 | 3.8 | 47     | 386.3 | 4.4 | 47     | 280.1 | 4.8 | 47     | 396.5 | 4.5 | 47     | 294.0 | 4.5  | 47     | 266.5 | 4.8 |
| 48     | 461.6 | 4.4 | 48     | 286.2 | 4.1 | 48     | 326.6 | 4.0 | 48     | 216.5 | 4.2 | 48     | 320.4 | 4.4 | 48     | 375.8 | 4.4 | 48     | 257.3 | 4.4  | 48     | 285.9 | 4.9 |
| 49     | 389.6 | 3.9 | 49     | 315.2 | 3.9 | 49     | 302.1 | 3.9 | 49     | 312.7 | 4.0 | 49     | 192.7 | 4.7 | 49     | 374.9 | 4.5 | 49     | 249.2 | 4.5  | 49     | 322.2 | 4.6 |
| 50     | 456.8 | 4.3 | 50     | 318.8 | 4.2 | 50     | 312.3 | 4.0 | 50     | 261.8 | 4.2 | 50     | 262.1 | 4.7 | 50     | 409.0 | 4.7 | 50     | 259.4 | 4.4  | 50     | 256.6 | 4.9 |
| 51     | 423.8 | 4.1 | 51     | 248.0 | 4.0 | 51     | 370.9 | 3.8 | 51     | 295.6 | 4.4 | 51     | 276.6 | 4.8 | 51     | 463.7 | 4.3 | 51     | 288.5 | 4.5  | 51     | 289.5 | 4.7 |
| 52     | 420.2 | 4.3 | 52     | 325.9 | 4.3 | 52     | 368.9 | 4.4 | 52     | 325.3 | 4.2 | 52     | 328.1 | 4.8 | 52     | 316.2 | 4.3 | 52     | 303.2 | 4.4  | 52     | 208.8 | 4.9 |
| 53 f   | 394.2 | 1.5 | 53 f   | 282.4 | 1.4 | 53 f   | 307.5 | 1.6 | 53 f   | 327.6 | 1.5 | 53 f   | 298.8 | 1.4 | 53 f   | 328.4 | 1.5 | 53 f   | 338.6 | 1.5  | 53 f   | 294.5 | 1.5 |
| 54     | 435.6 | 4.2 | 54     | 294.6 | 3.9 | 54     | 219.7 | 3.8 | 54     | 298.2 | 3.8 | 54     | 293.3 | 4.5 | 54     | 363.1 | 4.3 | 54     | 322.8 | 4.3  | 54     | 298.4 | 4.7 |
| 55     | 449.6 | 4.3 | 55     | 238.4 | 4.2 | 55     | 336.3 | 4.2 | 55     | 219.9 | 4.4 | 55     | 291.3 | 4.5 | 55     | 394.0 | 4.7 | 55     | 208.6 | 4.4  | 55     | 340.6 | 4.7 |
| 56     | 436.6 | 4.1 | 56     | 273.7 | 3.7 | 56     | 310.4 | 3.8 | 56     | 298.6 | 4.2 | 56     | 313.0 | 4.6 | 56     | 316.0 | 4.4 | 56     | 323.8 | 4.3  | 56     | 247.4 | 4.7 |
| 57     | 478.1 | 4.3 | 57     | 316.4 | 4.2 | 57     | 300.6 | 4.2 | 57     | 248.3 | 4.2 | 57     | 277.3 | 4.8 | 57     | 367.5 | 4.5 | 57     | 307.1 | 4.5  | 57     | 300.3 | 4.9 |
| 58     | 453.4 | 4.2 | 58     | 327.8 | 3.9 | 58     | 324.7 | 4.1 | 58     | 258.9 | 3.9 | 58     | 301.1 | 5.  |        |       |     |        |       |      |        |       |     |



Pedestal after centermean.

| CHIP 0 |       |      | CHIP 1 |       |     | CHIP 2 |       |     | CHIP 3 |       |     | CHIP 4 |       |      | CHIP 5 |       |     | CHIP 6 |       |      | CHIP 7 |       |     |
|--------|-------|------|--------|-------|-----|--------|-------|-----|--------|-------|-----|--------|-------|------|--------|-------|-----|--------|-------|------|--------|-------|-----|
| CH     | M     | STD  | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD | CH     | M     | STD  | CH     | M     | STD | CH     | M     | STD  | CH     | M     | STD |
| 0 r    | 250.0 | 0.0  | 0 r    | 250.0 | 0.0 | 0 r    | 250.0 | 0.0 | 0 r    | 250.0 | 0.0 | 0 r    | 250.0 | 0.0  | 0 r    | 250.0 | 0.0 | 0 r    | 250.0 | 0.0  | 0 r    | 250.0 | 0.0 |
| 1 r    | 485.7 | 11.1 | 1 r    | 363.6 | 9.8 | 1 r    | 338.9 | 9.3 | 1 r    | 510.7 | 1.1 | 1 r    | 460.6 | 10.1 | 1 r    | 435.7 | 9.7 | 1 r    | 250.1 | 10.2 | 1 r    | 439.5 | 9.2 |
| 2 r    | 249.8 | 0.7  | 2 r    | 249.9 | 0.6 | 2 r    | 250.7 | 0.7 | 2 r    | 250.3 | 0.7 | 2 r    | 250.4 | 0.7  | 2 r    | 249.9 | 0.7 | 2 r    | 250.4 | 0.7  | 2 r    | 250.1 | 0.7 |
| 3      | 249.7 | 4.8  | 3      | 250.6 | 5.2 | 3      | 251.2 | 4.6 | 3      | 250.9 | 5.3 | 3      | 249.1 | 6.2  | 3      | 250.5 | 5.3 | 3      | 249.6 | 5.0  | 3      | 251.2 | 5.3 |
| 4      | 252.2 | 4.0  | 4      | 250.4 | 4.4 | 4      | 249.9 | 4.2 | 4      | 249.5 | 4.7 | 4      | 251.2 | 5.7  | 4      | 249.4 | 5.2 | 4      | 248.6 | 5.1  | 4      | 250.5 | 5.0 |
| 5      | 250.7 | 4.5  | 5      | 250.7 | 4.9 | 5      | 250.2 | 4.5 | 5      | 249.6 | 5.0 | 5      | 250.6 | 5.7  | 5      | 250.9 | 4.7 | 5      | 250.6 | 5.2  | 5      | 250.6 | 5.1 |
| 6      | 251.1 | 4.3  | 6      | 251.3 | 4.4 | 6      | 251.2 | 4.2 | 6      | 250.8 | 5.0 | 6      | 250.1 | 5.5  | 6      | 251.8 | 5.0 | 6      | 251.6 | 5.1  | 6      | 251.1 | 5.3 |
| 7      | 250.7 | 4.6  | 7      | 252.2 | 4.7 | 7      | 249.7 | 4.4 | 7      | 250.9 | 4.8 | 7      | 248.2 | 5.5  | 7      | 250.3 | 4.9 | 7      | 251.7 | 4.8  | 7      | 252.1 | 5.1 |
| 8      | 251.0 | 4.2  | 8      | 251.0 | 4.2 | 8      | 251.6 | 4.2 | 8      | 250.6 | 4.8 | 8      | 250.2 | 6.0  | 8      | 250.8 | 5.0 | 8      | 249.9 | 5.0  | 8      | 250.0 | 4.9 |
| 9      | 251.3 | 4.3  | 9      | 250.7 | 4.8 | 9      | 250.8 | 4.5 | 9      | 250.9 | 5.0 | 9      | 249.8 | 5.5  | 9      | 250.3 | 4.9 | 9      | 250.5 | 4.8  | 9      | 250.3 | 5.2 |
| 10     | 250.9 | 4.1  | 10     | 250.6 | 4.5 | 10     | 251.2 | 4.1 | 10     | 248.8 | 4.9 | 10     | 249.0 | 5.7  | 10     | 249.8 | 5.1 | 10     | 249.6 | 4.8  | 10     | 249.7 | 5.3 |
| 11     | 257.0 | 4.5  | 11     | 250.6 | 4.7 | 11     | 250.7 | 4.4 | 11     | 248.7 | 4.6 | 11     | 251.0 | 5.4  | 11     | 251.8 | 4.9 | 11     | 250.5 | 5.0  | 11     | 250.6 | 5.1 |
| 12     | 250.9 | 4.1  | 12     | 250.3 | 4.4 | 12     | 251.1 | 4.0 | 12     | 250.8 | 4.7 | 12     | 250.3 | 5.4  | 12     | 251.4 | 4.7 | 12     | 250.4 | 5.0  | 12     | 250.7 | 5.3 |
| 13     | 249.6 | 4.7  | 13     | 251.1 | 4.6 | 13     | 251.8 | 4.6 | 13     | 250.2 | 4.8 | 13     | 250.4 | 5.5  | 13     | 250.2 | 4.8 | 13     | 251.3 | 4.8  | 13     | 250.9 | 4.9 |
| 14     | 251.1 | 4.2  | 14     | 251.2 | 4.7 | 14     | 250.7 | 4.1 | 14     | 250.2 | 4.8 | 14     | 251.3 | 5.7  | 14     | 250.4 | 4.9 | 14     | 251.4 | 5.1  | 14     | 250.5 | 5.3 |
| 15 f   | 249.7 | 1.6  | 15 f   | 249.8 | 1.6 | 15 f   | 250.7 | 1.6 | 15 f   | 250.5 | 1.5 | 15 f   | 250.2 | 1.7  | 15 f   | 250.7 | 1.6 | 15 f   | 250.4 | 1.7  | 15 f   | 250.7 | 1.7 |
| 16     | 249.7 | 4.4  | 16     | 250.4 | 4.2 | 16     | 249.6 | 4.7 | 16     | 250.4 | 4.7 | 16     | 251.8 | 5.4  | 16     | 250.2 | 4.6 | 16     | 251.0 | 4.7  | 16     | 251.0 | 5.0 |
| 17     | 250.1 | 4.2  | 17     | 250.9 | 4.1 | 17     | 250.1 | 4.0 | 17     | 248.8 | 4.6 | 17     | 251.3 | 5.7  | 17     | 251.0 | 5.1 | 17     | 249.3 | 4.8  | 17     | 250.5 | 5.2 |
| 18     | 251.3 | 4.5  | 18     | 251.8 | 4.6 | 18     | 251.2 | 4.3 | 18     | 251.4 | 4.7 | 18     | 251.1 | 5.2  | 18     | 251.8 | 4.7 | 18     | 250.9 | 4.9  | 18     | 250.2 | 5.0 |
| 19     | 251.0 | 4.1  | 19     | 249.3 | 4.1 | 19     | 251.3 | 4.1 | 19     | 249.7 | 4.6 | 19     | 251.7 | 5.6  | 19     | 251.3 | 4.8 | 19     | 249.2 | 4.8  | 19     | 250.9 | 5.1 |
| 20     | 251.6 | 4.7  | 20     | 250.2 | 4.5 | 20     | 251.5 | 4.3 | 20     | 251.2 | 4.5 | 20     | 251.1 | 5.3  | 20     | 250.1 | 4.5 | 20     | 250.8 | 5.1  | 20     | 251.2 | 4.7 |
| 21     | 250.6 | 4.0  | 21     | 250.1 | 4.1 | 21     | 249.3 | 4.2 | 21     | 249.7 | 4.6 | 21     | 251.1 | 5.4  | 21     | 250.3 | 4.8 | 21     | 251.3 | 4.7  | 21     | 250.3 | 5.0 |
| 22     | 251.2 | 4.3  | 22     | 251.7 | 4.5 | 22     | 251.7 | 4.4 | 22     | 250.6 | 4.7 | 22     | 251.7 | 5.2  | 22     | 250.1 | 4.7 | 22     | 251.6 | 4.6  | 22     | 250.0 | 4.9 |
| 23     | 249.8 | 4.0  | 23     | 250.2 | 4.3 | 23     | 249.3 | 4.2 | 23     | 250.6 | 4.5 | 23     | 251.4 | 5.4  | 23     | 250.5 | 5.0 | 23     | 252.5 | 5.0  | 23     | 251.9 | 5.0 |
| 24     | 250.7 | 4.4  | 24     | 250.5 | 4.3 | 24     | 251.2 | 4.2 | 24     | 250.4 | 4.6 | 24     | 251.0 | 5.4  | 24     | 250.2 | 4.6 | 24     | 248.9 | 4.8  | 24     | 251.3 | 4.9 |
| 25     | 250.0 | 4.0  | 25     | 252.2 | 4.2 | 25     | 250.2 | 4.2 | 25     | 251.0 | 4.5 | 25     | 251.0 | 5.4  | 25     | 250.9 | 5.1 | 25     | 251.7 | 5.0  | 25     | 250.5 | 5.1 |
| 26     | 251.0 | 4.4  | 26     | 249.6 | 4.4 | 26     | 251.9 | 4.3 | 26     | 251.3 | 4.7 | 26     | 249.8 | 5.1  | 26     | 250.0 | 4.6 | 26     | 249.8 | 4.8  | 26     | 250.8 | 5.0 |
| 27     | 250.2 | 4.1  | 27     | 250.6 | 4.2 | 27     | 250.1 | 4.2 | 27     | 250.2 | 4.6 | 27     | 249.3 | 5.5  | 27     | 251.2 | 4.8 | 27     | 250.0 | 5.0  | 27     | 250.2 | 4.9 |
| 28 f   | 250.7 | 1.5  | 28 f   | 250.0 | 1.9 | 28 f   | 250.6 | 1.4 | 28 f   | 250.7 | 1.6 | 28 f   | 251.5 | 1.8  | 28 f   | 250.5 | 1.8 | 28 f   | 250.7 | 1.8  | 28 f   | 251.2 | 1.8 |
| 29     | 250.5 | 4.3  | 29     | 251.7 | 4.7 | 29     | 249.6 | 4.3 | 29     | 250.7 | 4.5 | 29     | 250.8 | 5.3  | 29     | 251.4 | 4.8 | 29     | 251.2 | 4.8  | 29     | 250.3 | 4.8 |
| 30     | 250.6 | 4.0  | 30     | 250.9 | 4.3 | 30     | 252.0 | 4.0 | 30     | 250.2 | 4.8 | 30     | 249.9 | 5.6  | 30     | 251.5 | 4.9 | 30     | 249.9 | 4.8  | 30     | 251.2 | 5.2 |
| 31     | 250.1 | 4.2  | 31     | 252.2 | 4.6 | 31     | 253.5 | 4.2 | 31     | 249.5 | 4.5 | 31     | 250.5 | 5.1  | 31     | 249.8 | 4.5 | 31     | 251.9 | 4.8  | 31     | 251.1 | 4.7 |
| 32     | 250.6 | 4.2  | 32     | 250.4 | 4.3 | 32     | 253.7 | 4.3 | 32     | 250.6 | 4.5 | 32     | 249.4 | 5.3  | 32     | 250.3 | 4.9 | 32     | 249.8 | 4.9  | 32     | 250.6 | 5.1 |
| 33     | 250.3 | 4.4  | 33     | 250.1 | 4.3 | 33     | 251.2 | 4.2 | 33     | 250.1 | 4.5 | 33     | 252.1 | 5.0  | 33     | 251.9 | 4.5 | 33     | 250.4 | 4.7  | 33     | 249.1 | 4.9 |
| 34     | 251.9 | 3.9  | 34     | 251.3 | 4.1 | 34     | 250.1 | 4.1 | 34     | 251.0 | 4.7 | 34     | 250.2 | 5.5  | 34     | 251.3 | 5.0 | 34     | 249.8 | 4.8  | 34     | 249.4 | 5.0 |
| 35     | 251.1 | 4.3  | 35     | 249.8 | 4.6 | 35     | 250.5 | 4.0 | 35     | 251.6 | 4.5 | 35     | 251.1 | 5.1  | 35     | 249.3 | 4.9 | 35     | 249.9 | 4.8  | 35     | 251.9 | 4.7 |
| 36     | 252.7 | 4.0  | 36     | 249.7 | 4.0 | 36     | 250.9 | 4.0 | 36     | 250.0 | 5.0 | 36     | 251.3 | 5.5  | 36     | 251.1 | 5.0 | 36     | 250.5 | 5.0  | 36     | 249.5 | 5.0 |
| 37     | 251.2 | 4.3  | 37     | 250.5 | 4.5 | 37     | 250.2 | 4.1 | 37     | 251.8 | 4.3 | 37     | 251.0 | 5.3  | 37     | 249.9 | 4.5 | 37     | 250.6 | 4.7  | 37     | 249.4 | 5.0 |
| 38     | 250.0 | 4.0  | 38     | 251.4 | 4.3 | 38     | 250.4 | 3.8 | 38     | 250.4 | 4.5 | 38     | 250.6 | 5.5  | 38     | 251.0 | 5.1 | 38     | 250.6 | 5.1  | 38     | 252.0 | 5.1 |
| 39     | 250.2 | 4.4  | 39     | 251.4 | 4.7 | 39     | 252.0 | 4.3 | 39     | 251.0 | 4.9 | 39     | 251.4 | 5.7  | 39     | 249.4 | 5.4 | 39     | 251.9 | 5.2  | 39     | 250.1 | 5.6 |
| 40     | 250.2 | 3.9  | 40     | 251.7 | 4.4 | 40     | 250.6 | 4.0 | 40     | 250.2 | 4.4 | 40     | 249.9 | 5.6  | 40     | 250.8 | 5.1 | 40     | 251.0 | 5.1  | 40     | 250.3 | 5.2 |
| 41     | 250.9 | 3.9  | 41     | 251.2 | 3.9 | 41     | 250.3 | 4.0 | 41     | 251.2 | 4.0 | 41     | 250.7 | 4.8  | 41     | 249.8 | 4.3 | 41     | 250.2 | 4.5  | 41     | 250.7 | 4.8 |
| 42     | 249.3 | 4.0  | 42     | 249.0 | 4.0 | 42     | 249.9 | 4.0 | 42     | 251.0 | 4.2 | 42     | 249.9 | 4.6  | 42     | 250.6 | 4.4 | 42     | 250.8 | 4.3  | 42     | 251.5 | 4.8 |
| 43     | 250.2 | 4.0  | 43     | 251.8 | 3.8 | 43     | 250.5 | 3.9 | 43     | 250.8 | 4.1 | 43     | 249.1 | 4.7  | 43     | 250.5 | 4.1 | 43     | 251.3 | 4.4  | 43     | 250.7 | 4.5 |
| 44     | 250.8 | 4.1  | 44     | 251.5 | 4.0 | 44     | 249.8 | 4.4 | 44     | 250.6 | 4.2 | 44     | 251.3 | 4.5  | 44     | 251.2 | 4.4 | 44     | 252.1 | 4.8  | 44     | 250.9 | 4.7 |
| 45     | 249.2 | 4.1  | 45     | 250.4 | 3.8 | 45     | 250.6 | 3.9 | 45     | 252.6 | 4.1 | 45     | 249.8 | 4.6  | 45     | 250.1 | 4.3 | 45     | 250.2 | 4.2  | 45     | 251.6 | 4.7 |
| 46     | 250.1 | 4.0  | 46     | 250.1 | 4.3 | 46     | 251.2 | 3.8 | 46     | 250.7 | 4.3 | 46     | 250.8 | 4.5  | 46     | 251.4 | 4.2 | 46     | 251.6 | 4.2  | 46     | 251.4 | 4.5 |
| 47     | 251.3 | 4.1  | 47     | 250.6 | 4.1 | 47     | 251.4 | 3.7 | 47     | 249.4 | 4.2 | 47     | 250.7 | 4.5  | 47     | 250.3 | 4.1 | 47     | 250.7 | 4.4  | 47     | 250.8 | 4.7 |
| 48     | 248.3 | 4.2  | 48     | 250.6 | 4.1 | 48     | 250.3 | 4.2 | 48     | 249.6 | 4.2 | 48     | 251.0 | 4.5  | 48     | 251.8 | 4.3 | 48     | 250.7 | 4.4  | 48     | 251.1 | 4.6 |
| 49     | 251.0 | 3.9  | 49     | 250.6 | 4.2 | 49     | 251.0 | 3.9 | 49     | 250.3 | 4.0 | 49     | 250.5 | 4.4  | 49     | 249.4 | 4.4 | 49     | 251.2 | 4.7  | 49     | 250.8 | 4.8 |
| 50     | 251.1 | 4.4  | 50     | 250.3 | 4.1 | 50     | 250.8 | 3.8 | 50     | 250.2 | 3.9 | 50     | 250.2 | 4.6  | 50     | 252.7 | 4.4 | 50     | 250.4 | 4.4  | 50     | 251.4 | 4.8 |
| 51     | 249.4 | 4.0  | 51     | 250.1 | 3.9 | 51     | 250.5 | 3.9 | 51     | 249.8 | 4.0 | 51     | 250.5 | 4.6  | 51     | 250.5 | 4.2 | 51     | 251.4 | 4.2  | 51     | 250.5 | 4.5 |
| 52     | 250.6 | 4.2  | 52     | 251.4 | 4.0 | 52     | 251.0 | 4.4 | 52     | 250.4 | 4.1 | 52     | 251.6 | 4.8  | 52     | 250.4 | 4.5 | 52     | 250.7 | 4.6  | 52     | 249.9 | 4.9 |
| 53 f   | 250.5 | 1.7  | 53 f   | 250.2 | 1.6 | 53 f   | 250.5 | 1.6 | 53 f   | 249.4 | 1.5 | 53 f   | 249.7 | 1.5  | 53 f   | 250.1 | 1.5 | 53 f   | 249.7 | 1.7  | 53 f   | 250.8 | 1.6 |
| 54     | 249.3 | 4.3  | 54     | 250.8 | 4.0 | 54     | 251.0 | 3.8 | 54     | 250.4 | 4.2 | 54     | 249.4 | 4.6  | 54     | 250.5 | 4.3 | 54     | 249.6 | 4.3  | 54     | 251.9 | 4.5 |
| 55     | 250.4 | 4.5  | 55     | 249.7 | 4.1 | 55     | 252.0 | 4.2 | 55     | 250.9 | 4.2 | 55     | 252.0 | 4.5  | 55     | 250.8 | 4.4 | 55     | 251.6 | 4.7  | 55     | 250.5 | 4.6 |
| 56     | 250.1 | 4.4  | 56     | 250.5 | 3.9 | 56     | 250.4 | 3.8 | 56     | 251.2 | 4.0 | 56     | 249.9 | 4.6  | 56     | 250.3 | 4.1 | 56     | 249.9 | 4.3  | 56     | 251.4 | 4.7 |
| 57     | 250.9 | 4.4  | 57     | 249.2 | 4.2 | 57     | 249.5 | 4.0 | 57     | 251.1 | 4.4 | 57     | 251.2 | 4.8  | 57     | 250.5 | 4.5 | 57     | 251.0 | 4.4  | 57     | 250.0 | 5.0 |
| 58     | 251.2 | 4.0  | 58     | 250.9 | 4.0 | 58     | 249.9 | 4.0 | 58     | 251.4 | 4.1 |        |       |      |        |       |     |        |       |      |        |       |     |