

## Fec test report:

Date: 2021-10-07 16:00:39

Tester name: Boris

### Test#1 Monitoring values

Failed

0	FEC label	031	OK
1	FEC DC2438 ID	340000024dd73726	OK
2	FEC_T (to 35°C)	23.719	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.192	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2996	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2999	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3063	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3032	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3046	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3019	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3040	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3089	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 23.719 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.596 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: 340000024dd73726

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 TdcM(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 TdcM(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	506.9	5.4	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	381.2	0.7	2 r	388.0	0.6	2 r	370.4	0.7	2 r	349.5	0.7	2 r	405.3	0.7	2 r	347.8	0.7	2 r	389.9	0.7	2 r	312.7	0.7
3	330.3	4.8	3	418.5	4.8	3	285.5	5.2	3	291.0	5.0	3	390.5	5.3	3	285.8	4.8	3	265.9	4.8	3	263.0	5.2
4	379.8	4.4	4	358.4	4.5	4	200.2	4.5	4	302.7	4.8	4	347.1	5.3	4	305.6	4.5	4	247.7	4.5	4	180.9	5.0
5	347.4	4.8	5	342.4	4.6	5	294.3	4.7	5	345.6	5.0	5	388.0	5.4	5	276.1	4.8	5	280.1	4.6	5	226.2	5.1
6	268.0	4.4	6	364.3	4.4	6	308.7	4.2	6	372.1	5.1	6	419.7	5.0	6	286.4	4.8	6	280.2	4.4	6	183.6	4.8
7	337.4	4.8	7	425.0	4.8	7	286.1	4.5	7	384.2	4.8	7	351.1	5.0	7	275.5	4.4	7	260.7	4.5	7	219.6	5.0
8	326.1	4.5	8	365.2	4.1	8	249.6	4.4	8	264.8	4.9	8	385.5	5.0	8	242.9	4.8	8	360.7	4.5	8	184.0	5.2
9	350.9	4.7	9	369.0	4.7	9	306.9	4.5	9	249.7	4.8	9	398.3	5.0	9	281.8	4.8	9	299.9	4.4	9	195.7	4.9
10	252.5	4.4	10	391.2	4.3	10	281.0	4.1	10	327.3	4.5	10	404.6	4.9	10	323.9	4.5	10	263.2	4.5	10	210.9	4.9
11	323.5	4.5	11	344.3	4.3	11	296.4	4.7	11	319.7	4.8	11	403.1	5.0	11	334.5	4.5	11	282.6	4.4	11	263.7	4.9
12	293.8	4.2	12	383.8	4.3	12	306.2	4.3	12	370.4	4.3	12	444.9	5.1	12	338.2	4.4	12	308.3	4.6	12	206.7	5.0
13	365.1	4.6	13	343.1	4.5	13	218.7	4.3	13	338.6	4.7	13	355.2	4.9	13	220.5	4.9	13	238.7	4.5	13	219.8	5.0
14	310.5	4.2	14	347.8	4.4	14	174.3	4.3	14	345.3	4.5	14	349.4	4.8	14	262.6	4.5	14	332.7	4.4	14	147.3	5.0
15 f	288.4	1.7	15 f	380.6	1.6	15 f	335.1	1.6	15 f	326.4	1.6	15 f	316.9	1.5	15 f	300.3	1.5	15 f	269.5	1.5	15 f	293.7	1.6
16	384.7	4.5	16	399.2	4.3	16	179.1	4.6	16	302.7	4.7	16	423.0	4.6	16	320.6	4.5	16	275.7	4.3	16	167.6	4.8
17	376.4	4.2	17	379.9	4.3	17	224.4	4.2	17	334.5	4.5	17	349.2	4.8	17	295.2	4.3	17	332.4	4.3	17	280.8	4.8
18	342.8	4.3	18	340.4	4.4	18	197.0	4.4	18	329.9	4.6	18	389.8	4.6	18	264.7	4.3	18	320.0	4.4	18	137.4	4.8
19	380.4	4.3	19	371.0	4.2	19	322.8	4.2	19	284.6	4.7	19	392.6	5.0	19	289.3	4.3	19	291.9	4.4	19	265.5	4.9
20	245.6	4.2	20	355.8	4.4	20	260.2	4.3	20	241.8	4.5	20	349.7	4.9	20	345.1	4.4	20	310.1	4.6	20	250.1	4.9
21	400.9	4.1	21	334.1	4.1	21	233.4	4.2	21	333.5	4.6	21	331.4	4.6	21	261.5	4.5	21	309.0	4.4	21	270.7	4.6
22	408.0	4.4	22	314.6	4.3	22	273.0	4.3	22	317.2	4.7	22	358.1	4.6	22	233.4	4.4	22	272.1	4.2	22	177.2	4.6
23	363.3	4.3	23	334.3	3.9	23	262.9	4.3	23	309.2	4.5	23	372.2	4.7	23	263.5	4.3	23	313.5	4.4	23	261.7	4.8
24	306.4	5.0	24	379.1	4.3	24	251.9	4.5	24	309.9	4.4	24	270.2	4.8	24	289.5	4.5	24	289.8	4.2	24	283.6	4.7
25	440.2	4.2	25	333.2	4.2	25	283.7	4.3	25	217.8	4.4	25	419.7	4.7	25	228.3	4.3	25	262.8	4.2	25	281.8	4.9
26	281.2	4.5	26	328.2	4.3	26	331.4	4.4	26	288.8	4.5	26	347.0	4.6	26	331.9	4.4	26	248.1	4.2	26	176.4	4.9
27	297.1	4.5	27	366.2	4.1	27	192.8	4.3	27	339.9	4.6	27	313.6	4.9	27	230.5	4.4	27	327.5	4.5	27	224.4	4.7
28 f	317.2	1.7	28 f	343.4	1.7	28 f	224.7	1.7	28 f	342.0	1.7	28 f	413.9	1.6	28 f	230.9	1.5	28 f	243.7	1.6	28 f	210.7	1.7
29	329.7	4.4	29	389.8	4.4	29	274.4	4.4	29	315.4	4.7	29	334.1	4.6	29	254.5	4.5	29	275.8	4.1	29	208.8	4.7
30	384.3	4.2	30	361.6	3.9	30	291.9	4.1	30	314.6	4.2	30	398.7	4.7	30	289.6	4.5	30	317.0	4.4	30	159.6	4.8
31	417.4	4.5	31	368.7	4.2	31	224.4	4.4	31	328.8	4.3	31	367.8	4.7	31	222.0	4.5	31	264.0	4.3	31	221.7	4.7
32	398.1	4.3	32	308.2	3.8	32	212.2	4.0	32	314.8	4.2	32	316.6	4.8	32	246.0	4.6	32	320.9	4.7	32	203.1	4.7
33	378.4	4.5	33	439.3	4.2	33	229.4	4.2	33	307.7	4.9	33	322.9	4.7	33	267.7	4.5	33	308.6	4.2	33	225.0	4.9
34	363.6	4.2	34	376.2	4.1	34	288.1	4.0	34	261.5	4.3	34	316.1	4.8	34	371.1	4.2	34	270.5	4.3	34	181.1	4.8
35	369.8	4.3	35	311.6	4.1	35	267.5	4.5	35	362.6	4.4	35	446.5	4.5	35	251.1	4.3	35	277.3	4.3	35	200.4	4.9
36	319.9	4.3	36	405.9	4.3	36	210.7	4.2	36	287.6	4.4	36	317.9	5.1	36	235.9	4.5	36	322.4	4.7	36	234.5	4.9
37	341.1	4.3	37	387.0	4.5	37	263.1	4.5	37	312.3	4.8	37	350.0	4.8	37	204.4	4.7	37	304.2	4.2	37	255.2	4.7
38	299.1	4.2	38	422.9	4.0	38	226.6	4.1	38	282.6	4.3	38	319.8	4.8	38	261.8	4.8	38	310.9	4.5	38	194.8	4.7
39	367.6	4.5	39	318.6	4.4	39	306.2	4.2	39	283.8	4.9	39	393.6	5.2	39	273.6	4.9	39	339.1	4.8	39	168.5	5.1
40	326.3	4.3	40	406.3	4.2	40	225.3	4.1	40	267.0	4.3	40	351.8	4.8	40	347.9	4.3	40	291.1	4.2	40	351.5	4.9
41	357.6	4.0	41	364.6	4.0	41	284.6	4.0	41	292.3	4.1	41	393.9	4.4	41	276.4	4.2	41	335.7	4.0	41	317.8	4.6
42	361.5	4.2	42	367.2	4.0	42	261.6	4.0	42	258.1	4.0	42	299.6	4.5	42	316.2	4.3	42	324.3	4.2	42	201.3	4.9
43	369.2	4.0	43	332.3	3.7	43	221.3	3.9	43	363.1	3.9	43	246.6	4.2	43	325.6	4.1	43	273.7	3.9	43	262.3	4.7
44	402.4	4.4	44	300.9	3.9	44	252.5	4.2	44	307.9	4.2	44	370.5	4.4	44	255.1	4.0	44	278.1	4.2	44	234.4	4.8
45	323.2	4.2	45	389.2	3.9	45	326.0	3.8	45	285.9	4.2	45	397.7	4.2	45	264.7	4.2	45	357.5	4.0	45	223.0	4.4
46	351.1	4.5	46	373.9	4.0	46	340.8	4.0	46	348.4	4.4	46	399.9	4.2	46	232.1	4.5	46	332.9	4.1	46	241.8	4.5
47	334.1	4.2	47	381.2	3.9	47	241.9	4.1	47	293.1	4.0	47	377.4	4.2	47	320.5	4.0	47	261.6	3.9	47	263.2	4.5
48	389.1	4.2	48	363.9	3.9	48	285.4	4.2	48	325.5	4.3	48	382.7	4.2	48	307.4	4.2	48	250.9	4.2	48	238.3	4.7
49	330.7	4.2	49	423.8	3.9	49	192.9	4.3	49	281.6	3.9	49	376.6	4.2	49	275.3	4.3	49	302.2	4.1	49	225.8	4.5
50	339.9	4.1	50	290.1	4.2	50	247.3	4.0	50	265.0	4.2	50	370.0	4.4	50	226.8	4.2	50	322.2	4.2	50	169.7	4.5
51	361.2	4.0	51	398.3	3.7	51	222.3	3.8	51	282.4	3.8	51	316.1	4.4	51	338.1	4.1	51	310.0	4.2	51	284.0	4.7
52	306.9	4.5	52	387.7	4.1	52	201.8	4.2	52	334.5	4.2	52	334.5	4.3	52	277.7	4.0	52	264.1	4.4	52	157.5	4.8
53 f	341.9	1.4	53 f	437.1	1.4	53 f	234.6	1.4	53 f	251.3	1.7	53 f	354.8	1.5	53 f	279.2	1.5	53 f	382.2	1.4	53 f	202.7	1.5
54	359.7	4.1	54	343.3	3.8	54	259.9	3.8	54	285.6	4.4	54	369.9	4.2	54	353.2	4.3	54	296.0	4.2	54	205.1	4.4
55	380.9	4.4	55	427.6	4.0	55	281.8	3.9	55	282.4	4.0	55	392.1	4.4	55	280.6	4.1	55	302.2	4.0	55	130.5	4.7
56	302.8	4.2	56	359.6	4.2	56	292.2	4.0	56	358.9	3.9	56	407.8	4.2	56	259.0	4.0	56	288.2	4.0	56	213.4	4.5
57	388.0	4.2	57	403.4	4.0	57	312.4	4.1	57	283.9	4.2	57	339.0	4.3	57	253.0	3.9	57	266.8	4.3	57	214.1	4.7
58	398.2	4.2	58	372.8	3.8	58	201.3	3.8	58	288.3	4.0	58	342.3	4.3									



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	412.7	8.2	1 r	426.2	11.1	1 r	382.4	9.2	1 r	257.1	11.9	1 r	462.3	11.0	1 r	431.6	7.6	1 r	376.0	8.3	1 r	385.3	6.7
2 r	250.3	0.7	2 r	249.8	0.7	2 r	250.6	0.7	2 r	250.5	0.7	2 r	250.3	0.7	2 r	249.9	0.7	2 r	249.9	0.7	2 r	249.8	0.7
3	249.2	4.9	3	249.0	4.9	3	249.8	5.0	3	250.1	5.2	3	249.6	5.4	3	248.8	4.9	3	248.7	5.0	3	250.1	5.1
4	249.9	4.3	4	249.1	4.5	4	250.6	4.2	4	250.1	4.5	4	250.1	5.1	4	250.0	4.7	4	249.5	4.7	4	249.0	5.0
5	251.0	4.8	5	249.8	4.6	5	249.8	4.5	5	250.0	4.8	5	248.8	5.3	5	249.0	4.6	5	249.8	4.6	5	249.3	5.0
6	250.0	4.5	6	250.1	4.4	6	250.4	4.3	6	248.5	4.8	6	249.6	5.0	6	250.2	4.5	6	248.8	4.6	6	250.3	4.7
7	250.6	4.8	7	248.4	4.8	7	250.9	4.7	7	249.6	5.0	7	250.7	5.0	7	249.2	4.6	7	249.3	4.4	7	248.1	5.2
8	248.7	4.3	8	250.2	4.2	8	249.2	4.1	8	249.4	4.8	8	250.5	5.0	8	249.1	4.6	8	249.7	4.5	8	249.6	4.8
9	248.7	4.7	9	249.8	4.4	9	250.0	4.7	9	251.1	4.8	9	249.8	4.7	9	249.8	4.6	9	249.7	4.7	9	250.3	5.0
10	249.0	4.4	10	249.6	4.3	10	250.5	4.4	10	250.8	4.7	10	249.3	4.9	10	249.1	4.8	10	250.3	4.3	10	250.4	4.9
11	249.0	4.7	11	251.6	4.5	11	249.3	4.3	11	250.0	4.9	11	249.5	4.7	11	249.4	4.8	11	248.4	4.5	11	249.4	5.2
12	249.3	4.2	12	249.1	4.1	12	249.9	4.3	12	249.7	4.8	12	249.4	5.0	12	249.9	4.5	12	250.7	4.3	12	249.7	4.8
13	249.6	4.7	13	249.0	4.4	13	249.2	4.4	13	249.4	4.9	13	249.6	4.9	13	248.2	4.5	13	250.3	4.5	13	249.9	4.8
14	249.5	4.4	14	250.8	4.2	14	250.2	4.6	14	250.3	4.7	14	249.3	4.7	14	249.7	4.4	14	251.6	4.2	14	250.1	5.2
15 f	250.2	1.8	15 f	249.2	1.7	15 f	250.1	1.6	15 f	250.7	1.6	15 f	250.2	1.5	15 f	250.0	1.6	15 f	249.3	1.6	15 f	250.6	1.6
16	250.1	4.5	16	250.4	4.4	16	250.3	4.6	16	248.5	5.0	16	249.1	5.2	16	249.3	4.5	16	250.2	4.3	16	249.5	5.0
17	250.7	4.2	17	249.1	4.3	17	249.6	4.2	17	249.7	4.6	17	250.4	4.8	17	247.7	4.2	17	250.1	4.5	17	249.0	4.8
18	250.6	4.3	18	250.4	4.4	18	249.8	4.2	18	250.9	4.8	18	249.9	4.7	18	250.0	4.3	18	249.4	4.3	18	250.7	4.8
19	250.1	4.2	19	248.5	4.2	19	249.2	4.3	19	250.5	4.6	19	249.3	4.6	19	251.1	4.3	19	249.7	4.2	19	250.9	4.8
20	251.3	4.6	20	251.2	4.3	20	250.3	4.3	20	250.0	4.6	20	249.6	4.8	20	249.7	4.4	20	250.2	4.5	20	249.8	4.8
21	248.3	4.3	21	249.5	4.2	21	250.5	4.2	21	251.4	4.6	21	251.5	4.8	21	249.6	4.4	21	249.1	4.4	21	248.3	4.9
22	250.5	4.5	22	248.3	4.6	22	249.7	4.5	22	250.5	4.7	22	250.3	4.8	22	250.8	4.5	22	249.8	4.3	22	249.0	4.7
23	249.4	4.3	23	250.8	4.0	23	249.9	4.4	23	250.4	4.5	23	250.4	4.8	23	250.1	4.3	23	250.7	4.3	23	249.8	4.6
24	250.6	4.6	24	250.2	4.5	24	250.1	4.3	24	248.6	4.5	24	249.7	4.8	24	250.6	4.3	24	249.2	4.4	24	249.0	4.9
25	250.2	4.1	25	249.4	4.2	25	250.0	4.3	25	250.1	4.6	25	248.9	4.8	25	251.1	4.2	25	249.1	4.2	25	250.0	4.8
26	250.2	4.7	26	249.9	4.7	26	251.6	4.3	26	248.8	4.4	26	247.8	4.7	26	249.9	4.4	26	249.9	4.3	26	250.6	4.9
27	250.2	4.2	27	250.4	4.0	27	249.7	4.3	27	249.1	4.3	27	250.2	4.8	27	250.3	4.4	27	247.8	4.3	27	250.0	4.9
28 f	250.6	1.8	28 f	250.7	1.6	28 f	249.9	1.8	28 f	250.8	1.7	28 f	250.2	1.5	28 f	250.0	1.6	28 f	249.8	1.7	28 f	249.7	1.7
29	249.4	4.6	29	250.1	4.3	29	248.9	4.5	29	250.5	4.7	29	250.1	4.7	29	251.3	4.2	29	250.3	4.4	29	249.2	4.7
30	249.2	4.3	30	247.8	4.4	30	250.0	4.2	30	250.0	4.5	30	249.4	4.8	30	250.8	4.3	30	250.6	4.3	30	249.8	4.9
31	248.7	4.3	31	249.5	4.2	31	250.9	4.2	31	250.6	4.6	31	248.5	4.5	31	249.6	4.3	31	249.3	4.7	31	248.6	4.9
32	248.6	4.2	32	250.9	4.2	32	249.9	4.1	32	251.1	4.4	32	249.3	4.6	32	250.0	4.5	32	248.8	4.2	32	251.3	4.7
33	249.5	4.6	33	249.7	4.2	33	251.5	4.4	33	248.6	4.5	33	248.7	4.7	33	249.3	4.4	33	249.1	4.2	33	248.8	4.8
34	247.5	4.4	34	249.8	4.1	34	250.3	4.0	34	249.6	4.5	34	248.4	4.8	34	248.9	4.4	34	250.3	4.1	34	249.3	5.0
35	250.4	4.4	35	249.0	4.0	35	251.3	4.5	35	249.5	4.7	35	249.8	4.7	35	249.6	4.4	35	251.8	4.2	35	250.1	4.7
36	249.6	4.3	36	249.4	4.2	36	249.2	4.3	36	249.4	4.5	36	249.1	4.8	36	250.2	4.5	36	250.3	4.6	36	250.7	4.8
37	248.8	4.7	37	251.8	4.3	37	251.7	4.3	37	251.9	4.5	37	249.1	4.7	37	249.2	4.5	37	249.7	4.3	37	249.8	4.6
38	250.6	4.4	38	249.9	4.0	38	248.6	4.2	38	250.0	4.5	38	248.4	4.8	38	248.9	4.3	38	249.5	4.2	38	249.0	5.1
39	249.7	4.7	39	250.2	4.4	39	249.7	4.3	39	249.3	5.0	39	248.6	5.0	39	250.2	4.7	39	249.7	4.8	39	249.4	5.0
40	250.1	4.3	40	250.3	4.2	40	249.2	4.0	40	248.9	4.6	40	250.3	4.7	40	250.2	4.5	40	249.1	4.3	40	251.8	5.1
41	249.5	4.2	41	249.4	3.8	41	248.6	3.9	41	249.7	4.1	41	250.2	4.2	41	252.2	4.3	41	249.6	4.0	41	249.4	4.3
42	249.6	4.3	42	249.6	3.9	42	248.4	4.0	42	249.0	4.2	42	248.5	4.2	42	250.1	4.5	42	249.3	4.2	42	250.1	4.6
43	250.4	4.0	43	248.5	3.9	43	250.1	3.9	43	249.3	4.2	43	249.1	4.3	43	250.2	4.1	43	249.7	4.2	43	249.6	4.5
44	248.7	4.1	44	249.2	4.0	44	251.0	3.9	44	250.2	4.2	44	248.8	4.4	44	250.0	4.1	44	249.9	4.1	44	248.1	4.7
45	250.2	3.8	45	250.6	3.9	45	249.0	3.8	45	249.6	4.0	45	249.5	4.2	45	249.5	3.9	45	249.4	4.0	45	249.8	4.5
46	250.3	4.5	46	249.1	3.7	46	249.3	4.0	46	250.4	4.2	46	251.0	4.3	46	249.2	4.1	46	248.0	4.2	46	248.6	4.5
47	249.2	4.2	47	248.8	4.0	47	249.7	4.0	47	249.8	4.0	47	249.7	4.2	47	248.8	4.0	47	247.5	3.9	47	249.9	4.6
48	250.3	4.2	48	249.8	3.8	48	250.7	4.2	48	247.9	4.1	48	249.4	4.4	48	250.7	4.0	48	248.9	4.2	48	250.1	4.6
49	249.4	4.0	49	249.4	3.9	49	249.9	4.3	49	249.5	3.9	49	248.1	4.2	49	250.1	4.0	49	250.4	4.0	49	249.9	4.4
50	249.2	4.2	50	249.7	3.9	50	251.2	4.0	50	250.6	4.3	50	250.9	4.3	50	249.5	4.3	50	249.7	4.1	50	250.8	4.5
51	251.0	4.1	51	248.3	3.9	51	249.8	4.1	51	249.3	4.0	51	249.0	4.1	51	250.7	4.0	51	248.5	3.8	51	251.3	4.5
52	250.4	4.3	52	249.8	3.9	52	249.2	3.9	52	249.7	4.3	52	249.3	4.3	52	248.8	4.3	52	251.0	4.3	52	247.8	4.7
53 f	249.8	1.4	53 f	249.9	1.4	53 f	249.8	1.4	53 f	250.6	1.4	53 f	250.0	1.5	53 f	250.0	1.4	53 f	250.1	1.4	53 f	250.1	1.4
54	250.5	4.2	54	250.5	3.8	54	249.9	3.8	54	248.0	4.3	54	249.6	4.1	54	250.5	4.1	54	248.6	4.0	54	249.6	4.6
55	248.6	4.5	55	249.1	3.9	55	249.8	4.1	55	250.8	4.2	55	248.7	4.4	55	249.8	4.4	55	249.0	4.2	55	249.3	4.5
56	250.2	4.2	56	249.4	3.9	56	250.8	3.8	56	250.3	4.0	56	249.5	4.3	56	249.6	3.9	56	249.6	4.1	56	249.8	4.4
57	249.5	4.3	57	251.1	3.9	57	250.2	4.0	57	249.3	4.1	57	249.8	4.4	57	250.3	4.0	57	249.6	4.2	57	250.7	4.7
58	250.6	4.3	58	249.6	4.1	58	250.0	4.2	58	249.8	4.0												