

## Fec test report:

Date: 2021-10-07 12:44:15

Tester name: Boris

### Test#1 Monitoring values

Failed

0	FEC label	031	OK
1	FEC DC2438 ID	340000024dd73726	OK
2	FEC_T (to 35°C)	23.438	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.196	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV FAILED	FAIL
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3011	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3004	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3068	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3020	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3057	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3022	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3046	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3090	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 23.438 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.598 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 340000024dd73726

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	506.9	5.5	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	381.4	0.6	2 r	388.3	0.7	2 r	370.0	0.7	2 r	349.6	0.7	2 r	404.8	0.7	2 r	345.0	0.6	2 r	389.7	0.7	2 r	312.3	0.7
3	330.0	5.3	3	418.7	4.9	3	283.9	5.1	3	291.2	5.5	3	388.2	5.9	3	282.1	5.1	3	265.3	5.0	3	262.7	5.6
4	380.2	4.6	4	357.4	4.4	4	199.5	4.4	4	302.6	4.8	4	346.3	5.4	4	303.4	4.7	4	247.3	4.8	4	179.6	5.3
5	348.0	4.8	5	341.7	4.7	5	293.4	4.8	5	345.7	5.3	5	386.4	5.6	5	271.9	4.9	5	279.1	4.9	5	224.3	5.3
6	268.5	4.3	6	365.9	4.5	6	309.1	4.4	6	370.8	5.0	6	420.0	5.5	6	282.9	5.1	6	278.6	4.7	6	182.8	4.8
7	338.2	4.9	7	425.3	4.7	7	286.3	4.7	7	383.9	5.2	7	350.6	5.3	7	272.4	5.1	7	260.0	4.5	7	217.9	5.2
8	325.2	4.4	8	364.3	4.3	8	248.3	4.5	8	263.7	4.6	8	385.1	5.3	8	238.8	4.8	8	361.2	4.5	8	183.0	5.2
9	350.0	4.8	9	368.2	4.5	9	306.0	4.7	9	250.2	5.0	9	397.5	5.6	9	278.7	4.7	9	299.6	4.6	9	195.2	5.0
10	253.2	4.4	10	391.3	4.3	10	281.4	4.2	10	326.6	4.8	10	404.5	5.1	10	320.4	4.7	10	263.5	4.7	10	210.2	5.1
11	322.4	5.1	11	345.6	4.6	11	295.3	4.5	11	319.8	4.8	11	402.6	5.5	11	331.2	4.7	11	282.2	4.5	11	262.7	5.3
12	293.1	4.3	12	383.9	4.2	12	305.5	4.1	12	370.1	4.9	12	444.1	5.2	12	335.5	4.6	12	307.7	4.4	12	206.1	5.0
13	365.9	4.8	13	342.1	4.3	13	217.4	4.3	13	338.6	4.8	13	354.1	5.2	13	217.0	4.9	13	238.3	4.4	13	218.6	5.0
14	310.5	4.4	14	348.2	4.2	14	173.0	4.3	14	346.0	4.6	14	348.1	5.2	14	258.9	4.6	14	332.1	4.5	14	147.2	5.1
15 f	288.7	1.7	15 f	380.3	1.6	15 f	334.3	1.7	15 f	326.4	1.5	15 f	316.2	1.6	15 f	297.1	1.5	15 f	268.7	1.5	15 f	293.6	1.6
16	384.5	4.7	16	399.0	4.2	16	178.2	4.6	16	302.6	4.9	16	421.5	4.9	16	317.9	4.7	16	276.0	4.4	16	167.0	5.0
17	376.5	4.3	17	379.2	4.3	17	223.4	4.4	17	333.6	4.5	17	349.3	5.1	17	290.7	4.5	17	332.2	4.8	17	280.1	5.2
18	343.4	4.8	18	341.1	4.4	18	195.9	4.7	18	330.3	4.7	18	388.4	5.1	18	262.1	4.5	18	318.9	4.7	18	137.2	5.0
19	380.1	4.4	19	370.8	4.0	19	321.2	4.3	19	284.1	4.5	19	392.7	5.1	19	286.6	4.7	19	291.2	4.4	19	265.4	5.1
20	247.1	4.5	20	357.0	4.6	20	259.7	4.6	20	242.5	4.7	20	349.5	5.2	20	342.1	4.6	20	310.0	4.5	20	250.1	4.9
21	401.1	4.2	21	333.9	4.0	21	232.4	4.1	21	334.4	4.6	21	331.2	5.1	21	259.1	4.4	21	308.9	4.5	21	269.5	5.3
22	408.2	4.6	22	314.5	4.2	22	272.2	4.5	22	317.4	4.7	22	357.7	5.0	22	230.1	4.5	22	272.1	4.4	22	176.5	4.9
23	363.7	4.3	23	333.8	4.2	23	261.0	4.1	23	308.8	4.5	23	371.8	5.0	23	260.8	4.5	23	313.7	4.4	23	260.6	5.1
24	305.7	4.8	24	378.7	4.5	24	251.2	4.2	24	308.5	4.6	24	269.7	5.1	24	286.5	4.4	24	288.3	4.5	24	282.7	4.8
25	440.4	4.5	25	333.3	4.3	25	282.6	4.1	25	218.1	4.8	25	417.6	5.0	25	225.3	4.3	25	262.1	4.4	25	281.1	4.9
26	281.4	4.3	26	327.8	4.2	26	330.5	4.2	26	288.9	4.9	26	345.2	5.0	26	329.3	4.4	26	246.8	4.3	26	176.1	4.8
27	296.6	4.2	27	366.5	3.9	27	191.8	4.3	27	338.7	4.4	27	312.9	5.1	27	226.5	4.5	27	326.1	4.4	27	224.3	5.1
28 f	317.6	1.8	28 f	343.6	1.7	28 f	223.9	1.8	28 f	342.8	1.8	28 f	413.3	1.6	28 f	228.1	1.5	28 f	243.1	1.7	28 f	209.9	1.6
29	329.2	4.5	29	390.7	4.4	29	272.7	4.5	29	315.2	4.8	29	332.9	4.8	29	252.1	4.4	29	275.9	4.3	29	208.0	5.2
30	384.2	4.1	30	361.3	4.1	30	291.9	4.3	30	315.7	4.5	30	398.5	5.0	30	287.2	4.6	30	316.8	4.5	30	161.2	4.9
31	416.7	4.8	31	369.1	4.2	31	224.2	4.6	31	328.2	4.5	31	366.4	4.8	31	219.7	4.4	31	264.5	4.6	31	220.7	4.9
32	397.7	4.3	32	307.7	4.2	32	211.6	4.1	32	316.0	4.5	32	315.5	5.2	32	242.2	4.7	32	319.4	4.8	32	202.5	5.2
33	377.6	4.4	33	439.7	4.5	33	227.7	4.1	33	307.4	4.6	33	321.3	4.9	33	264.1	4.4	33	308.8	4.5	33	223.3	4.8
34	362.9	4.2	34	376.6	4.2	34	287.7	4.0	34	261.9	4.5	34	314.4	5.2	34	367.1	4.7	34	270.6	4.5	34	179.8	4.9
35	370.9	4.4	35	312.1	4.4	35	267.0	4.4	35	361.9	4.9	35	446.2	4.8	35	247.5	4.6	35	276.5	4.6	35	200.9	4.8
36	319.4	4.3	36	404.4	4.0	36	210.9	4.1	36	288.7	4.4	36	316.1	5.2	36	232.3	4.7	36	321.1	4.5	36	233.9	5.1
37	340.0	4.5	37	387.8	4.5	37	263.0	4.4	37	312.1	4.6	37	349.6	4.8	37	200.3	4.5	37	303.1	4.4	37	253.8	4.9
38	299.0	4.3	38	423.0	4.1	38	225.9	4.0	38	282.3	4.5	38	319.2	5.1	38	258.2	4.5	38	310.8	4.5	38	193.8	5.2
39	367.4	4.6	39	318.1	4.7	39	304.7	4.5	39	283.5	4.9	39	393.0	5.4	39	269.9	5.0	39	338.2	4.9	39	166.7	5.3
40	325.1	4.3	40	406.8	4.0	40	224.3	3.9	40	265.9	4.4	40	350.7	5.0	40	346.1	4.5	40	290.4	4.6	40	350.8	5.3
41	358.3	4.0	41	364.9	4.1	41	283.1	3.9	41	291.4	4.1	41	392.2	4.4	41	274.9	4.1	41	335.9	4.0	41	316.7	4.6
42	361.7	4.2	42	367.0	4.0	42	260.3	4.0	42	258.5	4.2	42	298.2	4.5	42	312.2	4.3	42	321.9	4.2	42	200.9	4.9
43	370.7	4.1	43	331.9	3.9	43	220.4	4.0	43	363.0	4.3	43	245.3	4.4	43	323.7	4.1	43	272.9	4.2	43	260.7	4.8
44	402.4	4.3	44	302.2	4.1	44	251.9	4.5	44	307.8	4.3	44	369.1	4.5	44	251.7	4.1	44	278.0	4.6	44	233.5	5.0
45	323.5	4.2	45	389.9	3.7	45	324.8	3.9	45	285.6	4.1	45	396.6	4.5	45	261.5	4.1	45	356.8	4.2	45	222.2	4.7
46	352.0	4.4	46	374.1	4.0	46	339.8	3.9	46	347.9	4.5	46	399.9	4.6	46	228.8	3.2	46	331.0	4.2	46	240.2	4.7
47	333.2	4.2	47	380.7	4.2	47	240.3	4.0	47	292.0	4.0	47	376.8	4.7	47	315.6	4.3	47	259.9	4.2	47	262.1	4.9
48	389.2	4.2	48	363.6	3.9	48	285.9	4.3	48	324.3	4.4	48	381.4	4.6	48	305.1	4.6	48	249.9	4.2	48	238.6	5.0
49	330.7	4.2	49	423.9	4.1	49	192.4	4.0	49	281.3	4.2	49	374.2	4.4	49	272.2	4.2	49	301.8	4.2	49	225.5	4.7
50	338.5	4.3	50	289.1	4.2	50	247.3	4.0	50	265.9	4.4	50	369.1	4.7	50	225.3	4.3	50	321.1	4.4	50	169.9	4.9
51	361.9	4.0	51	396.5	4.0	51	220.8	4.0	51	281.2	4.1	51	316.0	4.3	51	335.1	4.1	51	308.3	4.2	51	283.2	4.9
52	308.9	4.5	52	387.5	4.3	52	201.2	4.1	52	334.1	4.4	52	332.6	4.8	52	273.1	4.4	52	263.9	4.2	52	155.3	4.8
53 f	341.9	1.6	53 f	437.0	1.8	53 f	234.2	1.6	53 f	251.1	1.8	53 f	354.7	1.6	53 f	276.2	1.6	53 f	381.8	1.6	53 f	201.7	1.6
54	360.3	4.3	54	343.7	4.3	54	259.3	4.0	54	283.8	4.0	54	368.5	4.4	54	350.4	4.5	54	293.9	4.2	54	203.5	4.5
55	380.5	4.6	55	425.8	4.1	55	281.1	4.2	55	282.7	4.3	55	391.3	4.4	55	277.8	4.3	55	301.2	4.4	55	129.2	4.9
56	302.9	4.1	56	359.9	4.0	56	291.7	4.0	56	360.1	4.3	56	407.3	4.4	56	255.2	4.1	56	287.5	4.1	56	211.2	4.6
57	388.2	4.2	57	402.1	4.1	57	310.5	4.2	57	282.7	4.5	57	336.7	4.7	57	251.2	4.3	57	266.0	4.6	57	212.6	5.0
58	398.1	4.2	58	372.5	4.2	58	200.5	4.0	58	287.4	4.0	58	341.4	4.4									



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	413.3	8.5	1 r	427.1	11.6	1 r	382.8	9.4	1 r	257.3	12.4	1 r	461.9	11.4	1 r	430.4	8.1	1 r	376.2	8.6	1 r	384.9	7.3
2 r	250.5	0.7	2 r	250.3	0.7	2 r	250.2	0.7	2 r	249.7	0.7	2 r	249.8	0.7	2 r	250.2	0.7	2 r	249.7	0.7	2 r	250.5	0.7
3	250.2	4.8	3	250.3	5.0	3	251.2	5.0	3	250.6	5.1	3	251.1	5.2	3	251.0	4.7	3	249.8	4.9	3	249.6	5.3
4	250.3	4.2	4	250.5	4.4	4	250.0	4.2	4	250.6	4.7	4	250.5	5.0	4	249.6	4.7	4	249.7	4.7	4	249.8	4.9
5	250.2	4.7	5	249.9	4.6	5	250.3	4.7	5	250.4	5.0	5	251.2	5.1	5	250.0	4.6	5	250.1	4.4	5	251.9	5.0
6	251.0	4.4	6	248.9	4.2	6	249.4	4.6	6	250.7	4.5	6	248.7	5.0	6	249.9	4.7	6	249.7	4.5	6	250.7	5.1
7	250.9	4.5	7	249.9	4.5	7	250.7	5.0	7	250.2	4.8	7	250.6	4.8	7	248.9	4.6	7	249.4	4.5	7	249.3	5.2
8	250.9	4.3	8	251.6	4.1	8	252.3	4.3	8	249.6	4.9	8	249.7	5.0	8	250.2	4.5	8	249.9	4.4	8	250.8	4.8
9	250.5	4.7	9	251.4	4.6	9	250.7	4.4	9	251.0	5.0	9	250.3	5.0	9	249.5	4.4	9	249.8	4.5	9	250.6	4.9
10	250.2	4.5	10	249.6	4.2	10	249.6	4.1	10	251.5	4.6	10	249.6	5.0	10	250.8	4.7	10	249.1	4.5	10	250.6	4.8
11	251.0	4.7	11	249.8	4.3	11	250.8	4.5	11	249.2	4.9	11	250.5	4.8	11	250.2	4.8	11	250.3	4.4	11	249.2	4.9
12	251.0	4.1	12	249.8	4.1	12	251.5	4.4	12	250.3	4.5	12	250.7	4.8	12	250.5	4.5	12	250.2	4.3	12	250.5	5.1
13	249.7	4.6	13	250.2	4.4	13	250.7	4.4	13	249.2	4.8	13	250.5	4.9	13	249.7	4.7	13	251.1	4.5	13	250.0	4.8
14	250.5	4.4	14	249.8	4.3	14	250.6	4.1	14	249.2	4.6	14	250.2	4.8	14	250.3	4.5	14	250.9	4.1	14	251.1	4.9
15 f	249.5	1.7	15 f	250.6	1.6	15 f	250.4	1.6	15 f	250.7	1.6	15 f	250.4	1.6	15 f	250.9	1.5	15 f	249.9	1.5	15 f	249.9	1.5
16	250.8	4.4	16	250.1	4.3	16	249.7	4.6	16	249.0	4.7	16	250.0	4.8	16	249.9	4.4	16	250.5	4.5	16	250.2	4.8
17	249.4	4.2	17	252.2	4.3	17	250.5	4.4	17	250.6	4.4	17	250.6	4.5	17	250.3	4.5	17	250.1	4.5	17	248.8	4.8
18	249.4	4.4	18	249.4	4.7	18	251.6	4.4	18	251.3	4.7	18	251.2	4.7	18	249.8	4.4	18	249.7	4.1	18	251.3	4.8
19	250.7	4.3	19	250.4	4.5	19	251.0	4.3	19	250.8	4.2	19	249.8	4.8	19	250.4	4.4	19	250.7	4.2	19	250.9	4.8
20	250.9	4.3	20	249.0	4.6	20	249.8	4.2	20	251.2	4.7	20	249.1	4.5	20	250.4	4.3	20	250.1	4.4	20	249.1	4.7
21	248.6	4.0	21	249.7	4.1	21	250.3	4.0	21	250.4	4.4	21	249.9	4.8	21	250.2	4.5	21	249.7	4.3	21	250.0	4.8
22	249.6	4.5	22	249.2	4.2	22	250.0	4.5	22	251.5	4.5	22	250.4	4.7	22	250.4	4.4	22	249.7	4.4	22	250.6	4.6
23	250.0	4.1	23	249.3	4.2	23	251.3	4.1	23	250.2	4.5	23	250.0	4.6	23	250.2	4.3	23	249.3	4.2	23	251.3	4.7
24	250.8	4.5	24	249.8	4.3	24	250.5	4.3	24	251.0	4.4	24	249.9	4.7	24	250.1	4.3	24	251.9	4.3	24	251.4	4.7
25	250.8	4.5	25	249.6	4.2	25	249.6	4.7	25	250.9	4.5	25	251.3	4.6	25	251.1	4.4	25	249.9	4.3	25	251.5	5.0
26	250.0	4.7	26	250.6	4.2	26	250.6	4.2	26	251.1	4.8	26	250.8	4.5	26	250.4	4.5	26	251.4	4.1	26	251.7	4.7
27	249.7	4.2	27	250.4	4.2	27	250.1	4.1	27	251.1	4.3	27	250.2	5.0	27	249.7	4.2	27	249.7	4.3	27	250.9	5.1
28 f	249.6	1.6	28 f	250.2	1.8	28 f	250.4	1.8	28 f	250.5	1.7	28 f	250.6	1.6	28 f	250.7	1.6	28 f	250.4	1.6	28 f	250.4	1.6
29	251.0	4.3	29	249.5	4.3	29	250.7	4.2	29	250.0	4.6	29	250.4	4.8	29	250.6	4.3	29	249.7	4.2	29	250.7	4.9
30	251.0	4.3	30	249.9	4.1	30	248.7	4.1	30	249.4	4.5	30	248.6	4.5	30	251.2	4.3	30	250.9	4.3	30	250.3	4.8
31	249.8	4.6	31	250.4	4.0	31	250.7	4.2	31	251.0	4.5	31	251.1	4.3	31	249.3	4.4	31	249.4	4.5	31	249.9	4.9
32	250.3	4.1	32	250.3	4.0	32	249.8	4.2	32	249.7	4.5	32	249.5	4.8	32	251.0	4.4	32	250.8	4.4	32	251.4	4.8
33	249.5	4.5	33	249.2	4.1	33	250.2	4.3	33	250.4	4.8	33	252.2	4.7	33	250.8	4.4	33	250.4	4.3	33	250.1	4.8
34	249.9	4.1	34	250.5	4.2	34	250.4	4.3	34	249.5	4.4	34	250.6	5.1	34	250.8	4.3	34	249.5	4.3	34	250.3	4.5
35	249.6	4.3	35	249.8	4.4	35	250.7	4.3	35	250.4	4.8	35	249.4	4.6	35	250.6	4.5	35	251.1	4.4	35	248.7	5.0
36	251.2	4.5	36	250.8	4.1	36	250.2	4.1	36	249.7	4.6	36	250.3	4.5	36	251.3	4.5	36	252.3	4.5	36	250.8	5.1
37	251.2	4.2	37	249.4	4.2	37	250.7	4.5	37	251.0	4.6	37	249.5	4.6	37	250.7	4.6	37	250.8	4.2	37	250.4	4.6
38	250.4	4.2	38	249.5	4.1	38	250.7	4.1	38	251.2	4.4	38	250.7	4.9	38	250.5	4.4	38	249.5	4.2	38	250.8	5.0
39	250.3	4.4	39	251.4	4.5	39	250.8	4.3	39	251.1	4.8	39	250.4	4.8	39	251.0	5.0	39	250.4	4.7	39	250.9	5.3
40	250.6	4.4	40	250.5	4.0	40	251.1	4.0	40	250.4	4.4	40	249.4	4.9	40	248.9	4.6	40	250.4	4.4	40	251.1	5.0
41	248.5	4.0	41	249.9	3.6	41	249.8	3.8	41	252.0	4.1	41	250.7	4.3	41	249.1	4.1	41	249.0	4.0	41	250.8	4.8
42	249.8	4.3	42	249.3	4.1	42	250.4	4.4	42	249.6	4.2	42	250.4	4.5	42	251.2	4.3	42	250.9	4.2	42	251.3	4.7
43	249.1	4.2	43	250.0	3.9	43	251.4	4.0	43	249.9	4.2	43	251.8	4.2	43	249.5	4.0	43	249.0	4.1	43	250.3	4.5
44	250.4	4.5	44	248.8	4.0	44	249.7	4.0	44	249.8	4.1	44	250.8	4.3	44	250.4	4.3	44	248.8	4.3	44	251.2	4.8
45	249.1	4.0	45	250.2	4.0	45	249.9	4.1	45	250.7	4.2	45	248.6	4.2	45	250.2	4.3	45	250.0	4.1	45	250.6	4.6
46	250.5	4.4	46	250.0	3.9	46	249.7	4.0	46	249.2	4.2	46	248.7	4.4	46	250.5	2.7	46	250.8	4.2	46	250.8	4.5
47	249.8	4.1	47	249.3	3.8	47	251.3	4.0	47	251.1	4.2	47	249.2	4.5	47	250.3	4.1	47	249.9	4.1	47	251.1	4.7
48	250.5	4.4	48	249.7	4.0	48	249.1	4.1	48	251.4	4.2	48	252.3	4.8	48	250.0	4.4	48	249.7	4.2	48	249.1	4.7
49	250.2	4.3	49	250.7	3.9	49	251.1	4.2	49	251.2	4.1	49	252.0	4.3	49	251.6	4.4	49	249.2	4.1	49	248.8	4.4
50	250.6	4.4	50	250.2	4.3	50	250.5	4.3	50	250.7	4.3	50	249.9	4.3	50	249.4	4.2	50	250.2	4.1	50	249.8	4.6
51	250.0	4.2	51	251.7	3.8	51	250.1	4.1	51	251.3	4.1	51	249.0	4.2	51	250.0	4.2	51	249.9	4.1	51	250.4	4.6
52	248.9	4.2	52	251.1	4.2	52	250.7	4.0	52	249.7	4.2	52	250.6	4.4	52	251.9	4.4	52	250.0	4.5	52	252.0	4.6
53 f	250.3	1.6	53 f	250.1	1.5	53 f	250.7	1.7	53 f	250.7	1.5	53 f	249.6	1.6	53 f	250.6	1.7	53 f	250.0	1.5	53 f	250.0	1.8
54	250.4	4.2	54	249.8	4.3	54	249.5	3.9	54	251.6	3.9	54	250.2	4.5	54	249.1	4.0	54	251.0	4.1	54	249.3	4.4
55	251.5	4.3	55	249.9	4.1	55	250.5	4.0	55	249.4	4.4	55	250.8	4.5	55	249.9	4.4	55	250.5	4.2	55	250.6	4.8
56	249.9	4.3	56	249.3	4.0	56	250.2	3.9	56	249.6	4.3	56	250.2	4.3	56	251.1	4.2	56	251.3	4.1	56	251.5	4.8
57	249.9	4.4	57	250.5	4.1	57	251.4	4.3	57	249.9	4.4	57	250.0	4.4	57	250.4	4.4	57	250.3	4.3	57	251.2	4.9
58	251.0	4.4	58	250.7	3.8	58	249.5	3.9	58	251.5	4.0												