

Fec test report:

Date: 2021-10-07 15:49:45

Tester name: Boris

Test#1 Monitoring values

Passed

0	FEC label	030	OK
1	FEC DC2438 ID	a90000024dc44626	OK
2	FEC_T (to 35°C)	24.344	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.396	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3011	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2947	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3062	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3015	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3028	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3092	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2975	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 24.344 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.698 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: a90000024dc44626

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xffffd	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xffffb	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff0000
136	fe 0 after 3 test_mode 0x1	0	0 TdcM(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 TdcM(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	351.6	0.7	2 r	370.1	0.7	2 r	322.3	0.7	2 r	343.8	0.7	2 r	356.8	0.7	2 r	278.8	0.7	2 r	349.4	0.7	2 r	350.0	0.7
3	264.7	5.2	3	319.4	4.8	3	248.5	5.0	3	293.1	5.1	3	239.3	5.7	3	263.4	5.3	3	314.3	4.9	3	311.4	5.3
4	293.9	4.5	4	201.8	4.3	4	244.8	4.6	4	258.4	4.6	4	200.1	5.2	4	274.6	4.8	4	259.0	4.8	4	237.2	4.7
5	246.8	5.0	5	235.6	4.8	5	254.6	4.6	5	304.4	5.0	5	235.3	5.7	5	251.5	5.1	5	311.5	5.1	5	310.7	5.2
6	229.9	4.2	6	213.3	4.2	6	278.5	4.4	6	323.3	4.6	6	213.3	5.1	6	302.8	4.8	6	310.8	5.0	6	245.4	5.0
7	333.8	4.8	7	212.7	4.3	7	286.7	4.7	7	260.4	4.9	7	237.9	5.3	7	259.4	5.0	7	285.9	4.9	7	244.1	4.9
8	276.8	4.7	8	294.2	4.1	8	239.1	4.5	8	262.4	4.8	8	226.5	5.4	8	215.9	4.9	8	297.6	4.7	8	230.9	4.8
9	303.7	4.8	9	334.6	4.6	9	195.3	4.7	9	251.6	4.8	9	275.3	5.3	9	165.8	5.1	9	281.5	4.7	9	283.2	4.8
10	262.0	4.3	10	219.0	4.3	10	248.6	4.2	10	265.0	4.4	10	253.0	5.3	10	171.3	5.4	10	262.6	4.8	10	254.7	4.9
11	287.0	4.8	11	260.8	4.6	11	300.8	4.6	11	207.1	4.5	11	154.5	5.0	11	193.7	5.0	11	377.5	4.4	11	301.1	5.0
12	286.0	4.2	12	277.7	4.2	12	295.9	4.4	12	219.7	4.5	12	208.5	5.0	12	193.4	4.8	12	259.2	4.6	12	275.1	4.8
13	222.4	4.7	13	267.2	4.3	13	293.6	4.4	13	299.1	4.6	13	167.2	5.2	13	244.4	4.9	13	317.4	5.0	13	238.9	4.8
14	254.1	4.4	14	292.9	4.1	14	286.7	4.2	14	166.8	4.5	14	141.7	4.7	14	202.7	4.9	14	338.7	4.6	14	303.8	4.9
15 f	250.5	1.5	15 f	347.4	1.7	15 f	320.4	1.6	15 f	259.7	1.6	15 f	240.7	1.5	15 f	203.5	1.6	15 f	361.3	1.6	15 f	296.4	1.6
16	309.3	4.7	16	362.9	4.2	16	306.2	4.6	16	268.9	4.5	16	214.4	5.1	16	189.2	4.8	16	278.3	4.5	16	171.9	4.6
17	262.3	4.4	17	220.8	4.3	17	279.0	4.2	17	295.4	4.5	17	192.7	4.9	17	178.0	4.7	17	283.9	4.6	17	301.1	4.9
18	234.3	4.5	18	219.9	4.4	18	246.2	4.5	18	259.5	4.6	18	230.6	5.0	18	212.0	4.7	18	265.4	4.8	18	271.8	4.7
19	295.4	4.5	19	262.3	4.2	19	314.2	4.4	19	298.0	4.3	19	213.4	5.0	19	172.4	4.9	19	249.6	4.5	19	319.0	4.7
20	313.8	4.5	20	336.3	4.2	20	205.1	4.4	20	293.1	4.7	20	187.3	5.1	20	226.7	5.1	20	405.4	4.6	20	332.1	4.7
21	343.6	4.5	21	347.0	3.9	21	205.0	4.2	21	222.1	4.4	21	232.5	5.0	21	223.0	4.8	21	252.9	4.5	21	331.8	4.8
22	282.4	4.3	22	252.8	4.3	22	231.2	4.6	22	249.4	4.5	22	220.7	5.0	22	191.3	4.8	22	303.0	4.7	22	272.3	4.6
23	279.6	4.2	23	175.9	4.1	23	235.1	4.3	23	236.7	4.5	23	250.1	4.8	23	247.0	5.2	23	317.1	4.5	23	231.0	4.8
24	322.9	4.5	24	288.5	4.1	24	222.2	4.5	24	305.0	4.6	24	187.5	4.9	24	281.6	4.9	24	253.1	4.5	24	295.3	4.7
25	354.0	4.3	25	253.2	4.1	25	153.4	4.3	25	256.6	4.4	25	272.8	4.8	25	285.8	4.6	25	270.5	4.5	25	299.2	4.8
26	296.7	4.6	26	299.1	4.3	26	270.4	4.5	26	199.7	4.8	26	234.5	4.9	26	247.2	4.8	26	253.5	4.5	26	229.5	4.5
27	298.3	4.4	27	309.1	4.1	27	243.1	4.2	27	211.3	4.3	27	216.9	5.0	27	232.7	4.9	27	269.7	4.6	27	265.8	5.0
28 f	317.9	1.6	28 f	236.3	1.7	28 f	280.9	1.7	28 f	240.4	1.7	28 f	229.7	1.7	28 f	234.9	1.8	28 f	256.9	1.7	28 f	275.8	1.8
29	254.6	4.4	29	366.0	4.7	29	274.4	4.2	29	310.5	4.7	29	275.8	4.8	29	239.5	4.7	29	316.6	4.7	29	260.4	4.5
30	314.8	4.3	30	306.6	4.1	30	294.6	4.3	30	225.5	4.3	30	263.4	5.3	30	204.2	4.8	30	360.5	4.6	30	243.0	5.1
31	325.3	4.6	31	249.1	4.1	31	209.9	4.2	31	371.7	4.5	31	199.7	4.9	31	201.2	4.9	31	373.6	4.5	31	278.0	4.7
32	282.9	4.2	32	280.8	4.0	32	304.9	4.0	32	309.0	4.3	32	256.0	5.0	32	264.5	4.7	32	225.9	4.5	32	219.3	4.9
33	321.1	4.6	33	282.6	4.2	33	259.8	4.4	33	225.8	4.6	33	234.2	4.8	33	235.1	5.0	33	294.1	4.7	33	274.6	4.8
34	286.3	4.2	34	241.2	4.0	34	206.1	4.0	34	275.1	4.2	34	291.9	4.8	34	263.3	5.0	34	295.1	4.5	34	281.6	4.8
35	350.5	4.6	35	271.9	4.3	35	241.9	4.5	35	306.1	4.6	35	200.8	5.1	35	281.8	4.8	35	255.5	4.7	35	227.2	4.8
36	287.1	4.3	36	234.3	4.0	36	187.0	4.2	36	164.8	4.2	36	228.3	4.9	36	165.4	4.9	36	349.7	4.8	36	272.3	5.1
37	331.1	4.4	37	257.0	4.3	37	276.5	4.2	37	295.0	4.7	37	254.1	4.9	37	221.4	4.7	37	363.4	4.6	37	291.6	4.8
38	320.1	4.2	38	215.1	4.1	38	201.1	4.0	38	291.1	4.4	38	277.5	5.0	38	232.1	5.1	38	413.3	4.8	38	283.1	4.7
39	315.7	4.5	39	239.8	4.3	39	282.0	4.3	39	285.5	4.8	39	253.6	5.2	39	280.9	5.0	39	265.6	4.8	39	330.8	5.2
40	239.0	4.2	40	280.5	4.0	40	185.0	4.2	40	288.0	4.1	40	320.6	4.8	40	316.4	4.8	40	284.1	4.5	40	283.0	4.9
41	338.6	4.5	41	292.2	3.8	41	261.4	4.0	41	309.9	4.0	41	289.0	4.3	41	226.8	4.4	41	388.6	4.3	41	287.2	4.4
42	256.3	4.5	42	210.5	3.9	42	265.6	4.2	42	337.0	4.1	42	285.4	4.6	42	271.3	4.6	42	318.4	4.2	42	350.8	4.7
43	348.5	4.0	43	298.9	4.0	43	208.6	3.8	43	271.9	4.2	43	184.5	4.1	43	325.6	4.3	43	314.2	4.2	43	312.2	4.7
44	288.2	4.3	44	280.8	3.9	44	210.9	4.0	44	204.1	4.3	44	258.6	4.5	44	167.6	4.6	44	199.2	4.5	44	184.9	4.6
45	209.3	4.1	45	323.7	3.6	45	197.1	4.0	45	214.5	3.7	45	222.1	4.6	45	250.1	4.4	45	389.1	4.3	45	309.1	4.2
46	317.4	4.4	46	288.4	3.9	46	244.8	4.0	46	249.6	3.9	46	313.5	4.4	46	234.9	4.6	46	251.3	4.2	46	207.8	4.7
47	313.3	4.1	47	333.4	3.6	47	329.8	3.9	47	285.9	3.9	47	315.8	4.4	47	227.8	4.6	47	327.6	4.4	47	218.7	4.6
48	287.6	4.6	48	330.6	3.9	48	242.3	4.6	48	285.4	4.0	48	223.5	4.4	48	241.9	4.6	48	235.2	4.6	48	208.2	4.6
49	337.6	4.2	49	274.9	3.8	49	236.4	4.1	49	245.5	4.1	49	195.3	4.4	49	316.4	4.4	49	306.0	4.2	49	234.7	4.4
50	279.5	4.5	50	291.2	4.2	50	315.6	4.2	50	310.5	4.2	50	206.8	4.4	50	207.0	4.6	50	301.9	4.4	50	401.9	4.8
51	321.1	4.2	51	218.7	3.7	51	328.3	4.0	51	271.5	4.2	51	217.1	4.2	51	279.5	4.4	51	282.5	4.3	51	208.8	4.7
52	274.0	4.6	52	284.0	4.1	52	301.4	4.4	52	226.2	4.1	52	210.9	4.4	52	347.6	4.6	52	309.6	4.5	52	323.6	4.6
53 f	363.8	1.8	53 f	268.1	1.4	53 f	286.7	1.6	53 f	277.4	1.5	53 f	294.8	1.5	53 f	212.7	1.5	53 f	315.7	1.5	53 f	305.4	1.4
54	286.8	4.1	54	207.6	4.2	54	207.6	4.2	54	280.4	4.0	54	267.3	4.4	54	176.8	4.6	54	195.3	4.1	54	196.1	4.4
55	280.9	4.5	55	280.5	3.9	55	283.1	4.0	55	262.9	4.0	55	239.1	4.6	55	215.2	4.5	55	241.7	4.6	55	314.2	4.7
56	309.9	4.1	56	320.6	3.6	56	186.0	4.0	56	250.7	3.9	56	294.2	4.3	56	251.5	4.4	56	256.4	4.2	56	232.2	4.4
57	242.2	4.6	57	294.6	4.2	57	337.8	4.2	57	339.1	4.4	57	198.6	4.6	57	239.8	4.6	57	319.9	4.6	57	299.4	4.7
58	297.0	4.6	58	297.3	3.6	58	194.5	3.8	58	258.4	4.0	58	250.2	4.3									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	283.9	11.9	1 r	445.3	7.8	1 r	406.1	8.7	1 r	395.8	8.5	1 r	437.6	6.5	1 r	374.9	9.6	1 r	433.8	9.0	1 r	376.0	10.6
2 r	249.7	0.7	2 r	250.1	0.7	2 r	250.3	0.7	2 r	249.8	0.7	2 r	249.7	0.7	2 r	250.2	0.7	2 r	250.4	0.7	2 r	250.1	0.7
3	249.7	4.7	3	251.1	5.0	3	250.3	4.8	3	249.8	5.2	3	249.9	5.4	3	250.7	5.2	3	250.9	5.1	3	251.7	5.2
4	250.8	4.3	4	250.7	4.1	4	249.1	4.7	4	249.6	4.6	4	250.1	5.0	4	250.8	5.0	4	250.8	4.8	4	249.8	4.8
5	249.8	5.0	5	250.5	4.5	5	250.8	4.7	5	249.1	4.9	5	250.2	5.3	5	250.8	5.2	5	249.4	4.8	5	249.5	4.9
6	250.1	4.4	6	249.9	4.5	6	249.0	4.5	6	250.4	4.5	6	250.1	5.1	6	249.2	5.0	6	249.6	4.5	6	250.3	4.7
7	250.0	4.6	7	250.4	4.5	7	249.2	4.5	7	250.5	4.8	7	251.6	5.5	7	251.5	4.9	7	249.3	4.5	7	249.9	4.7
8	250.2	4.5	8	250.2	4.2	8	249.9	4.4	8	250.6	4.4	8	250.6	5.1	8	249.8	5.0	8	249.2	4.6	8	250.9	4.8
9	250.2	4.6	9	248.7	4.5	9	251.3	4.5	9	249.5	4.7	9	251.1	5.4	9	249.4	4.8	9	249.4	4.9	9	250.5	5.0
10	249.8	4.3	10	251.9	4.2	10	249.9	4.3	10	249.3	4.4	10	251.0	5.2	10	251.2	4.7	10	250.6	4.4	10	249.5	4.9
11	250.4	4.5	11	249.7	4.3	11	250.4	4.6	11	250.4	4.6	11	251.0	5.0	11	250.0	4.8	11	250.3	4.6	11	251.8	4.7
12	249.8	4.3	12	249.6	4.3	12	249.7	4.4	12	249.8	4.5	12	251.0	5.0	12	251.8	4.7	12	251.2	4.7	12	250.3	4.8
13	249.2	4.7	13	251.7	4.3	13	248.9	4.4	13	249.6	4.5	13	250.2	5.1	13	250.1	4.8	13	251.8	4.7	13	251.1	4.6
14	249.4	4.5	14	250.4	4.4	14	249.3	4.3	14	249.4	4.3	14	250.0	5.1	14	249.4	5.1	14	250.0	4.4	14	251.5	4.8
15 f	250.4	1.5	15 f	250.8	1.6	15 f	250.4	1.6	15 f	249.6	1.6	15 f	249.0	1.6	15 f	250.0	1.7	15 f	250.0	1.7	15 f	250.7	1.6
16	250.4	4.7	16	250.5	4.3	16	250.7	4.5	16	250.6	4.6	16	249.2	5.0	16	251.7	4.7	16	249.8	4.5	16	249.4	4.8
17	251.3	4.1	17	250.1	4.2	17	250.2	4.5	17	251.2	4.3	17	251.3	5.0	17	250.9	4.8	17	249.6	4.4	17	249.3	4.8
18	250.8	4.5	18	250.8	4.1	18	250.6	4.5	18	249.8	4.3	18	250.5	4.9	18	250.4	4.6	18	250.8	4.6	18	249.6	4.7
19	250.1	4.1	19	251.6	4.2	19	250.1	4.2	19	250.8	4.3	19	250.3	4.8	19	250.9	4.9	19	248.9	4.5	19	251.0	4.6
20	250.6	4.4	20	250.7	4.1	20	250.2	4.3	20	251.9	4.4	20	250.7	4.8	20	250.2	4.8	20	251.1	4.7	20	249.3	4.8
21	251.4	4.3	21	250.5	4.1	21	249.3	4.2	21	250.3	4.2	21	249.2	5.0	21	249.0	4.6	21	249.8	4.4	21	250.3	4.7
22	250.8	4.5	22	249.2	4.2	22	248.8	4.2	22	249.4	4.5	22	249.7	4.8	22	249.0	4.7	22	250.5	4.6	22	251.4	4.8
23	249.3	4.2	23	250.0	3.9	23	249.2	4.2	23	248.4	4.4	23	250.3	4.8	23	250.5	4.7	23	251.4	4.7	23	251.3	4.8
24	250.3	4.4	24	250.0	4.3	24	249.8	4.5	24	249.2	4.3	24	251.5	4.7	24	249.3	4.6	24	249.5	4.3	24	250.7	4.9
25	251.3	4.4	25	250.2	4.2	25	253.0	4.5	25	249.6	4.5	25	249.0	5.3	25	249.7	4.8	25	250.8	4.3	25	250.7	4.8
26	249.8	4.6	26	249.8	4.1	26	249.0	4.3	26	249.7	4.3	26	249.7	4.8	26	249.2	4.7	26	248.8	4.6	26	249.1	4.6
27	250.3	4.2	27	251.6	3.9	27	250.8	4.5	27	249.2	4.4	27	250.2	5.1	27	250.4	4.8	27	248.4	4.5	27	250.0	4.9
28 f	250.6	1.6	28 f	250.3	1.7	28 f	249.8	1.6	28 f	250.6	1.7	28 f	249.4	1.6	28 f	250.2	1.8	28 f	250.5	1.7	28 f	249.6	1.8
29	250.1	4.5	29	249.4	4.1	29	250.5	4.4	29	251.4	4.5	29	249.9	4.9	29	252.1	5.1	29	249.7	4.2	29	251.1	4.7
30	250.1	4.2	30	248.8	4.0	30	248.9	4.1	30	250.8	4.2	30	251.5	5.0	30	251.5	4.9	30	249.0	4.4	30	250.8	4.8
31	251.3	4.4	31	249.3	4.2	31	250.4	4.4	31	247.9	4.4	31	250.7	4.8	31	250.2	4.9	31	251.2	4.5	31	249.4	4.7
32	250.7	4.1	32	250.0	3.9	32	249.1	4.0	32	248.9	4.2	32	248.8	5.0	32	250.3	4.6	32	250.3	4.8	32	250.0	5.1
33	249.9	4.4	33	250.0	4.3	33	249.3	4.3	33	249.8	4.1	33	249.2	4.7	33	251.8	4.7	33	250.4	4.6	33	248.2	4.5
34	250.3	4.2	34	251.2	4.1	34	250.1	4.0	34	250.4	4.2	34	249.8	4.8	34	250.4	4.8	34	250.5	4.7	34	248.7	4.9
35	250.9	4.4	35	248.8	4.2	35	249.0	4.7	35	251.3	4.5	35	249.9	4.7	35	250.8	4.6	35	249.5	4.6	35	250.8	4.4
36	250.3	4.2	36	249.2	3.9	36	249.6	4.1	36	249.8	4.3	36	250.5	4.9	36	250.8	5.2	36	251.7	4.5	36	251.4	4.9
37	250.3	4.4	37	248.9	4.2	37	249.7	4.3	37	249.4	4.6	37	250.7	4.5	37	252.3	4.6	37	249.9	4.5	37	248.6	4.5
38	251.1	4.2	38	251.8	4.0	38	250.6	4.2	38	249.4	4.1	38	250.8	4.8	38	251.4	4.7	38	249.8	4.5	38	249.6	5.0
39	250.2	4.7	39	248.7	4.3	39	251.1	4.5	39	249.5	4.4	39	249.9	5.2	39	250.6	5.1	39	249.5	4.7	39	250.5	5.2
40	250.2	4.1	40	250.5	4.0	40	250.2	4.1	40	250.5	4.2	40	250.0	5.1	40	251.3	4.7	40	250.7	4.5	40	250.4	4.8
41	249.7	4.3	41	249.9	3.9	41	250.2	4.0	41	249.9	3.9	41	250.7	4.3	41	249.4	4.6	41	250.8	4.2	41	250.8	4.5
42	249.8	4.3	42	249.4	3.9	42	250.4	4.0	42	251.6	4.2	42	251.1	4.5	42	251.1	4.5	42	250.3	4.2	42	250.7	4.4
43	251.3	4.1	43	250.2	3.6	43	251.1	4.0	43	250.3	3.7	43	248.7	4.4	43	249.9	4.3	43	250.2	4.2	43	249.5	4.3
44	249.8	4.3	44	248.4	3.9	44	250.1	4.1	44	249.7	4.0	44	249.0	4.4	44	249.0	4.3	44	251.3	4.2	44	249.2	4.5
45	252.2	4.1	45	249.8	3.8	45	249.0	4.1	45	250.1	3.8	45	249.7	4.1	45	249.3	4.3	45	249.2	4.3	45	249.0	4.7
46	251.9	4.3	46	249.6	3.9	46	250.3	4.1	46	249.1	4.0	46	251.3	4.7	46	249.5	4.6	46	250.0	4.4	46	250.6	4.5
47	250.6	4.0	47	251.0	3.6	47	248.9	3.9	47	249.4	4.0	47	249.0	4.3	47	250.9	4.3	47	249.6	4.2	47	251.4	4.5
48	249.1	4.3	48	250.2	4.0	48	249.7	4.2	48	249.4	4.1	48	249.3	4.4	48	251.4	4.4	48	251.2	4.2	48	251.0	4.7
49	249.4	4.2	49	249.2	3.7	49	250.8	4.0	49	249.8	3.9	49	251.0	4.4	49	249.6	4.5	49	250.6	4.1	49	248.5	4.5
50	248.5	4.2	50	250.3	3.9	50	250.4	4.2	50	250.6	4.0	50	248.6	4.5	50	250.3	4.5	50	249.8	4.3	50	250.8	4.9
51	249.8	4.0	51	249.9	4.2	51	250.3	3.9	51	251.1	3.8	51	250.7	4.2	51	251.5	4.8	51	250.2	4.0	51	251.0	4.6
52	249.7	4.4	52	249.3	3.9	52	251.8	4.0	52	251.9	4.3	52	249.6	4.3	52	250.9	4.6	52	248.5	4.2	52	249.7	4.7
53 f	249.9	1.5	53 f	249.9	1.3	53 f	250.3	1.5	53 f	250.3	1.4	53 f	249.0	1.4	53 f	250.2	1.6	53 f	249.6	1.6	53 f	250.4	1.4
54	249.2	4.2	54	249.7	4.0	54	249.6	3.8	54	251.9	3.7	54	250.3	4.2	54	251.0	4.6	54	249.6	4.1	54	250.7	4.5
55	250.6	4.5	55	250.8	3.8	55	250.2	4.0	55	250.6	4.1	55	249.6	4.3	55	251.8	4.4	55	249.8	4.2	55	250.0	4.5
56	249.3	4.1	56	249.9	3.7	56	250.3	3.9	56	249.7	4.1	56	250.8	4.3	56	251.9	4.5	56	250.8	4.1	56	250.5	4.6
57	250.5	4.4	57	250.4	4.1	57	250.9	4.5	57	248.5	4.2	57	248.8	4.8	57	249.3	4.6	57	250.4	4.3	57	250.5	4.6
58	249.9	4.1	58	250.2	3.6	58	248.4	4.0	58	250.7	3.8												