

Fec test report:

Date: 2021-09-29 08:57:32

Tester name: lc

Test#1 Monitoring values

Passed

0	FEC label	030	OK
1	FEC DC2438 ID	a90000024dc44626	OK
2	FEC_T (to 35°C)	23.188	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.402	OK
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean FAILED	STDDEV FAILED	FAIL
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Failed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3021	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2951	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3071	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3030	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 1459	FAIL
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3023	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3100	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2972	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 23.188 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.701 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: a90000024dc44626

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdc(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdc(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdc(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdc(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	511.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	350.7	0.7	2 r	371.1	0.7	2 r	321.2	0.7	2 r	343.8	0.7	2 r	511.0	0.0	2 r	277.6	0.7	2 r	349.5	0.7	2 r	349.5	0.7
3	262.3	5.1	3	320.3	4.8	3	246.4	4.9	3	293.3	4.9	3	511.0	0.0	3	262.2	5.2	3	314.2	5.0	3	310.4	4.8
4	293.3	4.4	4	203.5	4.1	4	243.3	4.4	4	256.3	4.6	4	511.0	0.0	4	273.7	4.8	4	258.8	4.5	4	236.2	4.9
5	244.1	4.9	5	237.5	4.3	5	253.7	4.8	5	304.7	4.7	5	511.0	0.0	5	250.6	5.0	5	311.7	4.7	5	309.9	4.7
6	229.3	4.4	6	213.9	4.3	6	275.0	4.4	6	322.8	4.4	6	511.0	0.0	6	300.5	4.9	6	310.6	5.0	6	245.2	4.7
7	333.5	4.8	7	213.8	4.5	7	284.4	4.5	7	259.8	4.6	7	511.0	0.0	7	258.8	4.8	7	286.6	4.6	7	244.6	4.7
8	275.0	4.3	8	293.9	4.1	8	237.8	4.4	8	261.3	4.7	8	511.0	0.0	8	213.8	4.8	8	296.6	4.8	8	230.9	4.6
9	303.2	4.7	9	334.3	4.7	9	195.4	4.8	9	251.9	4.7	9	511.0	0.0	9	162.9	4.8	9	281.3	4.7	9	282.5	5.0
10	259.7	4.1	10	221.1	4.2	10	246.9	4.3	10	263.2	4.3	10	511.0	0.0	10	169.8	5.0	10	262.4	5.2	10	253.8	4.7
11	285.2	4.7	11	260.9	4.5	11	300.0	4.7	11	207.7	4.6	11	511.0	0.0	11	191.7	4.7	11	377.4	4.4	11	301.0	4.7
12	285.6	4.6	12	277.6	4.1	12	295.7	4.5	12	218.4	4.3	12	511.0	0.0	12	192.6	4.8	12	259.2	4.7	12	273.4	4.6
13	220.2	4.6	13	268.5	4.2	13	292.2	4.5	13	298.1	4.5	13	511.0	0.0	13	243.0	4.8	13	317.1	4.6	13	238.0	4.8
14	250.9	4.4	14	294.1	4.1	14	284.6	4.5	14	166.3	4.3	14	511.0	0.0	14	200.5	4.8	14	339.6	4.7	14	303.4	4.7
15 f	249.8	1.5	15 f	348.4	1.5	15 f	319.5	1.6	15 f	259.4	1.5	15 f	511.0	0.0	15 f	201.7	1.7	15 f	361.2	1.7	15 f	295.9	1.6
16	308.3	4.5	16	364.9	4.2	16	305.8	4.5	16	270.1	4.5	16	511.0	0.0	16	185.9	4.6	16	277.8	4.6	16	170.9	4.5
17	262.3	4.3	17	221.8	4.3	17	278.0	4.6	17	295.7	4.2	17	511.0	0.0	17	176.0	4.6	17	283.7	4.5	17	300.9	4.6
18	233.0	4.7	18	220.7	4.2	18	246.1	4.3	18	258.9	4.4	18	511.0	0.0	18	210.3	4.8	18	265.4	4.5	18	270.7	4.6
19	293.2	4.2	19	264.2	4.1	19	313.1	4.2	19	297.5	4.3	19	511.0	0.0	19	170.2	5.0	19	249.5	4.7	19	318.9	4.7
20	311.5	4.6	20	336.2	4.0	20	202.7	4.4	20	294.1	4.4	20	511.0	0.0	20	224.2	4.7	20	406.1	4.5	20	330.5	4.4
21	343.1	4.4	21	347.4	4.0	21	202.7	4.1	21	223.0	4.0	21	511.0	0.0	21	222.0	4.7	21	252.7	4.5	21	330.1	4.8
22	281.9	4.5	22	252.7	4.4	22	228.6	4.5	22	248.6	4.4	22	511.0	0.0	22	188.9	4.6	22	303.9	4.5	22	272.6	4.7
23	278.2	4.4	23	177.3	4.0	23	232.9	4.6	23	235.5	4.3	23	511.0	0.0	23	245.3	4.7	23	317.5	4.3	23	229.8	4.4
24	322.2	4.5	24	289.9	4.3	24	218.8	4.2	24	303.8	4.4	24	511.0	0.0	24	278.4	4.7	24	252.6	4.3	24	294.4	4.6
25	352.8	4.2	25	253.6	4.1	25	152.5	4.3	25	257.0	4.1	25	511.0	0.0	25	284.8	4.7	25	270.6	4.3	25	297.8	4.9
26	295.2	4.5	26	299.3	4.3	26	268.3	4.4	26	200.0	4.5	26	511.0	0.0	26	244.7	4.6	26	252.7	4.4	26	229.2	4.2
27	297.6	4.0	27	311.7	4.1	27	241.8	4.1	27	210.7	4.2	27	511.0	0.0	27	230.6	4.9	27	269.9	4.7	27	264.0	4.7
28 f	317.7	1.6	28 f	237.0	1.7	28 f	278.8	1.6	28 f	240.5	1.6	28 f	511.0	0.0	28 f	233.4	1.7	28 f	257.6	1.8	28 f	274.5	1.9
29	253.4	4.5	29	267.1	4.2	29	273.2	4.5	29	310.8	4.2	29	511.0	0.0	29	237.3	4.8	29	315.8	4.4	29	258.9	4.5
30	314.5	4.2	30	306.9	4.1	30	293.4	4.3	30	225.9	4.4	30	511.0	0.0	30	202.8	4.8	30	360.3	4.3	30	243.7	4.7
31	323.2	4.4	31	248.5	4.3	31	208.6	4.5	31	371.3	4.4	31	511.0	0.0	31	196.8	4.8	31	374.6	4.5	31	275.9	4.5
32	281.9	4.3	32	281.3	4.0	32	301.9	4.1	32	308.9	4.1	32	511.0	0.0	32	262.3	4.6	32	225.9	4.5	32	218.7	4.7
33	320.3	4.5	33	283.4	4.2	33	258.6	4.3	33	224.6	4.3	33	511.0	0.0	33	233.7	4.6	33	295.6	4.4	33	271.7	4.6
34	284.6	4.1	34	240.7	4.0	34	206.2	4.2	34	274.4	4.2	34	511.0	0.0	34	261.8	4.8	34	295.0	4.3	34	280.7	4.6
35	349.0	4.4	35	272.1	4.4	35	240.0	4.3	35	306.5	4.2	35	511.0	0.0	35	281.3	4.8	35	254.7	4.5	35	227.2	4.3
36	285.6	4.2	36	235.2	3.8	36	185.0	4.0	36	163.3	4.2	36	511.0	0.0	36	163.4	4.8	36	350.2	4.6	36	272.2	4.9
37	330.3	4.4	37	256.3	4.2	37	275.9	4.3	37	292.4	4.2	37	511.0	0.0	37	219.3	4.8	37	362.6	4.6	37	290.0	4.5
38	318.5	4.2	38	216.1	3.9	38	199.7	4.0	38	289.6	4.2	38	511.0	0.0	38	231.5	4.9	38	413.3	4.6	38	281.9	4.6
39	314.7	4.4	39	240.4	4.2	39	280.9	4.4	39	286.3	4.6	39	511.0	0.0	39	278.8	5.1	39	266.7	5.2	39	329.6	5.0
40	238.9	4.3	40	280.1	4.0	40	183.0	4.3	40	288.8	4.2	40	511.0	0.0	40	315.2	4.8	40	284.4	4.5	40	283.7	4.7
41	338.9	4.5	41	291.8	3.5	41	259.8	4.0	41	309.0	3.9	41	511.0	0.0	41	224.6	4.4	41	388.6	4.4	41	287.1	4.0
42	254.9	4.3	42	210.8	4.1	42	264.3	3.9	42	338.1	4.0	42	511.0	0.0	42	269.2	4.7	42	318.3	4.2	42	350.7	4.3
43	347.4	4.0	43	300.6	3.8	43	207.8	3.9	43	271.5	3.7	43	511.0	0.0	43	323.9	4.2	43	313.8	4.2	43	311.4	4.3
44	287.6	4.3	44	281.0	3.8	44	210.5	4.2	44	204.0	4.0	44	511.0	0.0	44	165.9	4.2	44	198.0	4.2	44	183.8	4.2
45	208.8	4.0	45	324.8	3.6	45	195.1	3.9	45	213.5	3.9	45	511.0	0.0	45	248.2	4.3	45	388.9	4.2	45	307.5	4.3
46	318.9	4.5	46	288.7	3.9	46	242.4	4.4	46	249.1	3.8	46	511.0	0.0	46	232.5	4.4	46	251.2	4.1	46	206.5	4.3
47	311.2	4.2	47	334.9	3.8	47	327.0	3.9	47	285.5	3.8	47	511.0	0.0	47	227.0	4.6	47	327.8	4.2	47	218.1	4.2
48	286.3	4.2	48	332.2	3.8	48	240.3	3.9	48	285.2	3.9	48	511.0	0.0	48	241.0	4.2	48	235.5	3.9	48	207.0	4.3
49	336.0	4.2	49	274.9	3.7	49	235.4	3.8	49	244.7	3.8	49	511.0	0.0	49	313.9	4.2	49	305.4	3.9	49	233.4	4.5
50	278.1	4.3	50	291.7	3.8	50	314.7	4.3	50	310.3	4.0	50	511.0	0.0	50	205.0	4.5	50	301.7	4.2	50	402.1	4.4
51	320.8	4.1	51	219.4	3.7	51	327.5	3.9	51	272.1	3.9	51	511.0	0.0	51	279.1	4.5	51	282.5	4.2	51	207.9	4.2
52	273.3	4.6	52	285.2	4.0	52	300.3	4.1	52	226.9	4.0	52	511.0	0.0	52	346.0	4.5	52	309.0	4.0	52	322.8	4.2
53 f	363.1	1.6	53 f	269.2	1.4	53 f	285.7	1.6	53 f	276.4	1.6	53 f	511.0	0.0	53 f	211.2	1.6	53 f	315.5	1.4	53 f	304.9	1.4
54	285.2	4.2	54	205.2	3.7	54	205.2	3.9	54	280.5	3.8	54	511.0	0.0	54	175.9	4.5	54	194.3	4.1	54	195.8	4.2
55	281.1	4.5	55	281.9	3.7	55	281.6	4.1	55	263.1	3.9	55	511.0	0.0	55	214.8	4.3	55	241.1	4.2	55	311.9	4.4
56	308.5	4.3	56	321.7	3.9	56	185.2	3.9	56	250.7	3.9	56	511.0	0.0	56	250.6	4.4	56	256.3	4.0	56	229.3	4.2
57	240.1	4.3	57	295.7	3.9	57	335.7	4.1	57	336.7	4.2	57	511.0	0.0	57	237.6	4.4	57	320.1	3.9	57	298.9	4.1
58	295.4	4.1	58	297.8																			

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	511.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	281.9	11.9	1 r	447.1	7.5	1 r	407.5	8.4	1 r	395.3	8.1	1 r	511.0	0.0	1 r	375.6	9.3	1 r	434.0	8.8	1 r	375.2	10.3
2 r	249.8	0.7	2 r	249.9	0.7	2 r	250.4	0.7	2 r	249.8	0.7	2 r	511.0	0.0	2 r	249.9	0.7	2 r	250.3	0.7	2 r	250.6	0.7
3	251.7	5.0	3	250.4	4.7	3	251.9	4.6	3	249.4	4.8	3	511.0	0.0	3	250.5	5.2	3	250.0	4.8	3	252.1	4.9
4	250.1	4.4	4	249.1	4.2	4	249.9	4.5	4	252.1	4.7	4	511.0	0.0	4	249.7	4.9	4	249.7	4.7	4	249.6	4.7
5	251.8	5.0	5	249.3	4.3	5	251.3	4.6	5	250.3	4.8	5	511.0	0.0	5	250.6	5.0	5	250.2	4.7	5	249.5	4.9
6	250.0	4.3	6	249.3	4.2	6	252.0	4.6	6	249.8	4.2	6	511.0	0.0	6	250.7	5.1	6	249.1	4.6	6	250.1	4.7
7	249.2	4.5	7	249.9	4.5	7	251.2	4.4	7	251.2	4.8	7	511.0	0.0	7	249.3	4.9	7	248.4	4.5	7	249.4	4.7
8	251.3	4.2	8	250.8	4.2	8	248.9	4.2	8	251.9	4.8	8	511.0	0.0	8	251.0	4.9	8	250.6	4.6	8	249.7	4.7
9	249.5	4.6	9	250.3	4.5	9	250.4	4.7	9	249.5	4.5	9	511.0	0.0	9	250.0	4.7	9	249.9	4.5	9	250.4	4.5
10	250.3	4.4	10	249.7	4.1	10	249.9	4.4	10	251.9	4.6	10	511.0	0.0	10	250.7	5.1	10	249.1	4.6	10	249.5	4.8
11	251.9	4.5	11	250.5	4.4	11	248.8	4.6	11	249.0	4.6	11	511.0	0.0	11	250.5	4.8	11	249.8	4.6	11	249.3	4.7
12	249.1	4.5	12	250.0	4.0	12	249.4	4.4	12	250.9	4.5	12	511.0	0.0	12	249.3	4.7	12	250.8	5.0	12	250.9	4.7
13	250.5	4.4	13	250.3	4.3	13	250.6	4.6	13	251.0	4.7	13	511.0	0.0	13	249.8	4.7	13	251.3	4.5	13	251.2	4.8
14	251.1	4.3	14	249.1	4.2	14	249.8	4.2	14	251.2	4.2	14	511.0	0.0	14	249.9	4.8	14	249.3	4.5	14	250.1	4.8
15 f	249.8	1.6	15 f	250.2	1.6	15 f	250.8	1.5	15 f	250.6	1.6	15 f	511.0	0.0	15 f	250.0	1.6	15 f	249.9	1.6	15 f	250.1	1.7
16	249.7	4.5	16	249.4	4.4	16	249.8	4.5	16	250.0	4.5	16	511.0	0.0	16	252.5	4.8	16	249.8	4.5	16	249.8	4.9
17	250.2	4.3	17	249.3	3.9	17	249.8	4.5	17	250.5	4.2	17	511.0	0.0	17	251.7	4.8	17	248.8	4.5	17	249.3	4.7
18	250.5	4.5	18	249.8	4.2	18	249.0	4.3	18	250.9	4.7	18	511.0	0.0	18	250.6	4.4	18	250.9	4.5	18	250.9	4.6
19	250.9	4.5	19	249.9	4.1	19	250.2	4.3	19	249.5	4.3	19	511.0	0.0	19	253.0	5.1	19	249.1	4.4	19	249.8	4.6
20	250.5	4.5	20	250.6	4.4	20	250.4	4.3	20	251.6	4.4	20	511.0	0.0	20	251.8	4.8	20	250.0	4.4	20	250.9	4.4
21	250.8	4.0	21	250.9	4.0	21	249.3	4.1	21	248.8	4.4	21	511.0	0.0	21	249.4	4.7	21	249.2	4.3	21	250.4	4.6
22	249.5	4.4	22	249.8	4.2	22	250.7	4.3	22	250.6	4.2	22	511.0	0.0	22	250.5	4.9	22	249.6	4.7	22	249.3	4.7
23	251.1	4.1	23	249.6	4.2	23	249.6	4.4	23	249.8	4.3	23	511.0	0.0	23	251.9	4.5	23	249.4	4.3	23	250.2	4.7
24	250.6	4.3	24	249.4	4.2	24	251.3	4.5	24	250.2	4.4	24	511.0	0.0	24	251.7	4.5	24	248.9	4.5	24	249.6	4.4
25	250.3	4.1	25	249.8	4.2	25	251.6	4.7	25	249.2	4.2	25	511.0	0.0	25	250.6	4.7	25	250.1	4.3	25	249.9	4.5
26	251.1	4.5	26	249.8	4.0	26	250.2	4.0	26	249.4	4.2	26	511.0	0.0	26	250.6	4.7	26	249.9	4.2	26	250.6	4.4
27	248.7	4.2	27	248.3	4.1	27	249.7	4.0	27	250.2	4.2	27	511.0	0.0	27	251.1	5.1	27	250.1	4.5	27	250.4	4.6
28 f	250.1	1.6	28 f	249.6	1.6	28 f	250.3	1.7	28 f	249.3	1.6	28 f	511.0	0.0	28 f	251.1	1.6	28 f	249.5	1.7	28 f	250.9	1.7
29	250.9	4.5	29	249.5	4.2	29	250.5	4.3	29	250.8	4.3	29	511.0	0.0	29	251.3	4.5	29	250.5	4.3	29	250.2	4.4
30	250.3	4.0	30	249.1	4.1	30	250.6	4.3	30	250.7	4.3	30	511.0	0.0	30	251.0	4.7	30	250.6	4.7	30	249.0	4.8
31	251.1	4.4	31	249.0	4.0	31	249.5	4.4	31	249.4	4.5	31	511.0	0.0	31	251.9	4.8	31	248.4	4.2	31	251.0	4.5
32	250.8	4.1	32	250.2	4.0	32	250.9	4.2	32	249.6	4.3	32	511.0	0.0	32	249.9	4.9	32	250.8	4.6	32	250.1	4.6
33	250.9	4.4	33	250.8	4.0	33	248.4	4.3	33	250.4	4.3	33	511.0	0.0	33	250.3	5.0	33	247.6	4.3	33	251.3	4.8
34	249.6	4.3	34	251.4	4.3	34	249.3	4.2	34	251.1	4.2	34	511.0	0.0	34	249.8	4.8	34	250.1	4.6	34	249.8	4.5
35	249.6	4.5	35	249.9	4.2	35	249.5	4.4	35	251.0	4.2	35	511.0	0.0	35	249.9	4.8	35	248.5	4.4	35	250.2	4.5
36	248.8	4.2	36	250.2	4.0	36	250.6	4.1	36	251.5	4.1	36	511.0	0.0	36	251.7	4.7	36	250.2	4.6	36	250.3	4.8
37	250.8	4.7	37	250.9	4.2	37	250.6	4.2	37	252.3	4.3	37	511.0	0.0	37	251.4	4.8	37	249.7	4.6	37	250.5	4.7
38	250.0	4.1	38	250.7	4.0	38	249.9	4.1	38	250.3	4.2	38	511.0	0.0	38	250.2	5.1	38	249.8	4.5	38	250.9	4.5
39	250.5	4.4	39	250.7	4.2	39	249.9	4.5	39	248.9	4.5	39	511.0	0.0	39	250.4	5.0	39	249.0	4.5	39	251.3	5.0
40	250.1	4.2	40	250.7	4.1	40	251.8	4.4	40	250.0	4.4	40	511.0	0.0	40	251.2	4.9	40	249.3	4.5	40	249.0	4.7
41	248.9	4.1	41	250.2	3.8	41	248.3	3.9	41	249.7	4.0	41	511.0	0.0	41	249.8	4.5	41	249.9	4.3	41	249.3	4.2
42	249.1	4.4	42	249.8	3.8	42	250.1	4.2	42	248.7	4.1	42	511.0	0.0	42	250.8	4.2	42	250.5	4.0	42	249.9	4.3
43	251.8	4.3	43	248.0	3.6	43	250.2	4.0	43	249.4	3.7	43	511.0	0.0	43	251.6	4.4	43	249.2	4.3	43	250.6	4.4
44	249.2	4.1	44	250.0	4.2	44	249.8	3.9	44	249.4	3.9	44	511.0	0.0	44	249.6	4.3	44	251.8	4.1	44	250.7	4.2
45	250.1	4.1	45	250.3	3.8	45	250.2	4.0	45	250.6	3.8	45	511.0	0.0	45	250.8	4.4	45	249.1	4.2	45	250.0	4.3
46	248.9	4.3	46	250.3	3.8	46	251.1	4.2	46	250.2	4.0	46	511.0	0.0	46	251.2	4.6	46	249.8	4.2	46	250.9	4.4
47	250.5	4.0	47	249.1	3.8	47	251.7	4.0	47	249.7	3.7	47	511.0	0.0	47	250.1	4.4	47	250.1	4.1	47	250.5	4.0
48	251.9	4.3	48	250.2	4.2	48	251.7	4.0	48	250.1	4.1	48	511.0	0.0	48	250.7	4.5	48	250.2	4.1	48	250.6	4.3
49	249.7	4.0	49	251.4	3.7	49	250.4	3.9	49	249.1	3.9	49	511.0	0.0	49	251.0	4.5	49	251.6	4.0	49	249.5	4.3
50	249.8	4.2	50	251.4	3.9	50	250.0	4.2	50	249.6	3.9	50	511.0	0.0	50	250.5	4.3	50	250.2	4.3	50	250.3	4.4
51	249.2	4.1	51	249.8	3.8	51	249.3	4.0	51	250.6	4.0	51	511.0	0.0	51	250.0	4.4	51	251.1	4.1	51	249.8	4.2
52	250.1	4.2	52	250.0	3.9	52	251.0	4.0	52	250.0	4.3	52	511.0	0.0	52	250.6	4.4	52	249.3	4.2	52	250.7	4.3
53 f	250.0	1.6	53 f	249.5	1.4	53 f	249.5	1.4	53 f	251.1	1.5	53 f	511.0	0.0	53 f	250.3	1.6	53 f	249.0	1.4	53 f	249.2	1.4
54	251.5	4.1	54	249.6	3.9	54	251.5	3.9	54	250.6	3.7	54	511.0	0.0	54	250.0	4.2	54	250.3	4.2	54	250.9	4.4
55	250.2	4.3	55	249.3	4.0	55	249.8	4.1	55	250.1	4.0	55	511.0	0.0	55	250.8	4.5	55	248.8	4.3	55	250.5	4.3
56	251.4	4.3	56	249.6	3.7	56	249.6	4.0	56	250.0	3.9	56	511.0	0.0	56	250.7	4.5	56	249.9	4.1	56	252.0	4.4
57	250.7	4.6	57	250.0	4.0	57	250.1	4.2	57	251.0	3.9	57	511.0	0.0	57	249.9	4.3	57	249.8	4.2	57	250.4	4.3
58	250.4	4.0	58	250.4	3.9	58	250.6	3.9	58	249.9	3.9												