

## Fec test report:

Date: 2021-09-28 14:16:46

Tester name: lc

### Test#1 Monitoring values

Failed

0	FEC label	022	OK
1	FEC DC2438 ID	1e0000024db56e26	OK
2	FEC_T (to 35°C)	24.312	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.2A to 1.6A)	1.704	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2984	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3112	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3080	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3070	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2993	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3094	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3101	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3060	OK

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 24.312 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.852 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 1e0000024db56e26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 ( Aligned SCA_Write )
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 TdcM(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 TdcM(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 TdcM(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 TdcM(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	474.7	11.3	1 r	511.0	0.0	1 r	511.0	0.0
2 r	364.1	0.7	2 r	314.3	0.7	2 r	344.3	0.7	2 r	329.9	0.7	2 r	323.0	0.7	2 r	278.4	0.7	2 r	304.1	0.7	2 r	342.5	0.7
3	268.5	5.3	3	297.4	5.0	3	269.6	4.9	3	255.4	5.7	3	221.7	5.7	3	146.1	5.2	3	257.7	5.3	3	294.5	5.2
4	247.1	4.6	4	245.3	4.3	4	291.4	4.2	4	235.4	5.0	4	267.2	5.7	4	217.9	5.1	4	261.3	4.9	4	290.2	4.9
5	233.8	5.2	5	268.2	4.9	5	234.3	4.8	5	187.0	5.3	5	120.8	5.6	5	169.1	5.2	5	246.9	5.1	5	321.7	4.9
6	237.2	4.5	6	236.0	4.4	6	234.0	4.2	6	284.9	4.9	6	240.6	5.2	6	237.5	5.0	6	146.5	5.0	6	236.0	5.0
7	202.7	5.0	7	374.1	4.8	7	272.3	4.7	7	290.8	5.0	7	211.2	5.2	7	81.3	5.2	7	204.9	4.7	7	361.4	5.0
8	300.3	4.4	8	265.5	4.2	8	226.8	4.3	8	244.0	5.0	8	203.5	5.7	8	230.8	4.9	8	274.8	4.8	8	345.8	5.0
9	222.4	4.9	9	283.4	4.6	9	250.4	4.7	9	276.2	5.1	9	305.5	5.5	9	148.6	5.0	9	273.8	5.0	9	322.0	4.9
10	296.4	4.5	10	139.3	4.4	10	221.1	4.5	10	257.9	5.0	10	194.0	5.5	10	186.5	5.2	10	231.7	4.8	10	236.3	5.1
11	243.9	4.7	11	227.6	4.6	11	243.4	4.4	11	250.5	5.0	11	217.3	5.3	11	165.1	5.1	11	299.1	4.9	11	297.9	5.2
12	279.3	4.4	12	297.3	4.2	12	367.3	4.6	12	237.9	4.8	12	301.0	5.3	12	259.9	5.2	12	230.1	4.9	12	265.4	5.0
13	256.1	4.8	13	308.9	4.4	13	300.7	4.5	13	176.4	5.2	13	219.1	5.0	13	150.3	4.7	13	235.9	5.0	13	283.6	4.8
14	231.0	4.4	14	245.2	4.3	14	231.2	4.6	14	257.3	5.0	14	241.2	5.3	14	306.5	4.9	14	247.6	4.6	14	278.9	4.8
15 f	244.7	1.6	15 f	260.0	1.6	15 f	226.2	1.6	15 f	290.9	1.6	15 f	273.1	1.7	15 f	91.1	1.7	15 f	294.5	1.6	15 f	287.8	1.6
16	164.9	4.6	16	295.3	4.5	16	309.9	4.5	16	250.1	4.8	16	291.4	4.8	16	229.0	4.7	16	193.4	4.7	16	354.6	4.8
17	203.4	4.3	17	221.4	4.2	17	205.5	4.3	17	216.3	4.8	17	169.2	5.4	17	75.5	4.8	17	244.9	5.0	17	262.8	4.8
18	287.5	4.5	18	336.8	4.7	18	303.5	4.7	18	269.6	4.7	18	228.5	5.2	18	230.6	4.7	18	215.5	4.7	18	354.5	4.7
19	263.1	4.3	19	248.9	4.3	19	245.4	4.1	19	284.2	4.7	19	243.9	5.3	19	236.4	4.6	19	191.6	4.7	19	292.2	5.0
20	187.0	4.6	20	245.3	4.5	20	241.8	4.8	20	257.6	4.9	20	152.4	5.2	20	228.0	4.7	20	279.2	4.6	20	372.7	4.7
21	259.6	4.3	21	236.9	4.2	21	256.2	4.0	21	251.6	4.9	21	221.2	5.0	21	184.5	4.9	21	218.6	4.9	21	326.2	5.1
22	266.5	4.7	22	273.7	4.2	22	353.4	4.5	22	270.3	5.1	22	252.2	5.0	22	190.1	4.8	22	208.3	4.7	22	354.5	5.2
23	227.9	4.3	23	269.2	4.4	23	223.4	4.3	23	255.5	4.9	23	282.0	5.2	23	260.7	4.8	23	273.0	4.7	23	378.0	5.0
24	239.8	4.6	24	246.5	4.5	24	238.2	4.2	24	236.0	4.7	24	354.8	5.1	24	184.8	4.8	24	212.2	4.6	24	223.8	4.7
25	263.9	4.2	25	285.2	4.5	25	203.3	4.3	25	232.3	4.7	25	303.3	5.3	25	243.4	4.8	25	276.8	4.5	25	275.1	5.1
26	301.3	4.7	26	284.0	4.6	26	343.7	4.4	26	276.1	4.7	26	321.0	4.9	26	159.9	5.1	26	290.5	4.8	26	226.5	4.5
27	200.8	4.3	27	216.8	4.5	27	257.4	4.0	27	196.4	4.7	27	208.4	5.1	27	155.8	4.8	27	238.7	4.7	27	307.0	4.8
28 f	270.1	1.8	28 f	281.9	1.8	28 f	274.4	1.7	28 f	262.1	1.8	28 f	238.3	1.8	28 f	179.3	1.8	28 f	214.9	1.8	28 f	314.1	1.7
29	283.5	4.4	29	213.2	4.2	29	241.5	4.7	29	200.8	4.9	29	188.9	4.8	29	340.7	4.6	29	385.7	4.7	29	300.5	4.9
30	225.9	4.6	30	295.7	4.2	30	260.9	4.3	30	320.7	4.8	30	224.4	5.1	30	178.3	5.1	30	254.4	4.7	30	318.1	5.0
31	203.4	4.4	31	327.7	4.5	31	276.6	4.4	31	184.4	5.2	31	207.9	5.1	31	191.6	4.8	31	278.9	4.6	31	233.8	4.8
32	291.1	4.5	32	361.8	4.3	32	204.1	4.3	32	276.4	4.6	32	189.2	4.9	32	189.0	4.9	32	293.3	5.0	32	339.4	5.1
33	152.8	4.7	33	284.8	4.3	33	283.0	4.4	33	250.2	4.7	33	221.3	5.0	33	188.7	4.7	33	294.7	4.8	33	262.4	4.6
34	200.7	4.4	34	256.0	4.2	34	256.2	4.1	34	244.6	4.5	34	218.2	5.1	34	153.8	5.0	34	286.8	4.8	34	362.0	4.9
35	250.0	4.5	35	264.8	4.5	35	212.7	4.4	35	270.1	4.6	35	301.3	5.5	35	246.9	4.8	35	251.5	4.9	35	271.1	5.0
36	259.7	4.2	36	153.4	4.2	36	331.2	4.0	36	223.4	4.8	36	285.9	5.1	36	215.4	5.0	36	278.3	4.7	36	268.6	4.9
37	295.4	4.6	37	282.4	4.5	37	253.2	4.3	37	213.2	4.5	37	339.2	5.1	37	186.4	4.8	37	269.8	4.6	37	281.4	4.6
38	274.8	4.3	38	248.9	4.5	38	336.0	4.5	38	219.6	4.5	38	319.7	5.3	38	169.7	4.9	38	249.3	4.9	38	299.2	5.0
39	323.4	4.8	39	231.0	4.5	39	288.0	4.4	39	225.3	5.2	39	193.7	5.5	39	179.1	5.3	39	252.4	4.8	39	235.5	5.1
40	289.1	4.1	40	264.9	4.2	40	266.7	4.2	40	257.6	4.7	40	309.7	5.3	40	221.8	5.0	40	235.5	4.8	40	291.8	5.1
41	346.1	4.2	41	353.3	3.9	41	310.4	3.9	41	222.3	4.2	41	188.7	4.6	41	214.6	4.3	41	232.9	4.5	41	248.0	4.7
42	283.9	4.5	42	263.3	4.2	42	259.3	3.8	42	298.4	4.2	42	299.1	4.6	42	170.9	4.5	42	203.8	4.5	42	306.4	4.5
43	295.6	4.0	43	228.0	4.2	43	207.8	3.9	43	248.8	3.9	43	249.5	4.5	43	254.4	4.5	43	187.2	4.4	43	280.4	4.6
44	348.7	4.5	44	274.1	4.2	44	262.5	4.1	44	230.8	4.3	44	225.2	4.6	44	158.7	4.2	44	223.0	4.4	44	242.1	4.8
45	242.3	4.2	45	308.4	4.0	45	286.4	3.9	45	194.8	4.1	45	245.0	4.5	45	202.7	4.4	45	254.4	4.3	45	253.9	4.7
46	255.8	4.3	46	214.7	4.1	46	245.3	4.0	46	258.2	4.5	46	189.8	4.6	46	218.4	4.2	46	217.3	4.3	46	233.9	4.6
47	310.9	3.9	47	211.0	3.8	47	287.8	3.9	47	241.1	4.1	47	332.7	4.5	47	208.7	4.1	47	277.2	4.5	47	264.8	4.6
48	240.6	4.5	48	212.7	4.2	48	288.4	4.1	48	232.9	4.7	48	213.0	4.5	48	204.3	4.4	48	161.9	4.4	48	353.0	4.8
49	252.2	4.1	49	247.2	3.9	49	245.1	3.9	49	244.4	4.0	49	196.6	4.6	49	264.2	4.4	49	275.9	4.3	49	246.2	4.5
50	275.7	4.5	50	297.2	4.2	50	207.4	4.1	50	237.1	4.5	50	277.2	4.5	50	204.7	4.4	50	198.3	4.4	50	293.7	4.4
51	281.1	4.1	51	268.2	3.9	51	286.0	4.0	51	325.1	4.1	51	269.8	4.4	51	126.1	4.2	51	291.8	4.2	51	290.7	4.6
52	260.2	4.3	52	183.7	4.2	52	296.1	4.4	52	262.6	4.2	52	208.4	4.5	52	217.2	4.5	52	224.1	4.1	52	353.4	4.8
53 f	310.4	1.5	53 f	256.3	1.6	53 f	226.9	1.5	53 f	262.6	1.4	53 f	365.8	1.6	53 f	136.7	1.6	53 f	235.1	1.4	53 f	295.3	1.5
54	248.1	4.4	54	251.1	3.9	54	278.9	3.8	54	234.4	4.2	54	220.4	4.1	54	152.3	4.4	54	193.3	4.2	54	261.5	4.8
55	253.6	4.5	55	290.4	4.2	55	240.2	4.1	55	230.2	4.3	55	250.0	4.6	55	170.1	4.4	55	302.4	4.5	55	309.5	4.7
56	292.3	4.3	56	200.9	3.8	56	260.6	3.9	56	288.2	4.2	56	266.2	4.2	56	241.1	4.4	56	273.1	4.2	56	276.1	4.6
57	318.5	4.5	57	218.4	4.2	57	215.9	3.9	57	265.3	4.5	57	292.8	4.5	57	241.0	4.5	57	238.3	4.6	57	336.0	4.6
58	215.2	4.2	58	235.1	3.9	58	323.6	4.0	58	236.9	4.3	58	244.3	4.3									



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	382.6	7.7	1 r	382.6	11.5	1 r	388.2	8.1	1 r	344.7	10.0	1 r	298.5	11.3	1 r	250.1	11.2	1 r	348.9	8.8	1 r	349.2	12.3
2 r	250.3	0.7	2 r	250.2	0.7	2 r	250.4	0.7	2 r	250.2	0.7	2 r	250.0	0.7	2 r	250.6	0.7	2 r	250.1	0.6	2 r	249.6	0.7
3	251.1	5.3	3	250.1	5.2	3	251.1	5.3	3	250.8	6.1	3	249.2	6.2	3	250.1	5.6	3	249.8	5.6	3	250.1	5.2
4	250.8	4.7	4	249.6	4.3	4	250.0	4.3	4	251.5	5.5	4	250.0	5.9	4	250.8	5.2	4	250.9	5.1	4	249.6	5.2
5	249.0	5.0	5	248.9	5.1	5	250.1	5.0	5	250.7	5.6	5	250.6	5.9	5	252.2	5.2	5	249.1	5.0	5	249.1	5.6
6	250.9	4.6	6	249.8	4.4	6	251.7	4.7	6	249.9	5.5	6	249.8	5.7	6	251.3	5.3	6	250.9	5.1	6	250.3	5.0
7	249.4	5.2	7	250.8	5.0	7	251.0	4.8	7	249.8	5.8	7	250.1	5.7	7	251.3	5.0	7	250.1	4.9	7	251.8	5.1
8	251.1	4.5	8	252.2	4.4	8	249.4	4.3	8	250.7	5.2	8	249.6	5.7	8	250.1	5.0	8	250.1	4.9	8	249.1	5.3
9	250.8	5.2	9	250.2	5.0	9	251.2	4.9	9	249.6	5.5	9	249.3	6.2	9	250.4	5.2	9	250.2	5.0	9	249.1	5.1
10	250.0	4.6	10	250.1	4.5	10	251.7	4.4	10	250.7	5.2	10	250.2	5.7	10	251.4	5.2	10	249.3	5.0	10	250.6	5.2
11	251.1	4.9	11	248.6	4.8	11	250.6	4.6	11	249.8	5.2	11	249.6	5.8	11	251.0	5.1	11	249.5	5.1	11	249.6	5.5
12	251.2	4.6	12	252.1	4.4	12	250.6	4.2	12	249.5	5.2	12	249.3	5.6	12	250.4	5.1	12	251.0	4.8	12	252.2	5.1
13	250.8	4.9	13	249.9	4.7	13	249.2	4.6	13	250.9	5.3	13	251.2	5.7	13	249.2	5.3	13	250.8	5.2	13	250.2	5.0
14	250.8	4.4	14	249.7	4.2	14	250.9	4.3	14	251.5	5.0	14	250.7	5.7	14	249.6	5.0	14	249.7	5.0	14	249.7	4.8
15 f	249.5	1.7	15 f	249.8	1.6	15 f	250.1	1.6	15 f	250.2	1.7	15 f	249.8	1.7	15 f	250.9	1.8	15 f	249.9	1.6	15 f	249.7	1.6
16	249.4	4.8	16	250.2	4.8	16	250.0	4.7	16	251.0	5.2	16	250.4	5.4	16	249.1	5.0	16	250.4	4.8	16	250.6	4.9
17	250.6	4.5	17	250.5	4.6	17	251.0	4.2	17	250.2	5.1	17	250.6	5.5	17	250.4	5.4	17	249.5	4.8	17	249.4	5.0
18	250.3	5.1	18	249.3	4.7	18	251.2	4.8	18	251.1	5.1	18	250.1	5.5	18	250.2	5.1	18	250.7	4.9	18	250.2	4.7
19	250.0	4.4	19	249.6	4.5	19	251.5	4.3	19	249.4	5.0	19	250.6	5.7	19	252.3	5.1	19	249.8	4.7	19	251.4	5.0
20	250.4	4.7	20	249.6	4.5	20	250.8	4.5	20	248.9	5.1	20	249.6	5.5	20	250.3	5.0	20	249.0	5.0	20	250.8	4.9
21	249.5	4.6	21	249.8	4.2	21	251.3	4.3	21	249.9	4.9	21	249.8	5.4	21	251.7	5.0	21	249.7	4.8	21	251.1	4.8
22	251.2	4.8	22	249.1	4.7	22	251.1	4.9	22	250.8	5.0	22	250.9	5.4	22	250.1	5.0	22	251.3	4.8	22	251.2	4.8
23	250.0	4.5	23	250.2	4.5	23	250.8	4.3	23	249.8	5.0	23	252.0	5.5	23	249.3	5.2	23	249.4	4.7	23	249.8	5.2
24	250.9	4.8	24	250.7	4.4	24	251.0	4.4	24	249.4	5.1	24	249.0	5.4	24	250.6	5.1	24	249.3	4.7	24	250.3	5.2
25	249.9	4.6	25	250.0	4.5	25	251.4	4.4	25	251.0	5.0	25	251.9	5.6	25	251.2	5.0	25	249.5	5.0	25	250.2	5.2
26	250.9	4.8	26	250.1	4.7	26	251.4	4.8	26	249.8	5.1	26	249.9	5.3	26	250.4	4.9	26	249.2	4.9	26	248.8	5.0
27	250.6	4.5	27	250.3	4.3	27	250.7	4.1	27	250.8	4.8	27	249.7	5.4	27	250.3	5.1	27	250.2	4.7	27	249.3	5.0
28 f	250.5	1.7	28 f	250.2	1.7	28 f	251.2	1.7	28 f	250.2	1.8	28 f	250.7	1.8	28 f	251.0	1.8	28 f	250.7	1.7	28 f	250.0	1.6
29	250.3	4.8	29	249.3	4.9	29	247.5	4.3	29	250.8	5.2	29	251.5	5.3	29	250.7	4.9	29	250.2	4.7	29	250.3	4.9
30	249.7	4.4	30	249.3	4.2	30	250.7	4.1	30	249.8	4.8	30	250.8	5.5	30	250.6	5.1	30	250.4	4.8	30	249.4	5.3
31	251.3	5.0	31	249.7	4.9	31	251.1	4.5	31	251.3	5.1	31	250.9	5.3	31	249.0	4.9	31	249.5	4.9	31	249.0	4.8
32	249.6	4.3	32	249.7	4.4	32	250.3	4.2	32	249.9	4.7	32	249.4	5.0	32	251.0	5.0	32	249.9	5.3	32	250.2	5.1
33	248.7	4.6	33	248.2	4.5	33	250.9	4.4	33	250.7	4.7	33	249.1	5.3	33	250.7	4.9	33	250.1	5.0	33	250.3	4.9
34	248.9	4.6	34	249.0	4.3	34	250.8	4.3	34	249.6	4.8	34	250.7	5.4	34	250.9	5.4	34	248.3	4.8	34	251.5	5.1
35	250.7	4.8	35	248.8	4.5	35	250.0	4.3	35	250.5	4.8	35	249.6	5.4	35	250.8	5.2	35	250.9	4.9	35	249.9	4.9
36	249.6	4.4	36	251.8	4.2	36	250.7	3.9	36	251.0	5.0	36	249.4	5.5	36	250.1	5.5	36	250.9	5.0	36	249.9	4.9
37	251.8	4.7	37	250.4	4.5	37	249.6	4.3	37	251.4	4.9	37	249.6	5.3	37	251.3	5.0	37	249.7	4.6	37	251.4	4.8
38	251.5	4.4	38	251.0	4.2	38	252.0	4.4	38	249.6	4.8	38	249.6	5.4	38	248.4	5.0	38	249.8	5.1	38	251.2	5.2
39	251.3	4.8	39	249.8	4.5	39	251.0	4.5	39	250.4	5.3	39	250.4	5.8	39	250.0	5.5	39	248.6	5.4	39	250.6	5.6
40	250.1	4.6	40	251.2	4.5	40	250.3	4.2	40	250.7	4.8	40	250.6	5.7	40	249.3	5.2	40	249.0	5.0	40	250.8	5.5
41	250.5	4.2	41	250.0	3.8	41	250.9	4.1	41	250.6	4.3	41	249.7	4.5	41	250.2	4.5	41	251.4	4.4	41	250.8	4.6
42	249.7	4.6	42	250.2	4.2	42	250.5	4.2	42	251.5	4.3	42	250.4	5.0	42	249.0	4.5	42	251.4	4.6	42	250.1	4.9
43	249.5	4.2	43	249.2	4.1	43	251.6	3.9	43	249.4	4.2	43	249.9	4.6	43	250.6	4.3	43	249.9	4.3	43	250.7	4.5
44	249.0	4.5	44	251.3	4.4	44	250.1	4.2	44	250.2	4.3	44	251.1	4.7	44	251.2	4.6	44	250.6	4.4	44	248.5	5.0
45	252.0	4.1	45	250.0	4.0	45	249.3	3.9	45	251.5	4.2	45	250.3	4.5	45	248.1	4.5	45	251.2	4.3	45	249.3	4.7
46	250.9	4.6	46	247.7	4.1	46	249.8	4.1	46	251.7	4.3	46	249.3	4.9	46	251.2	4.4	46	251.4	4.8	46	249.9	4.7
47	249.2	4.2	47	249.7	3.8	47	249.5	3.9	47	248.7	4.0	47	250.0	4.6	47	249.6	4.5	47	251.1	4.6	47	249.5	4.7
48	249.9	4.6	48	250.1	4.3	48	249.6	4.2	48	250.1	4.5	48	250.1	4.5	48	251.2	4.7	48	250.7	4.4	48	250.9	5.2
49	250.4	4.3	49	250.4	4.2	49	249.8	4.1	49	249.2	4.3	49	250.6	4.6	49	251.4	4.5	49	248.6	4.4	49	250.6	4.7
50	248.8	4.6	50	248.7	4.5	50	250.5	4.2	50	250.5	4.4	50	250.6	4.6	50	249.1	4.4	50	250.2	4.4	50	248.6	4.7
51	250.2	4.4	51	250.0	4.2	51	249.3	4.0	51	250.3	3.8	51	249.9	4.4	51	249.6	4.3	51	249.7	4.0	51	251.3	4.7
52	249.4	4.4	52	248.4	4.3	52	250.3	4.2	52	249.8	4.2	52	250.7	4.7	52	251.4	4.7	52	251.2	4.6	52	250.9	4.9
53 f	251.2	1.4	53 f	249.9	1.5	53 f	250.6	1.5	53 f	250.3	1.5	53 f	250.0	1.4	53 f	250.7	1.6	53 f	250.7	1.6	53 f	250.7	1.6
54	249.9	4.2	54	249.4	4.0	54	249.4	3.9	54	251.1	4.2	54	250.2	4.4	54	250.5	4.5	54	250.3	4.5	54	250.2	4.8
55	250.1	4.8	55	251.6	4.6	55	249.5	4.1	55	251.5	4.5	55	249.9	4.7	55	251.3	4.8	55	251.2	4.5	55	251.2	4.9
56	249.7	4.4	56	250.5	4.0	56	250.8	4.2	56	251.3	4.2	56	252.0	4.5	56	250.9	4.3	56	250.5	4.4	56	249.9	4.7
57	249.0	4.6	57	250.5	4.2	57	251.2	4.0	57	250.6	4.3	57	249.6	4.7	57	250.9	4.5	57	248.9	4.6	57	249.9	4.9
58	249.8	4.3	58	249.5	3.9	58	250.2	3.8	58	251.2	4.4</												