

## Fec test report:

Date: 2021-12-01 11:10:17

Tester name: lc

### Test#1 Monitoring values

Failed

0	FEC label	009	OK
1	FEC DC2438 ID	6c0000024dc35c26	OK
2	FEC_T (to 35°C)	22.219	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.334	OK
5	FEC_Vad (1.9V to 2.0V)	1.330	FAIL

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpm 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Failed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 71	FAIL
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 65	FAIL
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 75	FAIL
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 69	FAIL
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 72	FAIL
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 72	FAIL
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 75	FAIL
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 73	FAIL

## FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 22.219 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.667 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 6c0000024dc35c26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 ( Aligned_SCA_Write )
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.330 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.330 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	417.4	11.7	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.1	1 r	511.0	0.0
2 r	348.9	0.7	2 r	311.4	0.7	2 r	304.4	0.7	2 r	311.6	0.7	2 r	285.5	0.7	2 r	315.4	0.7	2 r	294.1	0.7	2 r	300.1	0.7
3	357.7	5.1	3	351.4	4.9	3	155.0	5.1	3	302.8	5.6	3	303.1	7.2	3	259.1	5.9	3	221.0	5.9	3	240.8	6.3
4	244.0	4.4	4	279.8	4.2	4	274.5	4.3	4	256.6	5.4	4	286.9	6.7	4	263.9	5.7	4	226.9	5.9	4	216.7	6.3
5	273.1	4.9	5	223.6	4.6	5	161.8	4.8	5	188.6	5.2	5	323.9	6.4	5	248.7	5.6	5	270.4	5.7	5	224.3	5.7
6	308.1	4.3	6	237.3	4.3	6	182.9	4.3	6	213.0	5.4	6	300.3	6.7	6	231.1	5.6	6	271.2	5.8	6	227.8	6.3
7	325.5	4.9	7	229.6	4.5	7	130.9	4.8	7	238.6	5.5	7	277.5	6.7	7	281.3	5.6	7	216.3	5.5	7	213.1	5.7
8	363.0	4.3	8	305.4	4.2	8	209.8	4.2	8	175.3	5.4	8	263.4	7.0	8	169.6	5.5	8	173.9	5.5	8	303.7	6.2
9	250.6	5.0	9	280.3	4.7	9	131.0	4.9	9	268.6	5.3	9	314.2	6.3	9	170.6	5.4	9	208.4	5.5	9	279.1	5.9
10	337.5	4.4	10	283.2	4.0	10	128.6	4.2	10	191.8	5.1	10	190.1	6.8	10	221.3	5.8	10	193.2	5.8	10	151.5	6.2
11	191.8	4.9	11	235.6	4.8	11	192.2	4.6	11	232.1	5.5	11	253.1	6.3	11	232.7	5.6	11	229.3	5.4	11	307.2	6.0
12	295.4	4.7	12	268.8	4.2	12	166.7	4.2	12	185.0	5.3	12	328.1	6.6	12	201.1	5.9	12	332.0	5.6	12	186.4	6.1
13	205.7	4.7	13	278.9	4.5	13	125.2	4.7	13	248.9	4.9	13	288.3	6.5	13	241.9	5.4	13	207.2	5.6	13	295.6	5.4
14	303.1	4.3	14	197.2	4.2	14	122.7	4.2	14	216.6	4.9	14	283.9	6.5	14	280.9	6.0	14	171.1	5.5	14	321.2	5.8
15 f	231.4	1.6	15 f	206.3	1.7	15 f	128.7	1.7	15 f	284.8	1.7	15 f	298.8	1.7	15 f	243.8	1.6	15 f	249.9	1.6	15 f	235.8	1.7
16	281.3	4.9	16	305.2	4.6	16	180.5	4.7	16	257.9	5.0	16	218.7	6.1	16	208.0	5.2	16	239.3	5.4	16	208.4	5.7
17	221.3	4.2	17	278.0	4.3	17	234.3	4.2	17	321.3	5.0	17	282.4	6.6	17	255.8	5.5	17	278.5	5.5	17	179.5	6.3
18	231.2	4.7	18	278.8	4.5	18	188.0	4.9	18	225.3	5.1	18	267.9	6.3	18	291.7	5.2	18	346.1	5.3	18	157.1	5.4
19	309.7	4.4	19	280.8	4.2	19	226.5	4.3	19	196.2	5.1	19	180.9	6.5	19	201.4	5.8	19	241.6	5.7	19	222.0	6.2
20	265.1	4.5	20	223.0	4.4	20	155.2	4.5	20	248.4	5.0	20	301.3	6.1	20	253.2	5.3	20	207.6	5.2	20	244.8	5.5
21	261.6	4.3	21	236.0	4.2	21	172.8	4.3	21	238.0	5.0	21	208.5	6.5	21	345.3	5.7	21	247.6	5.8	21	172.4	6.2
22	324.4	4.5	22	254.9	4.2	22	221.1	4.4	22	191.0	4.7	22	239.4	6.1	22	263.5	5.4	22	203.6	5.3	22	239.8	5.5
23	338.4	4.4	23	284.4	4.0	23	167.9	4.0	23	211.8	5.0	23	292.1	6.6	23	245.2	5.8	23	195.9	5.5	23	246.2	6.2
24	337.6	4.4	24	280.8	4.4	24	210.0	4.2	24	200.8	4.8	24	157.2	6.4	24	231.5	5.3	24	234.5	5.3	24	243.0	5.7
25	236.2	4.3	25	315.1	4.3	25	132.2	4.4	25	276.2	4.8	25	325.9	6.5	25	283.1	5.9	25	198.0	5.3	25	178.0	6.3
26	312.9	4.8	26	234.5	4.6	26	198.1	4.4	26	217.6	4.8	26	256.4	5.7	26	273.7	5.3	26	284.7	5.5	26	205.5	5.5
27	259.5	4.2	27	225.2	4.2	27	195.8	4.1	27	171.2	4.9	27	298.3	6.6	27	208.3	5.8	27	237.9	5.7	27	209.6	6.1
28 f	275.0	1.7	28 f	197.9	1.7	28 f	200.8	1.7	28 f	227.6	1.8	28 f	253.0	1.6	28 f	254.2	1.7	28 f	281.0	1.7	28 f	215.9	1.8
29	265.4	4.6	29	225.7	4.4	29	208.5	4.7	29	208.9	4.7	29	233.0	5.8	29	244.9	5.4	29	230.4	5.2	29	272.7	5.3
30	269.7	4.3	30	239.4	4.1	30	145.2	4.3	30	241.0	5.0	30	204.8	6.4	30	227.6	5.8	30	278.4	6.0	30	301.7	6.3
31	227.6	4.6	31	310.9	4.4	31	218.8	4.4	31	241.6	4.7	31	311.3	6.0	31	277.7	5.3	31	236.5	5.1	31	377.8	5.5
32	261.1	4.5	32	209.0	4.0	32	243.9	4.6	32	289.2	5.0	32	191.7	6.8	32	257.2	6.0	32	247.3	5.6	32	185.4	6.4
33	277.6	4.7	33	235.3	4.4	33	203.3	4.4	33	275.9	4.8	33	264.2	5.8	33	275.3	5.0	33	165.3	5.1	33	263.1	5.8
34	231.5	4.3	34	255.3	4.1	34	224.1	4.1	34	285.4	5.0	34	294.7	6.7	34	320.9	6.0	34	215.9	6.1	34	214.1	6.2
35	265.2	4.4	35	363.6	4.3	35	201.4	4.5	35	205.1	4.6	35	279.6	5.8	35	314.0	5.4	35	226.9	5.4	35	295.3	5.6
36	303.9	4.5	36	219.6	3.9	36	222.7	4.3	36	267.4	4.8	36	218.0	6.5	36	363.9	6.0	36	191.4	5.9	36	190.0	6.4
37	250.3	4.5	37	223.2	4.2	37	183.1	4.5	37	161.2	4.6	37	279.5	6.5	37	277.2	5.2	37	345.0	5.1	37	237.4	5.7
38	258.1	4.5	38	171.0	3.9	38	226.5	4.2	38	254.8	5.0	38	216.7	6.8	38	282.8	6.2	38	225.1	6.2	38	263.4	6.5
39	290.6	4.7	39	283.9	4.4	39	270.8	4.4	39	208.4	5.4	39	253.5	7.0	39	275.3	6.4	39	219.2	6.5	39	267.7	7.0
40	339.9	4.4	40	137.8	4.1	40	242.0	4.2	40	258.6	5.1	40	205.0	7.0	40	236.4	6.4	40	276.9	6.0	40	265.7	6.8
41	337.7	4.2	41	338.1	3.7	41	299.9	3.6	41	205.7	4.1	41	276.0	5.7	41	280.6	4.9	41	206.7	5.1	41	245.3	6.1
42	247.3	4.5	42	277.9	4.0	42	248.3	4.3	42	195.6	4.1	42	276.0	5.7	42	190.4	4.8	42	211.3	5.5	42	289.3	5.5
43	333.6	4.1	43	305.1	3.7	43	225.8	4.0	43	239.4	3.9	43	314.4	5.5	43	315.1	4.9	43	231.7	5.3	43	314.0	5.6
44	316.2	4.5	44	216.3	4.0	44	297.1	4.2	44	250.8	4.3	44	226.3	5.5	44	264.2	4.9	44	296.1	5.1	44	244.0	5.7
45	297.3	4.0	45	257.5	3.8	45	221.1	4.1	45	194.0	3.9	45	327.6	5.4	45	293.3	5.1	45	285.0	5.1	45	262.1	5.8
46	256.6	4.5	46	178.6	4.1	46	289.0	4.0	46	217.6	4.1	46	265.7	5.3	46	245.9	5.1	46	220.6	5.2	46	181.4	5.4
47	280.3	4.1	47	279.3	3.8	47	281.0	4.0	47	232.6	3.9	47	239.0	5.4	47	273.3	4.7	47	244.5	5.2	47	330.9	5.6
48	236.8	4.3	48	313.7	4.2	48	155.7	4.5	48	240.3	4.3	48	241.1	5.3	48	216.4	4.9	48	205.6	5.1	48	271.3	5.7
49	178.7	4.2	49	343.1	3.9	49	284.4	4.0	49	243.4	4.1	49	247.8	5.5	49	330.1	4.8	49	221.0	4.9	49	259.3	5.5
50	246.6	4.5	50	267.0	4.1	50	282.1	4.3	50	242.2	4.3	50	303.7	5.0	50	316.1	5.1	50	242.5	5.0	50	282.6	5.7
51	194.8	4.3	51	300.1	3.8	51	179.5	3.9	51	193.7	3.9	51	279.2	5.2	51	207.0	4.7	51	326.8	5.0	51	327.9	5.7
52	303.7	4.7	52	266.2	3.9	52	166.5	4.4	52	283.1	4.2	52	262.5	5.1	52	252.7	4.8	52	209.6	5.2	52	232.0	5.7
53 f	261.2	1.4	53 f	315.0	1.5	53 f	186.0	1.5	53 f	138.0	1.5	53 f	257.2	1.6	53 f	205.1	1.5	53 f	250.5	1.6	53 f	245.7	1.5
54	257.3	4.2	54	213.3	4.0	54	193.6	3.9	54	245.8	4.0	54	253.2	5.1	54	237.4	4.5	54	199.4	4.8	54	252.5	5.5
55	324.6	4.4	55	281.5	4.1	55	223.4	4.2	55	231.0	4.7	55	269.5	5.2	55	255.6	4.8	55	108.2	4.9	55	202.6	5.4
56	219.9	4.4	56	249.1	3.7	56	154.8	4.0	56	199.5	3.8	56	259.3	5.0	56	243.9	4.8	56	279.2	4.7	56	189.7	5.5
57	310.8	4.5	57	345.4	4.5	57	163.4	4.4	57	209.6	4.2	57	259.2	5.3	57	256.8	4.8	57	186.6	4.9	57	154.5	5.7
58	279.8	4.4	58	268.6	3.9	58	199.2	3.8	58	204.8	3.9	58	238.1	5.									



Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	395.8	10.4	1 r	467.5	6.6	1 r	251.9	11.9	1 r	322.4	10.4	1 r	366.4	14.0	1 r	303.0	11.2	1 r	276.7	11.8	1 r	324.3	10.2
2 r	250.0	0.7	2 r	250.8	0.7	2 r	250.9	0.7	2 r	249.7	0.7	2 r	249.8	0.7	2 r	250.7	0.7	2 r	250.3	0.7	2 r	250.3	0.7
3	250.1	4.9	3	250.9	4.8	3	251.2	5.0	3	250.0	5.6	3	251.9	6.7	3	249.8	5.5	3	249.1	5.5	3	250.2	5.9
4	250.9	4.2	4	251.0	4.1	4	251.3	4.4	4	251.5	5.1	4	249.4	6.5	4	249.7	5.1	4	250.4	5.2	4	248.6	5.6
5	250.1	5.0	5	249.3	4.6	5	250.2	5.0	5	249.2	5.4	5	251.3	6.4	5	248.6	5.3	5	252.4	5.4	5	250.1	5.4
6	250.3	4.5	6	249.9	4.3	6	250.2	4.5	6	250.7	5.1	6	250.0	6.2	6	249.3	5.0	6	250.4	5.2	6	249.6	5.7
7	249.7	4.9	7	250.8	4.6	7	250.9	4.7	7	250.6	5.2	7	250.0	6.3	7	250.4	5.3	7	251.0	5.0	7	249.6	5.3
8	250.0	4.4	8	250.1	4.2	8	250.5	4.2	8	251.1	5.1	8	252.5	6.3	8	250.2	5.2	8	251.5	5.1	8	248.8	5.6
9	249.2	5.1	9	249.1	4.9	9	250.3	4.7	9	249.7	5.1	9	249.8	6.3	9	250.7	5.1	9	250.4	5.1	9	250.3	5.2
10	250.3	4.3	10	250.3	4.0	10	249.2	4.3	10	250.2	5.4	10	252.2	6.5	10	250.1	5.2	10	250.0	5.2	10	251.5	5.5
11	251.3	4.6	11	250.1	4.6	11	249.7	4.8	11	250.0	5.1	11	250.3	5.8	11	249.6	5.4	11	250.5	5.2	11	251.1	5.5
12	252.1	4.6	12	251.1	4.3	12	250.6	4.2	12	250.5	5.0	12	251.3	6.3	12	250.5	5.0	12	250.4	5.2	12	250.8	5.8
13	250.2	4.7	13	251.2	4.5	13	249.8	4.8	13	251.7	5.2	13	250.3	6.2	13	249.4	5.2	13	251.7	5.0	13	249.4	5.3
14	250.5	4.4	14	251.2	3.9	14	249.7	4.2	14	249.0	5.0	14	249.5	6.2	14	250.8	5.4	14	249.7	5.3	14	249.9	5.6
15 f	251.0	1.7	15 f	250.8	1.6	15 f	250.2	1.7	15 f	249.9	1.7	15 f	249.8	1.6	15 f	250.3	1.6	15 f	250.0	1.7	15 f	250.5	1.6
16	250.5	4.7	16	251.7	4.5	16	250.7	4.5	16	250.3	4.8	16	249.0	6.0	16	251.4	5.0	16	251.2	5.2	16	250.5	5.2
17	250.8	4.3	17	250.0	4.2	17	252.0	4.5	17	250.1	5.2	17	250.8	6.1	17	251.8	5.2	17	249.0	5.0	17	250.1	5.5
18	251.1	4.5	18	249.9	4.3	18	250.3	4.6	18	249.0	4.9	18	249.6	5.6	18	250.3	4.9	18	250.6	4.9	18	251.6	5.1
19	251.3	4.4	19	250.5	4.0	19	249.0	4.2	19	250.7	5.0	19	249.9	6.3	19	250.8	5.4	19	249.7	5.2	19	251.7	6.0
20	250.2	4.8	20	250.8	4.3	20	250.3	4.6	20	251.4	4.8	20	252.1	5.6	20	249.2	4.9	20	249.4	5.3	20	249.6	5.1
21	250.1	4.2	21	251.2	4.1	21	250.2	4.3	21	250.7	5.0	21	250.1	6.1	21	251.4	5.2	21	249.6	5.4	21	250.5	5.7
22	251.7	4.6	22	250.0	4.4	22	250.1	4.3	22	250.3	4.6	22	251.6	5.7	22	249.7	4.8	22	250.4	4.9	22	249.7	5.0
23	251.0	4.2	23	250.5	4.0	23	250.6	4.3	23	250.1	4.9	23	250.4	5.7	23	248.8	5.1	23	250.4	5.4	23	250.3	5.6
24	249.1	4.5	24	249.7	4.3	24	249.9	4.3	24	251.5	4.9	24	251.1	5.5	24	250.8	5.0	24	249.2	5.1	24	248.5	5.0
25	250.4	4.6	25	250.5	3.8	25	251.2	4.2	25	251.5	4.9	25	251.7	6.1	25	249.9	5.3	25	250.9	5.2	25	249.9	5.8
26	250.8	4.7	26	249.6	4.3	26	249.9	4.2	26	250.1	4.8	26	251.4	5.4	26	248.6	4.9	26	249.2	4.9	26	251.9	4.9
27	250.0	4.3	27	250.3	3.9	27	249.5	4.1	27	250.0	4.8	27	250.7	6.1	27	249.7	5.3	27	249.6	5.2	27	250.5	5.8
28 f	250.4	1.7	28 f	251.0	1.7	28 f	250.7	1.7	28 f	250.1	1.7	28 f	250.4	1.6	28 f	250.4	1.8	28 f	250.2	1.8	28 f	250.4	1.8
29	250.8	4.4	29	249.2	4.4	29	249.3	4.5	29	250.5	4.6	29	252.4	5.8	29	250.9	5.0	29	250.0	5.2	29	250.5	5.2
30	249.1	4.4	30	249.7	4.1	30	251.5	4.2	30	250.1	4.9	30	251.1	6.2	30	250.4	5.6	30	251.7	5.5	30	249.7	5.8
31	250.3	4.6	31	251.1	4.2	31	250.3	4.4	31	249.2	4.6	31	249.7	5.3	31	250.0	4.8	31	250.6	4.9	31	249.8	5.0
32	250.9	4.3	32	250.3	4.1	32	249.4	4.2	32	250.3	4.7	32	249.7	6.4	32	249.9	5.5	32	249.7	5.4	32	250.6	6.0
33	250.3	4.6	33	250.3	4.2	33	251.2	4.4	33	247.9	4.7	33	249.7	5.8	33	248.7	5.1	33	250.8	4.9	33	250.2	5.3
34	252.0	4.2	34	250.3	4.1	34	251.4	4.5	34	250.1	4.7	34	249.6	6.1	34	249.3	5.4	34	251.4	5.7	34	251.3	5.8
35	250.5	4.6	35	249.5	4.6	35	250.0	4.3	35	251.1	4.8	35	249.4	5.6	35	250.4	5.1	35	251.8	5.0	35	249.7	5.2
36	248.7	4.2	36	249.1	4.0	36	250.7	4.2	36	250.4	4.9	36	251.2	6.2	36	251.7	5.5	36	249.7	5.4	36	250.3	6.0
37	252.2	4.6	37	251.6	4.4	37	251.3	4.2	37	250.2	4.6	37	250.0	5.6	37	253.2	5.0	37	250.8	5.0	37	251.3	5.1
38	251.1	4.5	38	250.1	4.0	38	251.3	4.2	38	249.6	4.8	38	248.8	6.3	38	250.1	5.7	38	249.8	5.5	38	250.9	6.0
39	251.4	4.8	39	251.1	4.4	39	251.2	4.6	39	251.6	5.1	39	249.9	6.5	39	251.0	6.1	39	250.0	5.9	39	249.8	6.4
40	249.1	4.1	40	249.6	4.0	40	250.1	4.1	40	249.2	4.7	40	250.1	6.5	40	250.9	5.6	40	250.2	5.4	40	250.0	6.0
41	250.1	4.2	41	251.1	3.9	41	250.4	3.8	41	250.9	3.9	41	251.4	5.6	41	249.9	4.7	41	252.2	5.0	41	250.7	5.4
42	251.7	4.7	42	251.0	4.1	42	251.3	3.9	42	248.7	4.3	42	250.6	5.7	42	251.2	4.8	42	249.8	5.0	42	250.9	5.5
43	250.3	4.0	43	251.9	3.9	43	250.1	4.1	43	250.8	4.1	43	251.2	5.3	43	250.6	4.6	43	250.9	4.9	43	250.6	5.2
44	250.6	4.8	44	249.9	4.2	44	251.4	4.1	44	251.5	4.3	44	251.4	5.1	44	249.6	4.9	44	251.1	5.0	44	251.0	5.3
45	251.1	4.3	45	251.3	4.0	45	252.2	3.8	45	249.1	3.9	45	250.4	5.2	45	250.9	4.4	45	250.3	4.9	45	250.7	5.5
46	249.9	4.3	46	249.9	4.1	46	249.7	4.2	46	248.8	4.3	46	250.9	5.1	46	249.6	4.7	46	250.5	4.9	46	249.9	5.6
47	250.2	4.5	47	251.5	3.8	47	250.8	3.9	47	250.2	3.7	47	250.8	5.2	47	251.8	4.8	47	249.0	5.0	47	250.6	5.4
48	250.4	4.4	48	250.2	4.0	48	251.8	4.1	48	251.0	4.4	48	250.3	5.0	48	250.4	5.0	48	250.3	4.7	48	251.2	5.4
49	248.7	4.4	49	250.6	3.9	49	252.3	4.0	49	251.5	4.0	49	249.7	5.1	49	250.5	4.5	49	251.0	4.9	49	251.1	5.4
50	249.7	4.3	50	250.4	3.9	50	249.1	4.0	50	249.7	4.2	50	249.2	5.0	50	250.1	4.5	50	251.1	4.9	50	249.3	5.5
51	249.6	4.2	51	250.0	4.0	51	251.5	3.8	51	250.4	3.9	51	250.8	5.2	51	250.4	4.5	51	251.5	4.7	51	250.5	5.3
52	249.4	4.3	52	252.7	4.3	52	249.1	4.2	52	249.0	4.4	52	249.8	5.0	52	250.6	5.1	52	248.7	4.7	52	250.1	5.2
53 f	250.6	1.4	53 f	249.8	1.4	53 f	250.6	1.5	53 f	250.5	1.4	53 f	250.5	1.6	53 f	250.4	1.4	53 f	250.2	1.6	53 f	249.5	1.4
54	251.7	4.1	54	250.0	3.8	54	250.5	3.8	54	251.0	3.9	54	249.6	5.0	54	249.8	4.6	54	251.4	4.6	54	252.1	5.4
55	250.5	4.6	55	250.9	4.2	55	251.5	4.4	55	249.4	4.1	55	249.2	5.0	55	250.7	4.6	55	249.7	5.2	55	251.1	5.1
56	250.9	4.8	56	251.6	3.7	56	248.6	4.0	56	251.4	3.9	56	251.0	4.9	56	250.3	4.3	56	249.9	4.5	56	250.6	5.4
57	250.5	4.7	57	250.8	4.2	57	250.9	4.4	57	250.3	4.1	57	249.3	5.0	57	250.1	4.9	57	249.4	4.9	57	250.9	5.1
58	249.6	4.0	58	248.6	3.8	58	250.4	3.9	58	249.5	4.												