

Fec test report:

Date: 2021-12-01 11:59:07

Tester name: lc

Test#1 Monitoring values

Passed

0	FEC label	008	OK
1	FEC DC2438 ID	ec0000024d999d26	OK
2	FEC_T (to 35°C)	22.250	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.504	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Failed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV FAILED	FAIL
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Failed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3060	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3003	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3111	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3006	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 29	FAIL
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3067	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3065	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3069	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 22.250 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.752 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: ec0000024d999d26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff0000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad:

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	494.5	10.2	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.1
2 r	299.5	0.7	2 r	271.4	0.7	2 r	297.9	0.7	2 r	315.4	0.7	2 r	251.4	0.7	2 r	332.7	0.7	2 r	300.6	0.7	2 r	286.4	0.8
3	300.0	4.9	3	217.1	4.5	3	330.0	4.8	3	301.8	5.1	3	207.1	6.0	3	320.4	5.2	3	243.1	5.1	3	213.2	5.6
4	229.0	4.2	4	157.4	4.2	4	299.9	4.3	4	182.6	4.8	4	147.6	5.7	4	287.1	4.9	4	257.7	4.9	4	131.7	5.8
5	223.3	4.6	5	185.1	4.5	5	285.3	4.5	5	198.9	4.8	5	207.7	5.8	5	284.5	4.9	5	241.6	4.8	5	194.8	5.4
6	258.5	4.2	6	177.7	4.6	6	186.0	4.1	6	239.0	4.4	6	143.5	6.0	6	326.2	5.1	6	197.1	4.8	6	174.8	5.3
7	259.7	4.6	7	144.3	4.5	7	275.4	4.4	7	181.7	4.7	7	267.0	6.0	7	276.1	4.8	7	180.3	4.8	7	267.4	5.2
8	202.7	4.5	8	114.6	4.3	8	232.9	4.4	8	257.5	4.7	8	147.1	5.7	8	278.4	5.1	8	150.2	4.7	8	187.7	5.4
9	294.2	4.5	9	187.2	4.4	9	258.3	4.6	9	270.6	4.5	9	239.5	5.5	9	381.4	5.0	9	254.3	4.8	9	253.8	5.3
10	329.6	4.5	10	204.8	4.2	10	250.9	4.2	10	158.3	4.7	10	122.6	5.7	10	335.9	4.8	10	180.2	4.9	10	169.9	5.3
11	259.5	4.5	11	182.9	4.4	11	267.7	4.4	11	210.0	4.7	11	222.9	5.9	11	351.6	4.9	11	216.4	5.0	11	256.6	5.3
12	292.9	4.4	12	174.4	4.1	12	340.0	4.4	12	278.1	4.8	12	177.8	6.0	12	337.6	4.8	12	196.9	4.8	12	172.5	5.2
13	289.3	4.3	13	174.4	4.5	13	255.4	4.6	13	205.9	4.4	13	213.6	5.6	13	267.4	4.7	13	288.1	4.8	13	215.8	4.9
14	254.7	4.1	14	152.5	4.1	14	272.4	4.2	14	243.9	4.7	14	134.7	5.8	14	337.0	5.0	14	233.0	4.7	14	296.0	5.3
15 f	237.3	1.7	15 f	215.6	1.6	15 f	248.7	1.6	15 f	216.4	1.7	15 f	266.9	1.7	15 f	266.4	1.6	15 f	325.9	1.7	15 f	265.3	2.0
16	305.1	4.5	16	141.9	4.2	16	240.7	4.4	16	230.9	4.5	16	142.9	5.6	16	287.4	4.6	16	203.7	4.5	16	288.8	5.0
17	215.7	4.4	17	129.6	4.3	17	259.5	4.2	17	165.6	4.8	17	115.8	5.6	17	312.3	4.6	17	318.1	4.9	17	167.7	5.3
18	165.2	4.4	18	192.6	4.3	18	252.4	4.1	18	144.6	4.3	18	235.6	5.4	18	317.4	4.6	18	246.1	5.2	18	221.3	4.9
19	244.3	4.3	19	185.6	4.0	19	260.6	4.8	19	224.4	4.3	19	127.9	5.9	19	231.9	4.8	19	287.2	4.9	19	279.0	5.5
20	287.4	4.4	20	134.5	4.3	20	261.6	4.3	20	166.4	4.7	20	167.0	5.4	20	267.7	5.1	20	187.6	4.7	20	254.2	5.0
21	47.8	4.3	21	210.1	4.0	21	216.4	4.0	21	226.2	4.4	21	196.2	5.5	21	291.2	5.2	21	217.5	4.8	21	240.9	5.3
22	231.2	4.3	22	137.3	4.3	22	159.1	4.4	22	186.4	4.6	22	208.6	5.4	22	316.5	4.6	22	244.6	5.1	22	197.4	4.7
23	277.1	4.1	23	287.8	3.9	23	214.4	4.2	23	251.6	4.6	23	162.1	5.8	23	343.4	4.9	23	225.8	4.8	23	200.8	5.3
24	300.0	4.3	24	173.2	4.5	24	319.2	4.1	24	254.5	4.5	24	184.0	5.2	24	308.1	5.1	24	186.6	4.8	24	293.1	5.1
25	227.8	4.3	25	148.9	4.0	25	258.1	4.2	25	279.2	4.5	25	172.5	5.9	25	252.1	4.9	25	187.8	4.9	25	196.7	5.2
26	272.7	4.3	26	122.3	4.6	26	198.2	4.2	26	270.9	4.4	26	241.0	5.3	26	312.4	4.7	26	181.3	4.6	26	225.8	5.1
27	265.4	4.5	27	121.7	4.1	27	207.4	4.1	27	207.8	4.1	27	224.1	5.5	27	287.7	5.0	27	294.3	4.9	27	241.6	5.0
28 f	193.6	1.7	28 f	122.1	1.9	28 f	230.7	1.8	28 f	198.5	1.7	28 f	210.7	1.8	28 f	234.8	1.7	28 f	219.4	1.8	28 f	204.5	1.9
29	341.6	4.6	29	153.4	4.4	29	232.8	4.4	29	194.9	4.4	29	247.0	5.2	29	246.2	5.0	29	127.0	4.5	29	200.9	5.2
30	195.4	4.3	30	223.6	4.2	30	275.9	4.1	30	301.8	4.3	30	127.4	5.5	30	340.3	5.0	30	166.4	5.0	30	255.7	5.5
31	234.3	4.4	31	180.6	4.2	31	311.3	4.2	31	205.3	4.4	31	163.0	5.0	31	264.6	4.7	31	154.2	4.8	31	182.7	5.0
32	216.5	4.3	32	190.2	4.1	32	254.1	4.0	32	236.3	4.1	32	186.4	5.5	32	262.7	4.9	32	295.2	4.8	32	235.6	5.4
33	260.4	4.5	33	195.4	4.3	33	190.6	4.2	33	346.0	4.2	33	157.4	5.1	33	278.9	4.6	33	208.3	4.8	33	270.7	5.0
34	254.4	4.3	34	201.4	3.9	34	259.1	4.1	34	199.2	4.7	34	186.6	5.8	34	283.6	5.1	34	192.7	4.9	34	269.8	5.5
35	278.0	4.7	35	212.8	4.2	35	288.4	4.3	35	251.1	4.5	35	127.9	5.3	35	296.3	4.7	35	250.4	4.8	35	167.6	4.9
36	166.9	4.1	36	154.4	4.2	36	188.8	4.0	36	202.1	4.1	36	210.3	5.4	36	272.7	5.0	36	209.9	5.2	36	273.0	5.6
37	165.5	4.7	37	163.4	4.3	37	323.9	4.3	37	180.7	4.3	37	123.2	5.2	37	283.8	4.7	37	279.8	4.8	37	223.5	4.7
38	204.5	4.3	38	186.7	4.1	38	209.3	4.0	38	216.2	4.6	38	211.8	5.5	38	257.6	4.8	38	190.9	5.0	38	198.2	5.7
39	162.2	4.6	39	203.2	4.2	39	285.4	4.5	39	251.5	4.8	39	169.3	6.1	39	303.6	5.3	39	237.3	5.4	39	183.7	5.8
40	255.8	4.2	40	245.6	4.1	40	250.9	3.9	40	152.4	4.2	40	219.5	5.8	40	307.3	5.2	40	307.3	5.2	40	236.6	5.8
41	176.0	4.1	41	278.1	3.7	41	205.0	3.7	41	226.7	3.8	41	219.1	5.3	41	339.3	4.7	41	177.9	4.6	41	231.9	4.9
42	205.6	4.3	42	165.3	4.0	42	265.5	4.1	42	231.1	3.9	42	218.9	2.3	42	224.4	4.4	42	183.4	4.4	42	143.4	4.8
43	128.7	4.2	43	228.1	3.9	43	237.8	3.8	43	320.2	3.9	43	146.2	2.3	43	270.1	4.5	43	288.6	4.3	43	195.2	5.4
44	178.8	4.2	44	106.5	3.9	44	179.3	4.1	44	227.4	4.0	44	218.6	4.9	44	253.9	4.3	44	212.4	4.4	44	268.3	5.0
45	133.1	4.2	45	204.9	3.9	45	225.0	3.8	45	292.0	4.1	45	217.1	4.8	45	269.3	4.2	45	286.8	4.3	45	208.6	5.0
46	251.3	4.1	46	152.0	4.0	46	312.6	3.9	46	242.6	4.1	46	186.2	4.9	46	321.0	4.5	46	266.1	4.2	46	283.9	4.8
47	249.2	4.2	47	208.4	3.8	47	234.9	3.8	47	220.8	4.0	47	113.0	5.1	47	366.1	4.4	47	301.1	4.5	47	213.7	4.9
48	257.5	4.2	48	199.2	4.3	48	234.9	4.0	48	209.4	3.8	48	160.6	5.0	48	241.2	4.3	48	234.7	4.5	48	246.9	5.0
49	169.1	4.2	49	92.8	4.0	49	221.7	4.0	49	220.5	4.0	49	221.3	4.9	49	218.4	4.2	49	257.4	4.4	49	236.9	4.8
50	246.0	4.4	50	170.7	4.1	50	335.9	4.0	50	176.5	3.8	50	131.3	4.9	50	241.5	4.4	50	259.9	4.5	50	281.0	5.1
51	161.0	4.2	51	125.4	3.6	51	265.2	4.0	51	250.8	4.0	51	158.2	4.8	51	305.8	4.5	51	233.2	4.1	51	330.2	5.0
52	259.7	4.5	52	173.2	4.2	52	278.2	4.5	52	208.2	3.8	52	162.4	4.8	52	241.5	4.1	52	239.7	4.5	52	302.9	4.9
53 f	285.8	1.5	53 f	136.5	1.4	53 f	269.9	1.6	53 f	235.2	1.3	53 f	115.7	1.5	53 f	318.8	1.7	53 f	203.9	1.5	53 f	231.0	1.6
54	223.0	4.0	54	283.6	3.8	54	229.3	4.3	54	182.2	3.7	54	146.4	4.5	54	286.9	4.6	54	270.2	4.5	54	245.3	5.1
55	172.4	4.2	55	214.7	4.1	55	250.2	4.0	55	202.1	3.9	55	249.9	4.7	55	365.1	4.4	55	241.4	4.7	55	226.6	5.3
56	214.2	3.8	56	131.5	4.0	56	216.5	3.8	56	220.0	3.9	56	113.5	4.6	56	270.2	4.1	56	216.0	4.4	56	249.5	4.9
57	280.6	4.4	57	115.1	4.0	57	330.9	4.3	57	283.1	4.4	57	212.1	5.0	57	281.8	4.5	57	265.2	4.3	57	262.7	4.8
58	282.0	4.2	58	173.8	3.8	58	128.5	4.0	58	241.6	3.7	58	274.7	4.5</									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	368.6	10.1	1 r	301.3	9.1	1 r	420.2	10.2	1 r	376.4	9.4	1 r	251.3	11.8	1 r	434.7	9.7	1 r	285.4	8.5	1 r	275.4	10.3
2 r	249.9	0.7	2 r	250.8	0.7	2 r	250.2	0.7	2 r	250.8	0.7	2 r	250.9	0.7	2 r	250.0	0.6	2 r	250.1	0.7	2 r	251.2	0.7
3	251.1	5.0	3	249.8	4.6	3	251.0	5.0	3	250.3	5.1	3	250.9	6.3	3	251.5	5.2	3	251.5	5.1	3	250.6	5.5
4	250.7	4.5	4	249.8	4.2	4	250.7	4.2	4	251.0	4.7	4	249.5	5.8	4	251.3	4.7	4	250.5	4.9	4	250.7	5.7
5	251.4	5.0	5	250.3	4.7	5	251.0	4.7	5	251.3	4.8	5	251.6	6.1	5	249.7	5.2	5	250.3	5.0	5	251.1	5.2
6	251.0	4.4	6	249.8	4.0	6	252.7	4.5	6	251.3	4.7	6	251.7	6.0	6	251.5	4.8	6	251.4	4.9	6	250.6	5.2
7	249.9	4.8	7	250.3	4.2	7	250.6	4.5	7	248.8	5.0	7	250.0	5.9	7	249.3	5.0	7	250.9	5.0	7	251.7	5.2
8	250.1	4.5	8	250.8	4.3	8	250.5	4.1	8	251.2	4.9	8	251.2	5.8	8	252.2	4.9	8	250.7	4.8	8	250.3	5.3
9	251.8	5.0	9	249.7	4.3	9	249.3	4.5	9	249.2	4.9	9	250.7	5.7	9	252.2	4.8	9	251.4	4.8	9	249.8	5.1
10	250.1	4.3	10	251.1	4.1	10	249.5	4.2	10	251.8	4.8	10	250.7	5.9	10	252.0	4.9	10	251.0	4.9	10	251.3	5.2
11	250.8	4.8	11	251.7	4.8	11	251.8	4.5	11	250.5	4.8	11	250.7	5.9	11	248.9	5.0	11	249.9	5.1	11	249.5	5.1
12	250.8	4.3	12	250.3	4.2	12	251.9	4.2	12	250.1	4.7	12	250.5	5.7	12	250.0	5.1	12	250.7	4.9	12	251.3	5.3
13	249.7	4.5	13	252.3	4.6	13	251.2	4.3	13	250.2	4.5	13	250.3	5.8	13	251.2	5.0	13	251.6	4.9	13	250.3	5.1
14	250.0	4.4	14	251.6	4.1	14	251.3	4.1	14	250.4	4.5	14	249.9	5.9	14	251.2	5.0	14	251.2	5.0	14	251.8	5.2
15 f	251.2	1.7	15 f	249.6	1.6	15 f	250.0	1.6	15 f	250.8	1.6	15 f	250.6	1.7	15 f	250.4	1.6	15 f	249.9	1.8	15 f	250.3	1.7
16	249.4	4.7	16	249.7	4.4	16	250.5	4.6	16	250.2	4.4	16	251.2	5.9	16	251.1	4.9	16	249.1	4.8	16	251.2	5.0
17	249.5	4.4	17	250.1	4.3	17	251.8	4.6	17	250.0	4.7	17	249.7	5.5	17	250.0	4.8	17	251.3	5.0	17	250.1	5.2
18	251.6	4.5	18	249.9	4.4	18	250.2	4.3	18	249.5	4.5	18	251.6	5.9	18	250.0	4.7	18	250.9	4.6	18	251.3	4.9
19	250.7	4.4	19	248.9	4.1	19	248.8	4.3	19	251.9	4.3	19	250.5	5.9	19	250.8	4.7	19	250.9	5.1	19	251.4	5.5
20	251.1	4.5	20	250.5	4.2	20	250.3	4.5	20	250.6	4.6	20	251.3	5.4	20	250.3	4.8	20	249.4	4.8	20	249.8	4.8
21	248.4	4.5	21	250.6	4.0	21	250.2	4.2	21	248.8	4.7	21	250.4	5.7	21	250.7	4.9	21	250.1	5.0	21	250.2	5.3
22	250.7	4.4	22	251.0	4.4	22	249.7	4.4	22	251.0	4.6	22	253.0	5.6	22	247.8	4.7	22	250.8	4.9	22	252.2	5.1
23	251.9	4.3	23	250.1	3.9	23	252.0	4.2	23	250.1	4.5	23	250.6	5.5	23	251.7	4.8	23	250.1	4.7	23	250.7	5.2
24	250.2	4.6	24	251.1	4.3	24	250.4	4.3	24	249.6	4.4	24	250.2	5.4	24	249.9	4.7	24	248.8	4.5	24	250.7	4.8
25	250.3	4.6	25	250.4	4.0	25	251.8	4.3	25	251.5	4.4	25	251.5	5.8	25	250.6	5.1	25	249.4	4.7	25	251.4	5.3
26	252.0	4.6	26	250.2	4.3	26	249.9	4.4	26	251.8	4.5	26	250.4	5.6	26	250.9	4.9	26	251.4	4.7	26	250.6	4.8
27	251.5	4.1	27	250.5	4.1	27	252.1	4.0	27	251.6	4.5	27	251.0	5.5	27	251.7	4.9	27	251.2	4.7	27	251.7	5.0
28 f	250.4	1.6	28 f	251.0	1.8	28 f	250.1	1.8	28 f	250.1	1.8	28 f	250.0	1.8	28 f	250.1	1.6	28 f	250.9	1.8	28 f	251.2	1.9
29	249.8	4.6	29	251.9	4.3	29	252.8	4.3	29	250.9	4.4	29	250.1	5.1	29	250.7	4.8	29	250.3	4.7	29	251.4	5.2
30	251.1	4.4	30	249.9	4.1	30	250.2	4.1	30	250.3	4.5	30	250.6	5.7	30	251.3	4.9	30	251.1	4.9	30	252.2	5.4
31	251.2	4.6	31	250.1	4.4	31	250.3	4.5	31	249.8	4.3	31	251.4	5.6	31	249.8	4.6	31	249.2	4.6	31	250.7	5.0
32	250.0	4.2	32	250.7	4.2	32	250.7	4.2	32	250.6	4.0	32	251.2	5.5	32	250.2	4.9	32	250.4	5.0	32	250.6	5.3
33	249.5	4.4	33	250.3	4.5	33	251.4	4.2	33	250.8	4.7	33	251.2	5.7	33	250.2	4.8	33	250.5	4.8	33	250.9	5.0
34	251.3	4.1	34	250.1	3.9	34	250.1	3.9	34	250.2	4.4	34	251.1	5.7	34	250.2	5.1	34	250.1	4.8	34	249.9	5.5
35	250.7	4.5	35	250.6	4.2	35	250.2	4.3	35	249.4	4.4	35	251.4	5.4	35	250.2	4.8	35	250.3	4.7	35	251.1	5.0
36	249.0	4.3	36	251.6	4.1	36	249.1	4.2	36	250.7	4.3	36	251.3	5.5	36	249.6	5.1	36	250.7	5.0	36	251.3	5.3
37	251.2	4.6	37	251.4	4.6	37	250.6	4.5	37	250.8	4.2	37	251.2	5.3	37	251.4	4.8	37	250.6	5.0	37	250.1	5.2
38	250.2	4.2	38	252.0	4.1	38	250.0	4.0	38	249.4	4.6	38	250.1	5.5	38	250.1	5.0	38	250.2	4.9	38	252.7	5.5
39	250.6	4.7	39	252.3	4.5	39	251.8	4.5	39	250.9	4.9	39	250.2	6.3	39	249.4	5.5	39	252.2	5.4	39	249.5	5.9
40	249.6	4.2	40	249.6	4.2	40	250.8	4.0	40	250.7	4.4	40	251.2	5.9	40	250.7	5.2	40	249.5	5.0	40	251.9	5.3
41	251.4	4.0	41	251.4	3.7	41	250.5	3.9	41	250.7	3.9	41	249.9	5.3	41	251.2	4.5	41	250.3	4.5	41	251.1	4.9
42	251.7	4.2	42	249.9	3.7	42	252.7	4.0	42	251.1	4.1	42	250.2	2.2	42	250.7	4.4	42	251.0	4.5	42	252.5	4.9
43	251.8	4.2	43	250.5	3.8	43	249.2	3.9	43	250.0	4.0	43	250.6	2.7	43	249.9	4.3	43	250.3	4.9	43	252.2	5.0
44	249.5	4.3	44	251.5	3.9	44	250.1	4.1	44	251.3	3.8	44	249.5	4.9	44	250.7	4.6	44	251.8	4.3	44	252.0	5.2
45	250.9	4.0	45	251.2	4.0	45	250.3	4.3	45	251.0	3.7	45	251.1	5.0	45	251.2	4.2	45	251.1	4.2	45	250.6	5.1
46	250.5	4.2	46	250.7	3.9	46	249.1	4.1	46	250.2	4.0	46	251.1	4.8	46	251.0	4.4	46	251.9	4.6	46	251.5	5.0
47	250.9	4.6	47	251.4	3.8	47	249.6	4.0	47	251.2	4.0	47	251.6	5.0	47	251.2	4.3	47	251.1	4.6	47	250.9	4.9
48	249.3	4.2	48	249.9	4.1	48	251.0	4.1	48	251.4	4.5	48	250.8	5.0	48	250.4	4.4	48	250.1	4.6	48	251.1	5.0
49	250.3	4.4	49	250.7	3.8	49	251.1	3.9	49	251.0	4.3	49	251.8	4.7	49	251.0	4.3	49	252.2	4.2	49	250.9	4.8
50	249.9	4.3	50	250.2	4.0	50	252.2	4.0	50	251.2	4.2	50	251.2	4.8	50	250.5	4.3	50	250.1	4.5	50	251.2	5.0
51	250.3	4.1	51	251.7	4.1	51	251.7	4.0	51	251.7	3.6	51	252.4	4.8	51	250.2	4.3	51	250.0	4.5	51	250.2	4.8
52	249.6	4.4	52	251.1	4.0	52	251.1	3.9	52	250.4	4.0	52	252.7	4.8	52	250.3	4.3	52	250.1	4.3	52	250.4	4.6
53 f	250.4	1.6	53 f	251.5	1.5	53 f	250.0	1.6	53 f	250.7	1.3	53 f	250.8	1.5	53 f	249.7	1.5	53 f	250.3	1.5	53 f	249.9	1.5
54	251.0	4.5	54	250.5	4.0	54	251.5	3.9	54	251.1	4.1	54	250.6	4.7	54	249.1	4.1	54	250.5	4.4	54	252.1	4.7
55	250.1	4.4	55	250.8	4.1	55	250.5	3.9	55	250.8	4.0	55	250.9	5.0	55	250.3	4.5	55	251.4	4.5	55	248.1	5.0
56	251.7	4.1	56	251.9	3.7	56	249.8	4.0	56	250.3	3.8	56	251.1	4.7	56	250.6	4.2	56	251.8	4.3	56	250.3	5.1
57	250.9	4.5	57	250.2	4.1	57	249.8	4.1	57	250.3	4.2	57	249.3	5.0	57	251.3	4.4	57	251.5	4.5	57	249.8	4.9
58	250.9	4.2	58	250.1	3.7	58	250.8	4.0	58	250.3	3.8												