

Fec test report:

Date: 2021-03-10 15:36:00

Tester name: Boris

Test#1 Monitoring values

Failed

0	FEC label	007	OK
1	FEC DC2438 ID	e30000024da8fa26	OK
2	FEC_T (to 35°C)	27.625	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	2.798	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.2 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3041	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3014	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3075	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2984	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3077	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3015	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3059	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3021	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 27.625 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 1.399 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: e30000024da8fa26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	510.6	1.3	1 r	511.0	0.0	1 r	511.0	0.0
2 r	395.3	0.7	2 r	345.9	0.7	2 r	307.4	0.7	2 r	353.4	0.7	2 r	290.7	0.7	2 r	331.2	0.7	2 r	325.6	0.7	2 r	307.9	0.7
3	335.4	4.5	3	341.0	4.2	3	258.5	4.7	3	266.4	5.1	3	245.4	5.2	3	206.5	4.3	3	277.3	5.0	3	328.1	4.7
4	358.3	4.0	4	342.3	4.2	4	330.1	4.1	4	207.7	5.0	4	272.4	4.7	4	229.2	4.4	4	296.1	4.6	4	251.4	4.7
5	364.1	4.1	5	323.2	4.5	5	161.1	4.3	5	282.4	5.0	5	261.7	4.8	5	214.7	4.5	5	278.1	4.8	5	241.2	4.7
6	320.9	4.2	6	215.7	4.1	6	294.1	4.2	6	246.4	4.7	6	155.6	4.9	6	213.3	4.1	6	279.4	4.5	6	261.3	4.6
7	338.1	4.3	7	297.8	4.2	7	245.6	4.3	7	272.0	5.2	7	253.7	4.6	7	249.7	4.5	7	294.0	4.4	7	208.0	4.7
8	328.1	4.1	8	268.5	4.2	8	256.8	4.2	8	203.3	4.4	8	286.3	4.7	8	169.8	4.4	8	307.4	4.4	8	267.1	4.6
9	268.8	4.1	9	335.4	4.2	9	261.2	4.5	9	351.3	4.9	9	190.6	4.6	9	284.2	4.1	9	307.6	4.5	9	250.7	4.9
10	287.7	4.1	10	268.9	4.0	10	229.8	4.1	10	227.1	4.6	10	190.5	4.8	10	237.8	4.2	10	273.8	4.8	10	231.7	4.6
11	276.1	4.1	11	310.1	4.2	11	284.2	4.3	11	257.5	4.7	11	183.3	4.5	11	208.7	4.3	11	251.8	4.7	11	277.8	4.7
12	333.7	4.1	12	279.6	4.0	12	327.4	4.2	12	264.1	4.4	12	271.8	4.6	12	253.2	4.1	12	350.7	4.7	12	240.2	4.6
13	247.0	4.2	13	296.2	4.1	13	249.5	4.2	13	234.8	4.9	13	258.2	4.5	13	228.9	4.0	13	289.8	4.5	13	315.6	4.8
14	276.0	3.8	14	278.9	4.2	14	237.3	4.1	14	270.3	4.5	14	235.1	4.7	14	226.1	4.4	14	266.7	4.6	14	224.0	4.7
15 f	315.1	1.6	15 f	229.3	1.8	15 f	250.2	1.7	15 f	308.1	1.7	15 f	298.6	1.8	15 f	322.1	1.7	15 f	307.8	1.8	15 f	237.4	1.8
16	308.5	4.1	16	212.0	4.0	16	332.2	4.2	16	211.0	4.6	16	186.8	4.4	16	246.6	4.0	16	367.5	4.6	16	261.8	4.7
17	365.7	4.0	17	321.3	4.0	17	252.1	4.3	17	283.0	4.5	17	180.6	4.7	17	204.8	4.2	17	181.6	4.7	17	225.5	4.4
18	437.4	4.0	18	198.6	4.1	18	294.6	4.5	18	244.7	4.7	18	172.7	4.6	18	171.6	4.1	18	331.8	4.3	18	222.6	4.7
19	345.4	4.1	19	284.8	3.9	19	243.1	4.2	19	282.6	4.4	19	204.1	4.6	19	220.6	4.3	19	286.0	4.5	19	290.5	4.8
20	262.9	4.4	20	282.2	4.0	20	268.3	4.2	20	241.2	4.4	20	240.5	4.4	20	130.4	4.3	20	319.4	4.6	20	237.3	4.5
21	323.9	4.0	21	287.2	4.0	21	260.8	4.3	21	262.1	4.4	21	174.8	4.6	21	239.0	4.1	21	291.2	4.6	21	230.0	4.7
22	252.9	4.0	22	333.3	4.0	22	239.7	4.2	22	248.9	4.6	22	226.8	4.5	22	239.4	4.2	22	232.1	4.4	22	282.1	4.7
23	304.4	4.1	23	277.4	3.9	23	235.9	4.2	23	270.0	4.5	23	156.6	4.3	23	201.9	4.4	23	262.5	4.5	23	264.1	4.8
24	300.1	4.0	24	255.6	4.0	24	224.2	4.1	24	259.9	4.5	24	139.7	4.5	24	135.4	4.2	24	264.4	4.2	24	239.7	4.6
25	299.9	4.2	25	214.6	3.9	25	225.6	4.2	25	265.2	4.4	25	219.5	4.6	25	212.0	4.2	25	337.7	5.0	25	294.5	4.7
26	357.5	4.1	26	263.0	4.2	26	204.9	4.5	26	225.4	4.5	26	276.2	4.4	26	275.7	4.4	26	287.5	4.3	26	226.1	4.6
27	277.5	4.0	27	308.4	3.8	27	248.5	4.0	27	306.4	4.0	27	238.1	4.6	27	287.2	4.2	27	284.0	4.3	27	229.8	4.9
28 f	340.4	1.6	28 f	276.3	1.7	28 f	303.2	2.0	28 f	249.3	1.7	28 f	123.2	1.8	28 f	225.1	1.7	28 f	205.0	2.0	28 f	180.5	1.8
29	322.6	4.2	29	225.1	4.0	29	207.1	4.2	29	349.8	4.5	29	267.9	4.9	29	222.3	4.2	29	257.1	4.7	29	272.7	4.9
30	248.7	4.0	30	240.3	4.0	30	231.3	4.1	30	300.6	4.2	30	157.9	4.6	30	197.4	4.3	30	291.2	4.4	30	269.3	4.5
31	246.5	4.1	31	213.3	4.0	31	202.8	4.2	31	234.2	4.5	31	203.1	4.4	31	274.4	4.2	31	323.0	4.3	31	191.3	4.6
32	353.8	3.9	32	272.3	3.9	32	307.9	4.2	32	239.1	4.2	32	146.4	4.7	32	246.0	4.3	32	248.2	5.0	32	272.9	4.7
33	279.3	4.1	33	326.9	3.9	33	243.2	4.1	33	249.2	4.5	33	193.6	4.4	33	254.3	4.3	33	232.2	4.5	33	251.4	4.7
34	231.0	4.2	34	246.8	3.9	34	245.4	4.2	34	358.0	4.2	34	278.5	4.6	34	292.6	4.3	34	287.5	4.5	34	279.8	4.6
35	305.8	4.1	35	317.4	4.1	35	237.5	4.2	35	408.0	4.5	35	242.4	4.5	35	249.1	3.9	35	293.9	4.6	35	257.6	4.8
36	310.1	4.0	36	206.1	4.0	36	221.6	4.2	36	305.8	4.5	36	186.3	4.3	36	223.1	4.4	36	323.9	4.5	36	172.3	4.6
37	335.6	4.1	37	225.6	4.1	37	211.8	4.2	37	268.8	4.5	37	219.9	4.3	37	286.7	4.0	37	272.4	4.4	37	342.6	4.6
38	304.9	4.1	38	256.9	3.9	38	264.0	4.1	38	314.8	4.3	38	117.3	4.6	38	230.6	4.3	38	250.3	4.5	38	301.6	5.0
39	414.1	4.3	39	349.2	4.2	39	274.8	4.4	39	228.2	4.8	39	277.3	4.7	39	208.6	4.4	39	294.3	5.3	39	364.5	5.4
40	362.2	4.1	40	300.8	4.3	40	250.8	3.9	40	300.2	4.2	40	162.8	4.6	40	314.8	4.4	40	273.5	4.7	40	248.4	4.9
41	392.2	3.8	41	187.7	3.7	41	254.0	3.7	41	248.8	4.0	41	229.1	4.2	41	335.2	3.8	41	185.4	4.2	41	260.7	4.6
42	336.4	4.0	42	316.8	3.7	42	285.3	3.9	42	366.2	4.1	42	226.2	4.1	42	223.5	4.0	42	195.8	4.1	42	288.4	4.7
43	318.2	3.8	43	291.4	3.8	43	228.8	4.1	43	271.1	4.0	43	234.6	4.1	43	279.4	3.9	43	270.3	4.3	43	261.5	4.4
44	308.4	4.0	44	230.8	4.0	44	253.6	4.0	44	378.6	4.2	44	178.2	4.3	44	235.5	4.0	44	199.9	4.2	44	256.7	4.7
45	361.0	4.0	45	289.8	3.7	45	204.6	4.1	45	283.7	4.1	45	208.8	4.2	45	300.7	3.9	45	255.4	4.2	45	363.9	4.8
46	372.8	3.7	46	226.9	3.7	46	259.8	3.8	46	295.9	3.9	46	271.9	4.2	46	223.6	3.9	46	200.2	4.2	46	258.8	4.6
47	298.3	4.0	47	243.4	3.6	47	241.2	3.9	47	337.6	3.8	47	248.8	4.2	47	279.6	4.1	47	372.4	4.1	47	192.3	4.7
48	345.4	3.9	48	308.3	3.7	48	227.4	4.0	48	232.7	4.3	48	283.6	4.4	48	254.8	4.0	48	278.0	4.2	48	293.2	4.7
49	318.1	4.2	49	253.2	3.7	49	220.1	3.8	49	278.8	3.8	49	226.5	4.2	49	167.6	3.9	49	342.0	4.0	49	208.4	4.5
50	244.6	4.2	50	241.8	3.8	50	198.1	3.9	50	332.9	4.0	50	240.2	4.2	50	216.0	3.9	50	248.5	4.2	50	202.2	4.6
51	286.6	4.0	51	314.4	3.6	51	227.6	3.9	51	286.4	4.0	51	244.2	4.2	51	292.1	4.1	51	233.9	4.2	51	321.9	4.6
52	276.9	4.0	52	193.8	4.3	52	232.8	4.1	52	254.0	3.9	52	198.9	4.2	52	161.2	4.3	52	285.3	4.5	52	312.3	4.7
53 f	207.8	1.6	53 f	345.5	1.7	53 f	219.8	1.7	53 f	349.0	1.6	53 f	191.4	1.7	53 f	283.3	1.6	53 f	229.0	1.6	53 f	203.6	1.5
54	314.8	3.9	54	217.1	3.6	54	194.6	3.9	54	276.1	4.0	54	157.0	4.3	54	162.9	4.0	54	210.6	4.2	54	289.1	4.6
55	359.8	3.9	55	253.6	3.7	55	285.0	4.0	55	235.8	4.2	55	210.9	4.3	55	303.0	4.1	55	290.4	4.4	55	275.5	4.6
56	340.7	4.0	56	232.8	4.0	56	227.4	4.0	56	303.3	3.9	56	129.5	4.1	56	177.3	4.2	56	302.3	4.2	56	323.3	4.5
57	312.9	4.0	57	296.5	3.8	57	257.6	3.8	57	294.8	4.3	57	198.5	4.3	57	271.2	4.0	57	293.4	4.3	57	193.5	4.6
58	269.2	3.8	58	277.3	3.9	58	239.0	3.9	58	240.9	3.9	58	238.6	4.5									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	458.6	7.5	1 r	421.8	7.6	1 r	341.7	9.7	1 r	375.3	8.1	1 r	358.1	10.2	1 r	265.3	9.2	1 r	320.1	10.8	1 r	499.8	6.8
2 r	250.0	0.7	2 r	249.8	0.7	2 r	250.5	0.7	2 r	250.2	0.7	2 r	249.7	0.7	2 r	250.1	0.7	2 r	249.7	0.7	2 r	250.0	0.7
3	249.2	4.7	3	250.9	4.4	3	251.1	4.8	3	249.9	5.6	3	250.3	5.8	3	250.2	4.9	3	249.9	5.0	3	250.8	5.4
4	249.6	4.1	4	251.9	4.0	4	249.5	4.1	4	249.1	4.9	4	248.8	6.0	4	250.9	4.8	4	249.1	5.0	4	250.4	5.1
5	250.8	4.3	5	249.8	4.3	5	249.8	4.7	5	249.5	5.7	5	249.5	5.6	5	248.8	4.6	5	250.3	5.2	5	249.9	5.1
6	249.9	4.2	6	250.4	4.3	6	251.3	4.2	6	251.1	5.0	6	251.0	5.8	6	249.7	4.7	6	249.2	5.1	6	249.7	5.5
7	249.8	4.5	7	249.1	4.2	7	250.4	4.5	7	250.4	5.6	7	249.3	5.5	7	249.4	4.5	7	249.3	4.7	7	249.8	5.1
8	250.0	4.3	8	250.0	4.2	8	249.6	4.4	8	250.9	5.1	8	250.4	6.0	8	249.2	4.6	8	250.3	4.8	8	250.1	4.8
9	249.1	4.3	9	248.3	4.2	9	249.8	4.8	9	250.8	5.3	9	249.1	5.1	9	250.6	4.4	9	248.7	4.8	9	251.5	5.1
10	249.7	4.1	10	250.2	4.0	10	250.9	4.1	10	248.4	4.8	10	251.1	6.1	10	250.3	4.5	10	251.4	4.8	10	248.1	5.3
11	250.8	4.3	11	250.4	4.2	11	250.2	4.5	11	251.1	5.1	11	250.7	5.1	11	251.4	4.5	11	250.5	4.7	11	249.9	5.1
12	250.1	4.2	12	249.8	4.2	12	249.8	4.1	12	250.5	5.0	12	248.9	5.7	12	250.5	4.7	12	250.1	4.6	12	251.1	5.2
13	249.6	4.4	13	249.0	4.3	13	252.0	4.2	13	249.1	5.1	13	251.1	5.1	13	250.3	4.7	13	249.5	4.8	13	249.6	4.9
14	249.5	4.1	14	248.4	4.1	14	249.7	4.2	14	249.2	4.7	14	250.2	5.6	14	251.1	4.5	14	250.0	4.7	14	250.3	4.9
15 f	249.4	1.6	15 f	250.9	1.7	15 f	250.0	1.7	15 f	250.1	1.6	15 f	249.4	1.8	15 f	250.5	1.5	15 f	250.0	1.7	15 f	250.5	1.7
16	250.5	4.3	16	250.6	4.1	16	250.2	4.2	16	250.8	4.9	16	250.3	5.1	16	249.4	4.6	16	250.1	4.6	16	249.8	4.8
17	248.7	4.0	17	250.2	4.1	17	247.6	4.4	17	248.8	4.8	17	250.6	5.7	17	249.4	4.5	17	250.6	4.8	17	250.6	5.0
18	251.5	4.3	18	248.7	4.1	18	250.7	4.4	18	250.4	5.4	18	247.6	5.0	18	251.8	4.4	18	249.7	4.5	18	250.6	5.1
19	249.8	4.1	19	250.2	3.9	19	249.6	4.2	19	251.5	4.9	19	250.2	5.8	19	248.8	4.6	19	250.6	4.7	19	249.3	5.2
20	249.8	4.2	20	248.1	4.1	20	250.2	4.4	20	248.9	4.9	20	251.8	5.1	20	252.3	4.9	20	249.9	4.9	20	250.2	5.0
21	249.8	4.1	21	250.1	3.9	21	250.9	4.0	21	250.0	4.6	21	249.5	5.5	21	251.0	4.7	21	250.2	4.7	21	249.3	5.2
22	250.7	4.5	22	250.3	4.2	22	250.6	4.3	22	250.1	4.7	22	250.1	5.0	22	251.0	4.4	22	250.2	4.7	22	249.2	4.9
23	251.3	4.3	23	249.5	4.2	23	249.2	4.2	23	250.0	4.6	23	249.9	5.3	23	249.7	4.7	23	249.2	4.8	23	249.0	4.8
24	249.1	4.2	24	250.1	4.0	24	249.4	4.2	24	251.2	4.8	24	250.5	5.1	24	252.4	4.6	24	251.3	4.7	24	251.3	4.8
25	249.1	4.0	25	250.3	4.0	25	249.1	4.2	25	251.0	4.6	25	249.7	5.5	25	250.5	4.5	25	250.0	4.8	25	249.9	5.1
26	249.9	4.1	26	249.6	4.0	26	249.8	4.3	26	251.1	4.7	26	250.4	5.0	26	248.0	4.7	26	250.1	4.6	26	248.2	5.0
27	248.8	4.2	27	251.0	3.8	27	250.6	4.0	27	248.5	4.6	27	250.5	5.7	27	251.3	4.8	27	249.3	4.9	27	249.1	5.1
28 f	250.1	1.6	28 f	250.2	1.8	28 f	250.8	1.8	28 f	250.0	1.7	28 f	250.4	1.9	28 f	250.0	1.6	28 f	249.9	1.9	28 f	249.3	1.8
29	250.4	4.1	29	249.4	4.0	29	249.8	4.0	29	249.1	4.9	29	251.6	5.0	29	250.3	4.5	29	250.1	4.6	29	249.3	5.0
30	249.4	4.1	30	251.2	4.0	30	251.6	4.1	30	249.3	4.6	30	250.0	5.4	30	250.7	4.7	30	251.2	4.9	30	251.5	5.5
31	249.4	4.5	31	250.3	4.2	31	250.2	4.3	31	250.6	4.7	31	250.8	4.9	31	250.0	4.5	31	250.9	4.3	31	250.6	4.8
32	247.9	4.1	32	250.1	3.9	32	251.1	4.1	32	250.2	4.5	32	251.1	5.4	32	249.8	4.7	32	250.4	5.0	32	249.0	5.2
33	249.2	4.2	33	248.0	4.0	33	249.4	4.2	33	249.8	4.5	33	250.2	5.0	33	250.9	4.3	33	249.6	4.6	33	250.2	4.9
34	248.8	4.2	34	249.8	4.1	34	250.6	4.1	34	249.1	4.8	34	249.0	5.4	34	249.6	4.7	34	249.1	5.1	34	249.6	5.6
35	251.0	4.2	35	249.7	4.6	35	249.8	4.5	35	250.6	4.6	35	250.3	5.0	35	250.6	4.5	35	250.2	4.9	35	249.5	5.0
36	248.8	4.2	36	251.9	3.8	36	251.1	4.1	36	251.2	4.7	36	248.8	5.6	36	248.8	4.8	36	251.7	4.8	36	250.3	5.4
37	248.5	4.2	37	249.5	4.0	37	249.4	4.1	37	251.1	4.5	37	250.0	5.0	37	249.8	4.6	37	250.6	4.6	37	249.8	5.2
38	250.0	4.4	38	249.8	3.8	38	249.9	4.0	38	249.8	4.8	38	250.5	5.5	38	248.7	4.8	38	249.9	5.0	38	249.7	5.4
39	249.0	4.3	39	251.1	4.4	39	249.9	4.5	39	249.5	5.0	39	251.1	5.7	39	251.6	5.2	39	250.7	5.3	39	249.2	5.9
40	249.8	4.1	40	249.0	3.9	40	249.9	4.0	40	250.1	4.6	40	250.6	5.8	40	249.7	4.8	40	250.7	5.0	40	252.2	5.8
41	250.7	4.3	41	250.7	3.7	41	249.7	4.0	41	250.7	4.1	41	251.8	4.8	41	249.4	4.2	41	250.9	4.4	41	249.1	5.0
42	251.1	4.3	42	250.4	3.7	42	250.3	4.0	42	249.1	4.2	42	251.4	4.6	42	250.9	4.3	42	250.2	4.5	42	249.0	4.9
43	250.7	4.2	43	249.2	3.8	43	251.1	4.0	43	249.4	3.9	43	249.2	4.9	43	249.4	4.3	43	250.1	4.4	43	248.8	4.8
44	250.3	4.5	44	250.1	3.9	44	250.0	4.1	44	249.5	4.2	44	250.8	4.5	44	251.0	4.3	44	249.6	4.3	44	249.9	5.0
45	249.9	4.2	45	249.1	3.8	45	250.4	3.9	45	249.4	4.0	45	249.7	4.5	45	250.9	4.3	45	251.3	4.5	45	249.2	5.4
46	250.1	4.5	46	249.9	3.8	46	249.2	4.0	46	251.9	4.2	46	249.8	4.5	46	250.2	4.2	46	252.1	4.5	46	249.9	5.1
47	249.7	4.1	47	251.1	3.8	47	250.2	4.1	47	249.3	4.2	47	249.3	5.0	47	249.3	4.5	47	249.2	4.9	47	250.2	5.0
48	250.7	4.3	48	251.1	4.0	48	251.5	3.9	48	249.5	4.2	48	249.7	4.7	48	249.4	4.2	48	249.8	4.4	48	251.4	5.0
49	250.8	4.0	49	250.1	3.8	49	250.3	3.9	49	251.4	4.0	49	249.2	4.7	49	249.2	4.0	49	250.0	4.4	49	251.2	4.9
50	248.3	4.2	50	248.7	3.8	50	249.1	4.1	50	250.9	4.2	50	250.7	4.5	50	250.5	4.1	50	249.6	4.6	50	251.2	4.9
51	249.5	4.1	51	249.1	3.9	51	251.3	3.8	51	250.8	4.2	51	249.7	4.6	51	250.7	4.3	51	250.4	4.2	51	250.7	5.2
52	250.5	4.2	52	249.7	4.0	52	249.5	4.3	52	249.2	4.2	52	249.7	4.5	52	250.3	4.4	52	250.7	4.6	52	250.4	4.9
53 f	249.5	1.6	53 f	250.4	1.6	53 f	249.7	1.7	53 f	250.2	1.6	53 f	250.2	1.8	53 f	250.0	1.6	53 f	249.9	1.6	53 f	249.3	1.6
54	249.4	4.1	54	248.4	3.8	54	250.3	4.0	54	250.4	4.1	54	249.3	4.5	54	249.6	4.7	54	250.3	4.5	54	250.1	4.9
55	248.9	4.1	55	250.1	4.1	55	250.6	4.0	55	249.1	4.4	55	251.2	4.6	55	250.3	4.4	55	251.1	4.3	55	249.2	5.1
56	248.2	4.1	56	249.3	4.0	56	250.5	3.8	56	250.7	3.9	56	250.7	4.8	56	251.1	4.2	56	249.8	4.3	56	251.8	4.8
57	250.6	4.3	57	249.2	4.3	57	249.5	4.1	57	250.6	4.2	57	251.3	4.4	57	249.2	4.1	57	251.1	4.5	57	249.9	4.9
58	250.7	4.2	58	250.2	4.2	58	249.8	4.0	58	250.7	3.9												