

Fec test report:

Date: 2021-12-01 10:58:59

Tester name: lc

Test#1 Monitoring values

Passed

0	FEC label	005	OK
1	FEC DC2438 ID	ee0000024da81526	OK
2	FEC_T (to 35°C)	22.156	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.2A to 1.6A)	1.552	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3054	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2988	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3031	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3077	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3092	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3081	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3060	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3031	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdc(2) Fem(00) FEC_T: 22.156 degC
2	fe 0 moni V 0	0	0 Tdc(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdc(2) Fem(00) FEC_I: 0.776 A
8	fe 0 moni S 0	0	0 Tdc(2) Fem(00) FEC_Serial: ee0000024da81526

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdc(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdc(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdc(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdc(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdc(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdc(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdc(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdc(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdc(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdc(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdc(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdc(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdc(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdc(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	510.9	0.6	1 r	511.0	0.0
2 r	314.6	0.7	2 r	339.2	0.6	2 r	277.4	0.7	2 r	299.3	0.7	2 r	261.8	0.7	2 r	299.4	0.7	2 r	287.0	0.7	2 r	368.1	0.8
3	366.9	5.2	3	298.3	4.8	3	209.6	5.1	3	208.3	5.9	3	256.3	7.4	3	224.8	6.0	3	232.4	6.1	3	384.0	6.1
4	317.9	4.5	4	362.7	4.1	4	292.1	4.4	4	296.2	5.3	4	184.7	6.9	4	311.6	5.7	4	328.3	5.6	4	372.6	6.0
5	254.3	5.1	5	401.7	4.8	5	148.8	5.0	5	255.4	5.7	5	306.6	6.7	5	241.8	5.7	5	172.6	5.6	5	330.9	5.8
6	304.1	4.4	6	303.7	4.7	6	287.7	4.3	6	274.9	5.2	6	277.3	6.6	6	329.2	5.6	6	193.1	5.5	6	337.2	6.0
7	353.7	5.0	7	450.1	4.9	7	229.0	4.9	7	196.0	5.5	7	250.2	6.9	7	361.7	5.7	7	210.3	5.3	7	378.6	5.9
8	277.3	4.5	8	388.6	4.4	8	186.8	4.5	8	302.6	5.1	8	269.2	6.7	8	222.2	5.7	8	286.2	5.8	8	390.5	5.8
9	318.4	4.9	9	318.1	4.9	9	158.2	4.8	9	237.9	5.4	9	277.0	6.8	9	359.8	5.4	9	222.6	5.5	9	398.9	5.8
10	307.2	4.5	10	355.6	4.2	10	258.6	4.4	10	168.7	5.1	10	226.9	7.1	10	318.8	5.7	10	227.5	5.4	10	410.2	5.9
11	245.6	4.8	11	398.0	4.5	11	216.9	4.6	11	281.2	5.1	11	299.8	6.5	11	251.3	5.5	11	160.4	5.4	11	324.1	5.5
12	307.9	4.5	12	352.0	4.2	12	177.2	4.5	12	210.6	5.5	12	273.9	6.5	12	248.2	5.7	12	223.8	5.5	12	269.8	6.1
13	312.8	4.8	13	342.9	4.4	13	190.3	4.5	13	230.6	5.2	13	255.1	6.5	13	192.2	5.6	13	126.0	5.6	13	270.4	5.4
14	231.9	4.6	14	355.8	4.2	14	173.9	4.4	14	240.3	5.0	14	266.1	6.5	14	288.5	5.6	14	191.5	5.5	14	340.7	6.0
15 f	358.7	1.6	15 f	310.3	1.6	15 f	257.7	1.6	15 f	202.9	1.8	15 f	207.0	1.6	15 f	292.7	1.6	15 f	224.8	1.6	15 f	321.1	1.6
16	233.9	4.6	16	348.6	4.5	16	215.4	4.8	16	170.6	4.8	16	267.9	6.2	16	314.2	5.4	16	254.0	5.6	16	469.2	5.4
17	321.5	4.2	17	366.7	4.1	17	226.1	4.1	17	221.8	5.0	17	300.9	6.6	17	217.6	5.7	17	152.5	5.6	17	314.4	6.0
18	276.9	5.0	18	291.3	4.6	18	167.7	4.6	18	295.4	5.1	18	162.1	6.6	18	343.8	5.6	18	237.1	5.3	18	311.3	5.5
19	239.6	4.4	19	327.0	4.2	19	184.4	4.1	19	177.5	5.0	19	268.0	6.5	19	275.5	5.6	19	257.0	5.8	19	417.3	6.1
20	301.5	4.7	20	324.8	4.5	20	222.2	4.6	20	196.1	5.2	20	262.0	6.2	20	230.3	5.6	20	234.2	5.3	20	358.4	5.6
21	223.2	4.2	21	389.5	4.1	21	220.0	4.4	21	209.8	5.1	21	168.4	6.5	21	227.1	5.7	21	228.4	5.6	21	337.6	6.1
22	219.5	4.7	22	312.2	4.4	22	248.4	4.2	22	345.9	5.1	22	242.3	6.3	22	209.8	5.3	22	235.8	5.4	22	303.3	5.4
23	327.8	4.4	23	360.1	4.0	23	188.0	4.2	23	166.9	4.8	23	345.7	6.4	23	301.5	5.7	23	264.4	5.5	23	380.9	5.8
24	214.9	5.0	24	217.1	4.3	24	158.6	4.7	24	229.0	4.9	24	184.1	6.1	24	243.2	5.6	24	220.0	5.2	24	291.2	5.5
25	354.0	4.6	25	310.5	4.2	25	241.8	4.0	25	309.6	4.7	25	323.3	6.4	25	314.4	5.5	25	175.8	5.5	25	349.7	6.0
26	205.9	4.7	26	357.6	4.4	26	266.2	4.6	26	165.3	5.2	26	214.2	6.3	26	311.4	5.4	26	225.9	5.1	26	366.9	5.5
27	229.0	4.3	27	337.2	4.2	27	292.3	4.2	27	276.5	4.8	27	257.7	6.5	27	273.2	5.9	27	257.6	5.6	27	311.6	6.1
28 f	265.0	1.8	28 f	415.4	1.6	28 f	203.9	1.7	28 f	288.4	1.9	28 f	230.7	1.6	28 f	208.0	1.8	28 f	207.1	1.8	28 f	320.2	1.8
29	347.6	4.9	29	357.1	4.4	29	349.3	4.4	29	260.1	4.9	29	232.6	6.1	29	306.3	5.4	29	192.7	5.8	29	353.9	5.5
30	260.3	4.6	30	260.0	4.8	30	242.1	4.1	30	175.4	4.8	30	243.6	6.7	30	192.4	5.7	30	279.1	5.5	30	313.4	6.2
31	187.9	4.6	31	314.1	4.4	31	208.9	4.7	31	237.3	5.0	31	306.0	6.1	31	239.3	5.1	31	221.9	5.7	31	257.4	5.4
32	234.5	4.3	32	330.8	4.0	32	164.2	4.4	32	213.6	4.5	32	219.0	6.6	32	197.1	5.9	32	222.2	5.8	32	356.9	6.0
33	231.1	4.7	33	300.6	4.4	33	235.1	4.5	33	253.6	5.0	33	251.6	6.1	33	269.9	5.1	33	190.8	5.5	33	210.0	5.5
34	203.5	4.2	34	318.7	4.2	34	230.1	4.0	34	125.3	4.7	34	184.3	6.4	34	229.2	5.9	34	251.3	5.7	34	321.3	6.1
35	265.9	4.6	35	315.8	4.4	35	271.0	4.3	35	143.5	4.7	35	270.4	6.0	35	202.8	5.5	35	260.9	5.1	35	243.5	5.5
36	290.4	4.5	36	327.7	4.3	36	184.6	4.3	36	246.3	4.7	36	249.9	6.4	36	241.3	6.0	36	390.4	5.7	36	297.0	6.1
37	221.6	4.5	37	234.8	4.3	37	307.9	4.4	37	224.7	5.1	37	355.5	5.8	37	267.7	5.2	37	243.1	5.4	37	296.0	5.3
38	282.6	4.7	38	334.7	4.1	38	278.3	4.0	38	245.6	4.8	38	231.2	6.5	38	195.7	6.0	38	178.7	6.1	38	313.8	6.1
39	231.2	4.9	39	327.0	4.4	39	294.1	4.7	39	195.1	5.3	39	251.6	7.1	39	277.6	6.4	39	205.1	6.3	39	192.0	6.7
40	273.3	4.5	40	316.0	4.4	40	248.0	4.0	40	274.8	4.9	40	174.8	7.1	40	290.7	6.1	40	226.8	6.3	40	294.6	6.6
41	266.8	4.1	41	371.2	3.9	41	223.9	3.9	41	239.2	4.4	41	272.4	5.5	41	272.5	4.9	41	310.1	5.0	41	321.9	5.7
42	291.8	4.3	42	245.0	3.9	42	171.8	4.2	42	175.4	4.3	42	269.9	5.4	42	212.6	4.9	42	187.4	5.2	42	351.6	5.4
43	244.4	4.1	43	268.8	3.8	43	265.2	3.9	43	214.4	4.2	43	288.1	5.3	43	282.9	5.0	43	253.2	4.8	43	302.6	5.3
44	319.7	4.5	44	398.7	4.0	44	156.0	4.1	44	137.9	4.3	44	278.6	5.3	44	339.9	5.1	44	176.6	4.9	44	342.1	5.2
45	249.3	4.0	45	364.9	3.9	45	229.1	4.0	45	205.3	4.2	45	333.3	5.3	45	312.5	4.7	45	220.6	4.9	45	293.0	5.3
46	270.9	4.4	46	325.3	4.2	46	213.2	4.5	46	289.0	4.3	46	235.7	5.3	46	286.5	5.0	46	281.7	4.9	46	339.6	5.6
47	240.9	4.1	47	358.7	3.6	47	295.0	4.0	47	191.0	4.1	47	275.5	5.2	47	294.4	4.6	47	199.3	4.8	47	336.4	5.4
48	160.0	4.4	48	284.5	4.1	48	218.7	4.1	48	210.4	4.3	48	266.2	5.2	48	232.4	4.9	48	224.2	4.8	48	234.6	5.2
49	265.9	4.2	49	310.0	3.7	49	272.4	4.0	49	208.9	4.2	49	286.5	5.2	49	205.9	4.5	49	157.4	5.0	49	336.2	5.7
50	227.4	4.5	50	261.8	4.1	50	240.7	4.0	50	170.1	4.4	50	323.2	5.2	50	285.4	4.7	50	156.0	4.9	50	319.2	5.3
51	288.6	4.3	51	360.0	4.0	51	266.8	3.9	51	293.8	4.0	51	288.9	5.1	51	285.4	4.7	51	214.3	5.0	51	321.3	5.2
52	169.0	4.5	52	360.5	4.2	52	235.9	4.1	52	177.9	4.3	52	174.0	5.2	52	255.2	4.8	52	273.3	4.8	52	335.1	5.4
53 f	208.0	1.4	53 f	350.5	1.5	53 f	269.4	1.6	53 f	274.2	1.6	53 f	255.7	1.7	53 f	176.2	1.5	53 f	228.5	1.6	53 f	322.8	1.5
54	313.6	4.3	54	334.0	3.6	54	256.7	4.0	54	218.8	4.1	54	128.7	5.4	54	286.4	4.5	54	229.3	4.6	54	411.9	5.4
55	184.1	4.5	55	350.3	4.1	55	256.5	4.2	55	155.7	4.5	55	248.4	5.1	55	270.3	4.9	55	212.3	4.9	55	358.6	5.4
56	220.8	4.4	56	317.2	4.3	56	185.0	4.0	56	212.3	4.2	56	175.3	5.2	56	214.1	4.7	56	161.4	4.9	56	364.2	5.4
57	222.8	4.4	57	316.5	4.2	57	205.2	4.2	57	224.4	4.3	57	272.2	5.4	57	326.5	4.7	57	212.2	5.0	57	362.6	5.3
58	272.5	4.1	58	286.6	4.2	58	334.2	3.9	58	245.9	4.1	58	255.8	5.0									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	441.4	10.8	1 r	326.6	10.1	1 r	309.6	8.5	1 r	281.8	9.7	1 r	297.4	10.7	1 r	321.8	8.8	1 r	271.6	11.4	1 r	436.8	12.3
2 r	249.5	0.7	2 r	250.3	0.6	2 r	250.8	0.7	2 r	250.7	0.7	2 r	250.1	0.7	2 r	250.8	0.7	2 r	250.2	0.7	2 r	250.3	0.7
3	249.4	5.0	3	250.5	4.6	3	248.7	4.8	3	250.6	5.3	3	250.2	6.5	3	250.2	5.6	3	249.9	5.5	3	250.1	5.5
4	250.6	4.1	4	250.4	4.1	4	251.8	4.4	4	249.4	4.9	4	249.5	6.0	4	249.1	5.3	4	250.5	5.2	4	249.7	5.5
5	248.7	4.9	5	249.1	4.4	5	249.5	4.7	5	250.9	5.3	5	249.8	6.1	5	250.3	5.1	5	250.7	5.2	5	249.2	5.2
6	250.6	4.8	6	249.8	3.9	6	249.5	4.1	6	250.8	4.8	6	251.3	6.0	6	251.2	5.3	6	249.4	5.1	6	249.6	5.6
7	249.4	4.7	7	250.6	4.3	7	251.4	4.4	7	251.1	5.0	7	249.2	5.8	7	250.5	5.4	7	249.9	5.0	7	251.2	5.1
8	250.3	4.5	8	248.9	4.1	8	249.1	4.3	8	249.0	5.0	8	249.8	6.2	8	250.1	5.6	8	250.3	5.2	8	249.1	5.4
9	249.8	4.6	9	250.3	4.6	9	250.7	4.5	9	249.8	5.0	9	250.9	6.0	9	250.2	5.1	9	250.1	4.9	9	250.7	5.5
10	250.3	4.2	10	249.9	4.0	10	251.3	4.2	10	250.9	5.0	10	250.5	6.1	10	250.0	5.1	10	249.7	5.2	10	251.0	5.4
11	248.6	4.8	11	250.5	4.2	11	249.5	4.7	11	249.7	4.8	11	249.9	6.0	11	250.3	5.2	11	251.1	5.2	11	249.7	5.0
12	248.9	4.3	12	250.2	4.3	12	251.9	4.4	12	248.4	4.8	12	249.5	6.0	12	251.1	5.2	12	249.2	5.3	12	248.6	5.2
13	250.5	4.5	13	250.2	4.4	13	251.6	4.4	13	250.1	4.7	13	251.2	5.9	13	251.7	5.2	13	249.6	5.1	13	248.8	5.3
14	249.9	4.4	14	250.5	4.1	14	250.8	4.2	14	250.3	4.7	14	250.4	5.7	14	250.0	5.3	14	249.1	5.1	14	248.1	5.4
15 f	249.7	1.7	15 f	250.0	1.6	15 f	249.8	1.6	15 f	250.6	1.7	15 f	250.6	1.6	15 f	250.1	1.6	15 f	249.6	1.6	15 f	250.3	1.6
16	248.9	4.5	16	248.5	4.4	16	251.7	4.4	16	249.4	4.9	16	251.1	5.6	16	249.1	5.0	16	250.6	5.1	16	250.1	5.1
17	249.9	4.3	17	250.4	4.0	17	249.9	4.1	17	249.6	4.8	17	249.6	6.2	17	250.6	5.4	17	250.1	5.0	17	252.0	5.4
18	251.3	4.6	18	250.6	4.5	18	249.6	4.5	18	249.7	4.7	18	250.7	5.5	18	250.6	4.8	18	250.7	4.8	18	250.3	5.0
19	247.9	4.4	19	250.8	4.2	19	251.5	4.1	19	249.9	4.7	19	249.4	5.9	19	250.3	5.2	19	251.4	5.3	19	250.8	5.6
20	250.0	4.4	20	250.6	4.2	20	249.7	4.8	20	251.9	4.5	20	250.9	5.8	20	248.6	5.4	20	251.1	5.1	20	251.1	5.1
21	249.1	4.2	21	249.4	4.2	21	250.2	4.2	21	248.9	4.7	21	251.8	5.9	21	249.8	5.4	21	249.3	5.1	21	250.2	5.5
22	249.2	4.4	22	250.1	4.2	22	250.2	4.4	22	250.2	4.7	22	251.1	5.5	22	248.3	4.9	22	249.5	4.8	22	250.2	5.1
23	248.4	4.3	23	249.5	4.1	23	251.7	4.0	23	249.9	4.6	23	249.6	6.0	23	249.1	5.3	23	249.1	5.4	23	250.5	5.3
24	251.2	4.5	24	250.1	4.2	24	251.5	4.4	24	250.6	4.7	24	250.4	5.6	24	251.6	5.0	24	249.2	5.1	24	249.8	5.1
25	250.1	4.2	25	249.8	4.1	25	249.6	4.1	25	250.4	4.8	25	250.5	5.6	25	250.9	5.2	25	248.9	5.5	25	248.8	5.3
26	249.1	4.3	26	248.8	4.2	26	249.8	4.3	26	251.0	4.8	26	251.0	5.5	26	251.9	4.9	26	249.3	4.7	26	251.5	5.1
27	251.2	4.3	27	249.8	4.1	27	251.1	4.4	27	251.0	4.5	27	249.6	5.7	27	249.6	5.4	27	250.6	5.2	27	249.3	5.6
28 f	250.2	1.7	28 f	250.8	1.5	28 f	250.7	1.7	28 f	251.5	1.8	28 f	249.5	1.6	28 f	249.8	1.7	28 f	249.8	1.8	28 f	251.0	1.7
29	249.5	4.5	29	250.1	4.0	29	250.5	4.3	29	250.0	4.5	29	249.3	5.4	29	250.4	5.0	29	250.5	5.1	29	250.0	5.0
30	249.1	4.3	30	249.4	4.0	30	250.5	4.1	30	248.6	4.5	30	249.2	5.9	30	250.7	5.3	30	248.7	5.6	30	250.1	5.5
31	249.5	4.5	31	249.4	4.3	31	248.7	4.3	31	250.9	4.7	31	250.3	5.6	31	252.0	4.8	31	250.6	5.2	31	250.7	5.0
32	250.9	4.2	32	249.5	4.1	32	251.4	4.2	32	250.0	4.1	32	249.6	5.9	32	249.0	5.5	32	250.5	5.4	32	248.2	5.5
33	250.4	4.5	33	248.2	4.1	33	249.4	4.4	33	250.6	4.7	33	250.1	5.4	33	251.3	4.7	33	250.3	5.0	33	248.8	4.8
34	249.3	4.2	34	248.8	4.0	34	250.5	4.1	34	250.6	4.5	34	249.8	6.0	34	250.3	5.5	34	250.1	5.3	34	251.1	5.7
35	249.0	4.3	35	249.2	4.5	35	250.8	4.3	35	248.7	4.5	35	249.5	5.3	35	249.9	5.2	35	250.2	5.1	35	250.2	5.0
36	249.7	4.4	36	249.5	3.9	36	250.6	4.2	36	251.6	4.6	36	250.2	6.0	36	249.5	5.3	36	250.7	5.4	36	250.2	5.5
37	248.6	4.3	37	250.1	4.1	37	251.4	4.3	37	249.6	4.5	37	249.8	5.4	37	250.0	4.8	37	249.2	5.0	37	250.7	4.8
38	249.4	4.1	38	251.1	4.1	38	251.2	4.1	38	250.0	4.6	38	251.1	5.8	38	249.5	5.4	38	250.0	5.3	38	250.8	5.5
39	251.0	4.5	39	249.5	4.7	39	250.2	4.4	39	249.7	4.9	39	249.5	6.6	39	251.0	5.9	39	251.4	5.9	39	251.4	6.0
40	251.3	4.3	40	250.4	4.0	40	249.5	4.2	40	249.3	4.8	40	249.6	6.1	40	250.5	5.6	40	249.2	5.7	40	249.9	5.8
41	248.8	4.1	41	250.2	3.9	41	250.9	3.7	41	248.1	4.0	41	250.2	5.2	41	250.5	4.5	41	251.4	4.9	41	250.4	5.2
42	251.8	4.1	42	250.3	3.8	42	250.8	4.0	42	250.4	4.0	42	250.1	4.9	42	249.8	4.7	42	249.5	4.6	42	249.5	5.0
43	249.1	3.8	43	248.5	3.8	43	251.3	3.8	43	252.2	3.8	43	251.5	4.9	43	250.8	4.5	43	251.2	4.8	43	249.1	5.0
44	251.8	4.1	44	250.7	3.8	44	249.7	4.1	44	249.3	4.0	44	249.6	4.7	44	249.3	4.5	44	249.9	4.6	44	250.9	5.0
45	251.3	3.9	45	249.4	3.7	45	249.9	4.0	45	251.2	4.0	45	250.9	4.8	45	249.8	4.4	45	250.0	4.8	45	249.7	4.8
46	250.4	4.1	46	251.4	4.1	46	251.3	3.9	46	250.7	4.3	46	251.5	4.8	46	250.6	4.4	46	250.3	4.7	46	250.7	4.9
47	250.2	3.9	47	250.4	3.8	47	249.7	4.0	47	251.9	3.9	47	249.2	4.9	47	249.5	4.6	47	251.3	4.7	47	250.3	5.1
48	248.8	4.3	48	248.5	4.2	48	250.5	4.1	48	251.6	4.3	48	251.7	4.9	48	251.3	4.5	48	250.6	4.3	48	250.7	4.9
49	250.9	4.0	49	250.7	3.9	49	251.4	4.1	49	247.9	4.2	49	249.7	4.7	49	249.4	4.3	49	250.1	4.9	49	249.5	4.9
50	250.4	4.1	50	251.9	3.8	50	250.8	4.0	50	251.4	4.4	50	249.7	4.8	50	251.7	4.6	50	250.5	5.1	50	251.8	4.8
51	248.9	4.1	51	249.5	3.7	51	250.9	4.3	51	249.3	4.0	51	250.2	4.7	51	250.5	4.5	51	250.0	4.4	51	250.7	5.0
52	250.7	4.2	52	251.2	3.9	52	249.8	4.2	52	250.1	4.2	52	250.5	4.8	52	251.0	4.3	52	250.1	4.4	52	250.5	4.8
53 f	250.1	1.4	53 f	250.4	1.6	53 f	251.3	1.6	53 f	250.7	1.5	53 f	250.2	1.6	53 f	250.9	1.5	53 f	250.4	1.5	53 f	249.8	1.5
54	249.8	4.0	54	249.2	3.9	54	249.1	3.9	54	250.1	4.0	54	250.1	4.6	54	251.0	4.6	54	249.8	4.5	54	249.3	5.0
55	250.2	4.3	55	250.1	4.2	55	249.7	4.2	55	250.6	4.2	55	249.3	4.7	55	249.8	4.3	55	248.9	4.5	55	248.8	4.7
56	250.0	3.9	56	249.4	3.8	56	250.6	3.9	56	250.6	3.9	56	251.5	4.6	56	250.7	4.2	56	251.8	4.4	56	249.8	5.0
57	249.7	4.3	57	249.5	4.1	57	250.5	4.4	57	250.6	4.1	57	249.3	5.0	57	250.8	4.7	57	250.1	4.7	57	251.0	4.8
58	249.9	4.0	58	249.7	3.9	58	250.2	4.0	58	250.3	4.0</												