



Signal Digitization in IceCube

Ryo Nagai (Chiba University) On behalf of the IceCube Collaboration

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Water Cherenkov Workshop (Online)

IceCube / -Upgrade / -Gen2



Constraints on in-situ digitization



IceCube DOM Digitization

DOM: Digital Optical Module



- A 10" PMT facing downwards
- 5160 DOMs are installed in the ice
- 99% are still working for >10 years

Front-end DAQ board (Mainboard) ADC ATWD PMT signal ADC ATI Amplitiers 'PMT ADC

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IceCube DOM Digitization



- ATWD is a fast, custom-made ASIC, which digitizes with 128 sampling bins with 300 MSPS (~426 ns window) after receiving the triggers
- Since ATWD is busy during the digitization (takes 29 μs), there are 2 ATWDs on a mainboard and switch if one is busy, to reduce the dead time
- To expand the dynamic range, 3 different amplifier outputs into ATWD
- In parallel, PMT ADC is a bit slow, but longer waveform can be digitized

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DOM Problem for Upgrade era

Already 20 years passed since the development...

- ATWD system limits the time window & (would) have large dead-time — we don't want to miss rare events / waveforms
- Many components (especially FPGA) are already obsolete — we can't produce the same board any longer

Also, technology has been much grown...



Family of Digital Optical Modules



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Upgrade Digitization-1: Simple Scheme



- Difference between them: <u>**# PMTs**</u> (channels)
- Analog front-end circuit & FPGA function are identical
 - The board shape, layout, etc. are different
- \rightarrow Will show the D-Egg case only

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Upgrade Digitization-1: Simple Scheme



- Two 8" HQE PMTs
- Horizontally slimmed design to reduce the drilling cost...
 (The narrower hole, the faster/cheaper drilling)
- ~300 production completed in 2021

Front-end DAQ board (Mainboard)



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Upgrade Digitization-1: Simple Scheme



- Very simple scheme makes it possible **to digitize without dead-time**
 - Thanks to the off-the-shelf extremely low power ADC (ADS4149)
- FPGA (Cyclone-V) stores the data to the flash memory only when the trigger signal is published
- Operation power consumption is only 4.5 W (for 2 channels)

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Upgrade Digitization-1: Signal Readout



- Waveform readout : standard operation for D-Egg DAQ
 - Time window changeable up to $\sim 30 \ \mu s$
 - But slow readout (~10 Hz)
- Only getting integrated charge & time information
 - So fast readout (>kHz)
 - Use it to check SPE distribution shape



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Upgrade Digitization-2: multi-PMT



- 24 3" PMTs
- Photon incident direction information
- ~400 production ongoing but some parts are in short supply now...

Front-end DAQ board (Mainboard)



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Upgrade Digitization-2: multi-PMT



- Similar to the simple scheme, but instead of high frequency ADC, divide 2 signal lines — can keep enough time resolution (~1 ns)
 - 120 MHz waveform ADC
 - 960 MHz timing discriminator
- Operation power consumption is ~10 W

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Upgrade Digitization-2: multi-PMT

Low charge

- Both waveform / charge-time info readouts are supported (same as PDOM/D-Egg)
 - Main software is identical to PDOM/D-Egg's
- Clear PMT signal is observed
 - Enough S/N to the SPE
 - Linear response seen for < 50 PE signal
- Charge-time info readout contributes to obtaining clear SPE distribution in a short time



[1] PoS ICRC2021 (2021) 1070

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High charge



-Base (wuBase) ontend nuous Digitizing wuBase + Chris Wendt dy8 **FPGA** Pulse Shaping 60 MSPS 12-bit ADC LTC2142 Waveform anode wuBase shapes dictated by spaces ming edge between PMTs nm **FPGA** MCU s mDOM micro-Base) 150 mW/each Threshold STM32L5 s => Wide dynamic range LOM (16) **Jynode signals** are x16_1and captured in a lower consumption FPGA <u>base +</u> v-lever processing a level waveform data unicator ables, route MCU • Another possibility: build ASIC (would save power & cost) wubase for LOM-16 polar position shown. STM32H7 equatorial z Water Where & and occupation linersions different 2022 16

Gen2 Digitization: First test results

- Clear SPE has been observed with the FWHM of ~50 ns
 - Baseline noise ~1 ADC count...
 extremely good!
- Anode+dynode readout contribute to expanding the dynamic range...
 - Even if anode side saturated, dynode signal can recover the whole range of the pulse

Circuit design looks no problem



[1] PoS ICRC2021 (2021) 1062

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Summary

- IceCube detectors are in deep ice, so the in-ice digitization is necessary
- IceCube is now using several in-ice digitization systems with carefully managing the critical limitations:
 - cost, power consumption, ...
- Thanks to the technology growing, Upgrade modules can digitize without dead-time
 - D-Egg: Simple scheme, the final testing stage
 - mDOM: Complicated, the production stage
- Gen2 module (LOM) is under development, but its main concept shares with the Upgrade modules and so far looks working well

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