TOSHIKO YUASA LABORATORY

Summary II of TYL Instrumentation and Computing projects

D_RD_20, D_RD_23, D_RD_18, HEP_15

FRANCE-JAPAN PARTICLE PHYSICS

LAL KEK Tsukuba HEP

2020 Joint workshop of FKPPL and TYL/FJPPL

Continuation of the project [D_RD_20]:

New challenge for Inner Pixel Tracker construction

Koji Nakamura (KEK)

Yoichi Ikegami, Koji Nakamura*1 (KEK)

Kazuhiko. Hara, Hideki Okawa (Tsukuba)

Dimitris Varouchas, Tobbias Fitschen (PhD student),

Anastasia Kotsokechagia (PhD student), Lydia Fayard,

Mark Escalier, Abdenour Lounis, Pierr Petroff, Reisaburo Tanaka*2(LAL)

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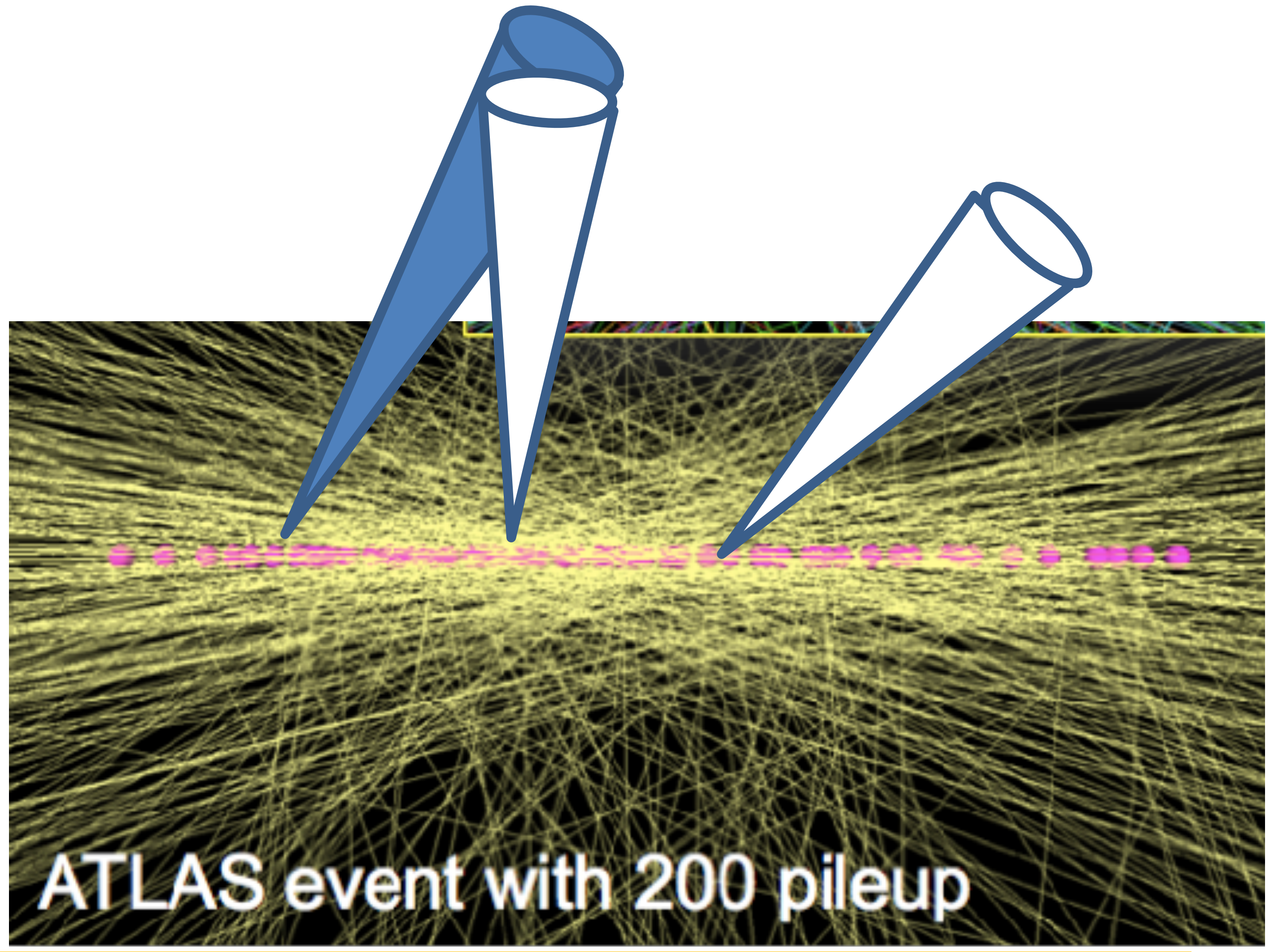
Framework : ATLAS Upgrade for HL-LHC

- **High Luminosity LHC (HL-LHC)**
  - Start around 2026- with new crab cavity in the interaction region.
  - Target : $\sqrt{s}$**=14TeV L=5-7x10^{34}cm^{-2}s^{-1}** $\int Ldt$**=3000-4000fb^{-1}**
  - Physics program focus on the precise measurements of the Higgs couplings (e.g. Y_τ, Y_b and λ_{HHH}) and BSM searches.
- **Tracking detector is key element**
  - To keep B/τ-tagging performance up to μ=200 pileup in an event.
  - Need to launch innovative solution for detectors, mechanics, efficient triggering and advanced analysis technics.

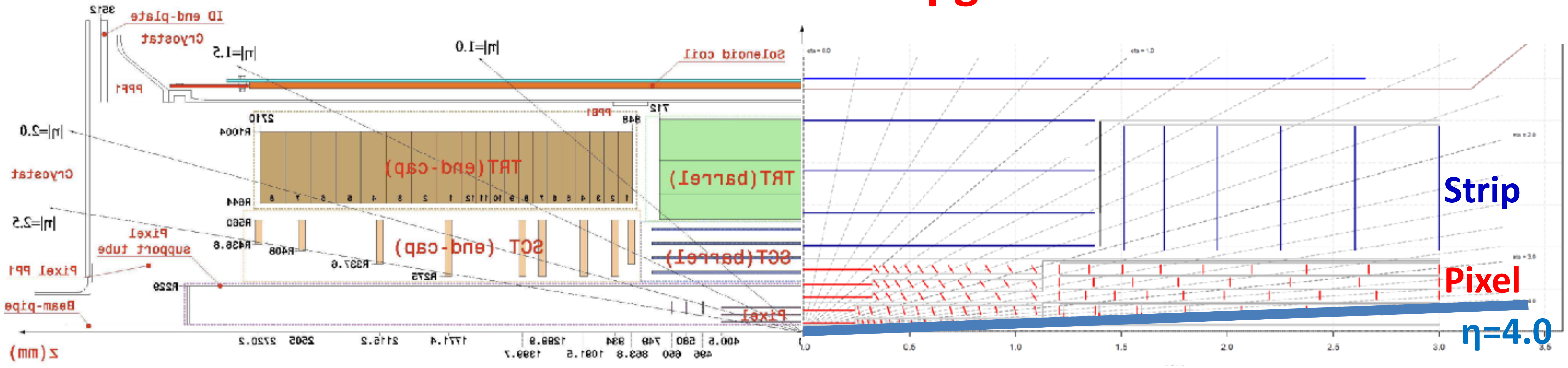
ATLAS plans a full replacement of Inner Tracker for the Upgrade

- All silicon tracker (Pixel & Microstrip)
- ***Requirements for Pixel detector***
  - Pixel Size : 50um x 50um (or 25um x 100um)
  - Radiation @ outer layer : 3x10^{15}n$_{eq}$/cm^2
  - Thickness : 100 or 150um
  - Low noise (<100e) → 600e stable threshold
  - High Readout Rate : 5.2Gbps (or 4x1.28Gbps)

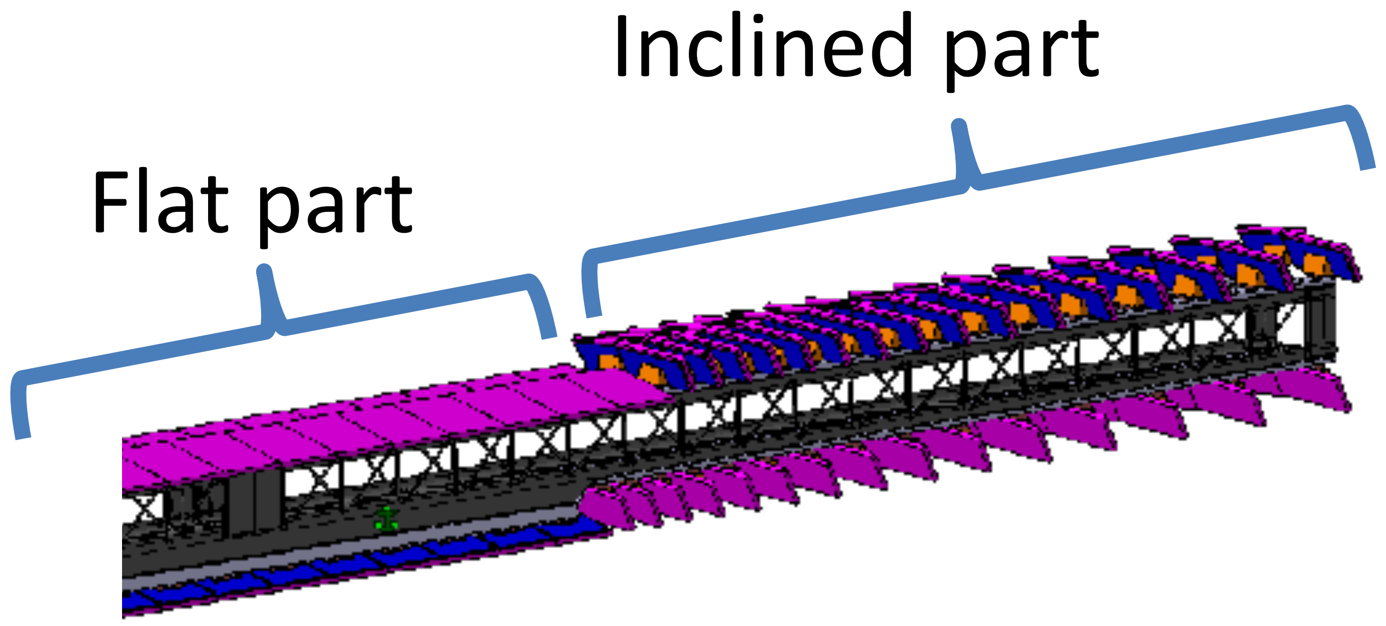


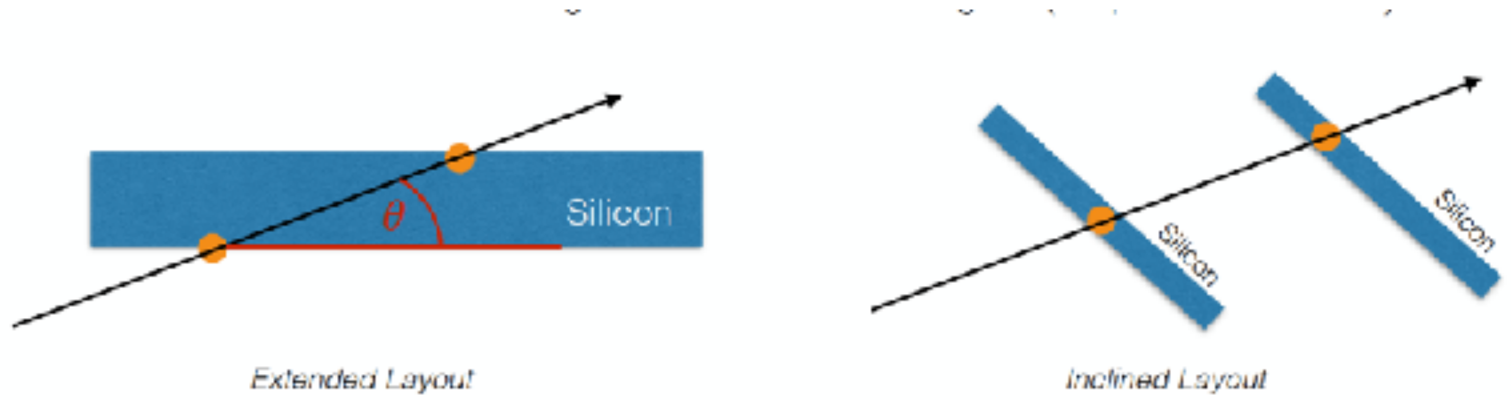
ATLAS inner tracker(ITK) project for HL-LHC

Current ATLAS Detector **ITK upgrade detector**



- Larger coverage area
  - Pixel : 2.7m² ➔ **8.2m²**
  - Strip : 34m² ➔ **165m2**
- Higher Forward coverage
  - $\eta<2.5$ ➔ **$\eta<4.0$**
- Mechanics : slanted
  - Reduce material
  - Higher tracking resolution.



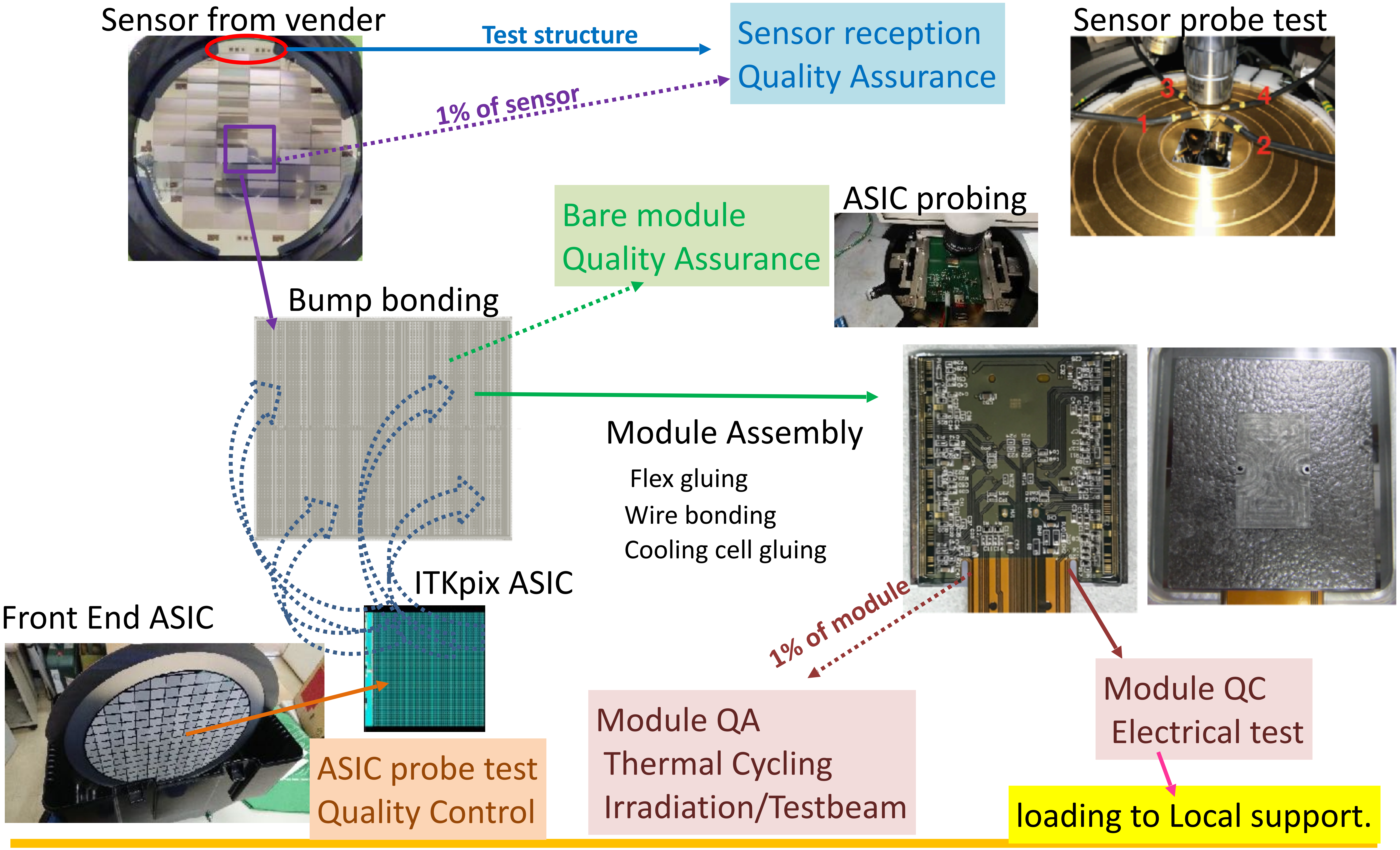


D_RD_20 program proposal

- Building production modules based on the developed pixel detector.
  - ***2019-2020 : preparation of production***
  - ***2021-2024 : production of the modules***
- Constructing ITK pixel detectors is extremely challenging
  - **>10000 quad planar pixel modules to be produced. About 20% of modules are build by us.**
  - **Finalize the design and construction method.**
  - **Development of Quality Control and Quality Assurance.**

- **Mainly we ask funding for exchange people between FR-JP**
  - **Share experience/common development**

QC/QA flow for module production

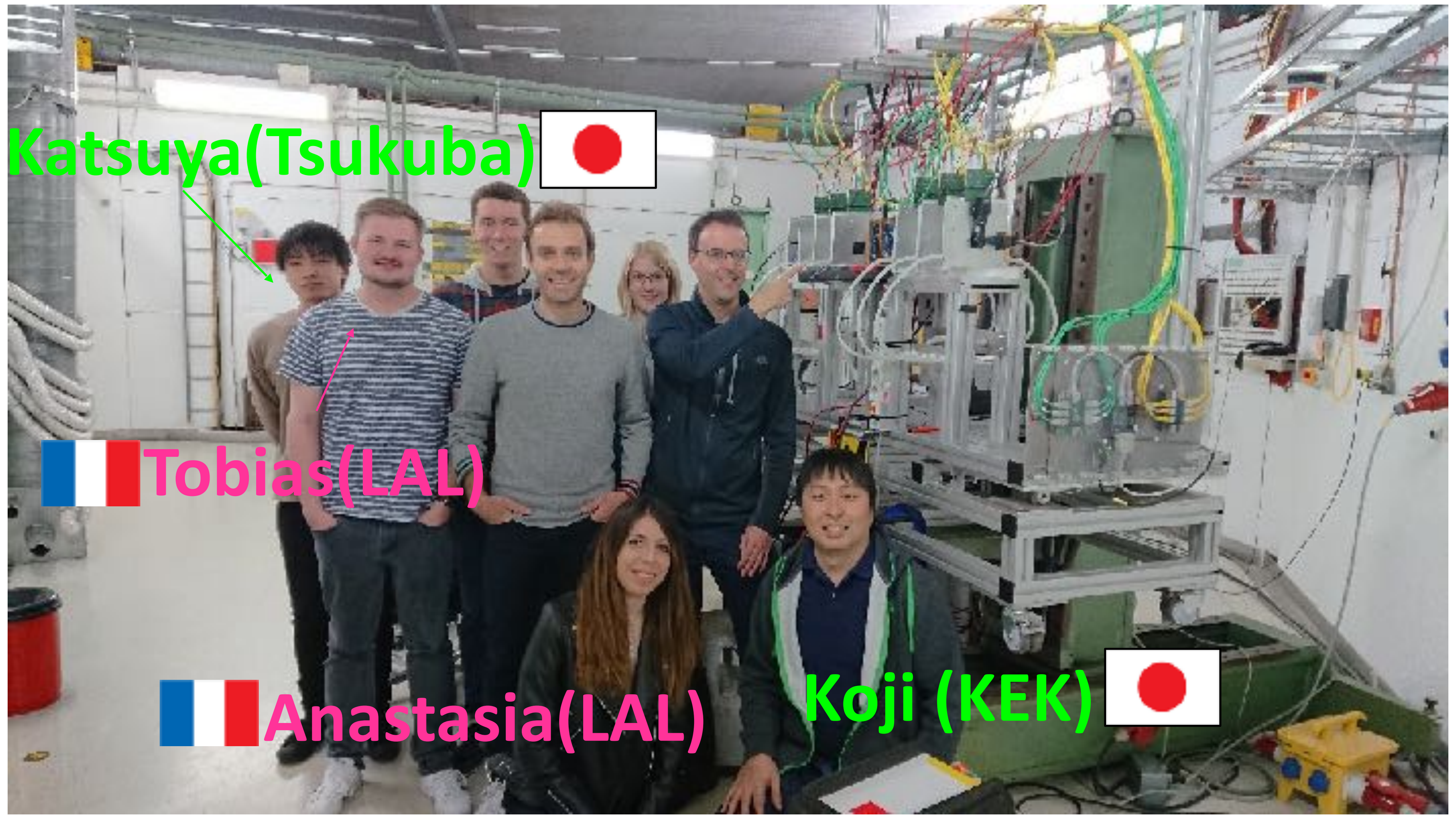


Activity in 2019

- Finalizing design of the n+-in-p type Pixel Module towards Production of ITk upgrade.
- Final vendor qualification process (Market survey)
- Tested characteristics of sensor.
  - Check of Module performance by testbeam.
  - Irradiation to test radiation tolerance.

- Three testbeams at DESY
  - 22nd -29th July, 2019
  - 23rd Sep – 7th Oct, 2019
  - 25th Nov – 9th Dec, 2019

- Operation of these testbeams by RD_20 group as major contribution.



Plans for 2020 -> 2022

- Finalize vendor qualification (Market survey)
  - Planned a testbeam as soon as COVID-19 situation get better.
  - Finalize all performance measurements by ITk pixel sensor Final design review (FDR) : scheduled in Summer.
- Started Pixel Sensor Pre-production (10% of whole production)
  - The site qualification for pre-production measurement almost completed.
  - Finalize all performance measurements of pre-production sensor by ITk pixel sensor Production Readiness Review (PRR) : scheduled in Summer.
- Module Pre-production will start in the later this year
  - Define and setup quality control(QC) and quality assurance(QA) procedure for the pre-production.
  - Finalizing the QA/QC by the Final Design Review (FDR) in June 2022.
- Exchange students and staff to accelerate the effort described above
  - Collaborative work for testbeam operation and analysis →France
  - Irradiation campaign in Tohoku-University Japan France→Japan
  - Share the test setup for the QC/QA during production France<-> Japan

View of 2022

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  - The site qualification for pre-production measurement almost completed.
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IJClab KEK Tsukuba HEP

2022 Joint workshop of FKPPL and TYL/FJPPL

Continuation of the project [D_RD_23]:

Development of Precision Timing Silicon Detector (LGAD) for Future Collider Experiments

KEK: Koji Nakamura[*1]
Tsukuba Univ.: Kazuhiko Hara, Tasuki Ueda (Master student), Sayuka Kita (Master student)
IJClab: Reisaburo Tanaka[*2], Abdenour Lounis, Khwaira Yahya (PhD student), Maurice Cohen-Solal

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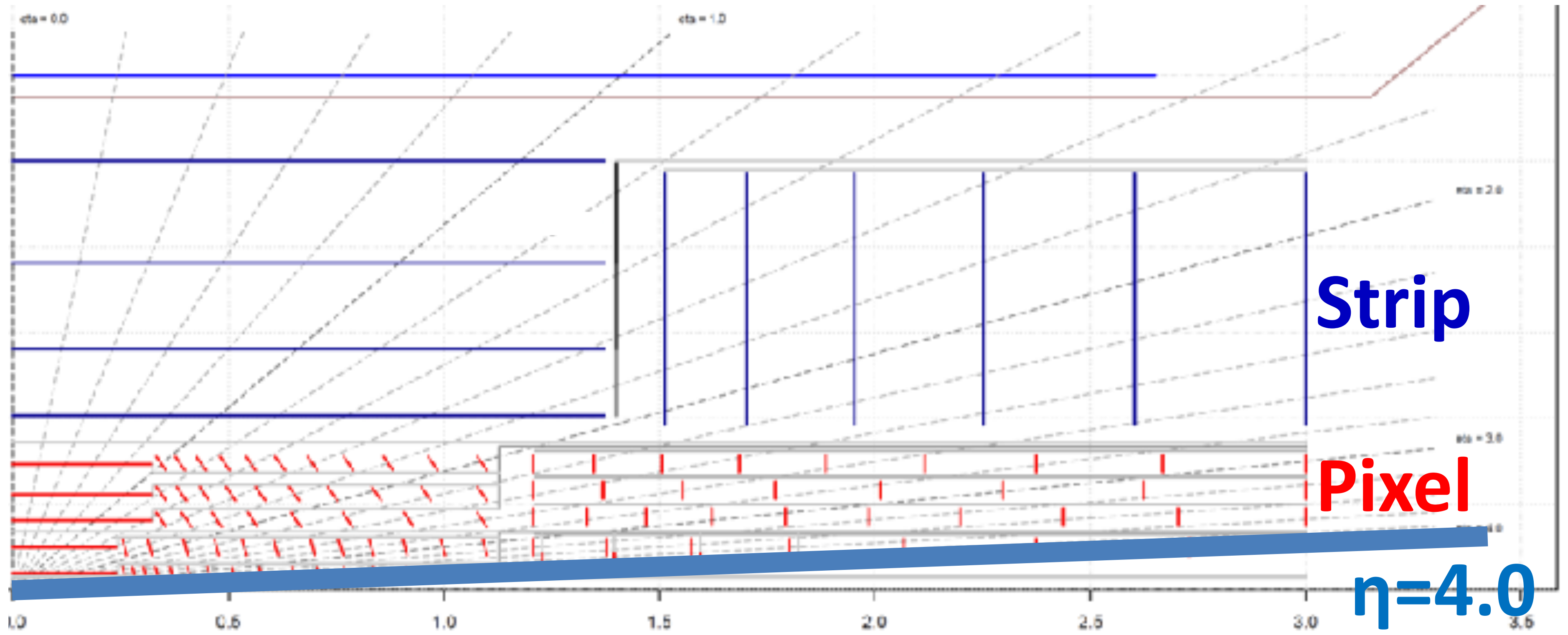
What we need for Hadron Collider(+ILC)?

- High Luminosity LHC detector

ITK upgrade detector



- Strip : ~75.5um pitch
- Pixel : 50um x 50um pitch

Is this granularity possible?

ILC

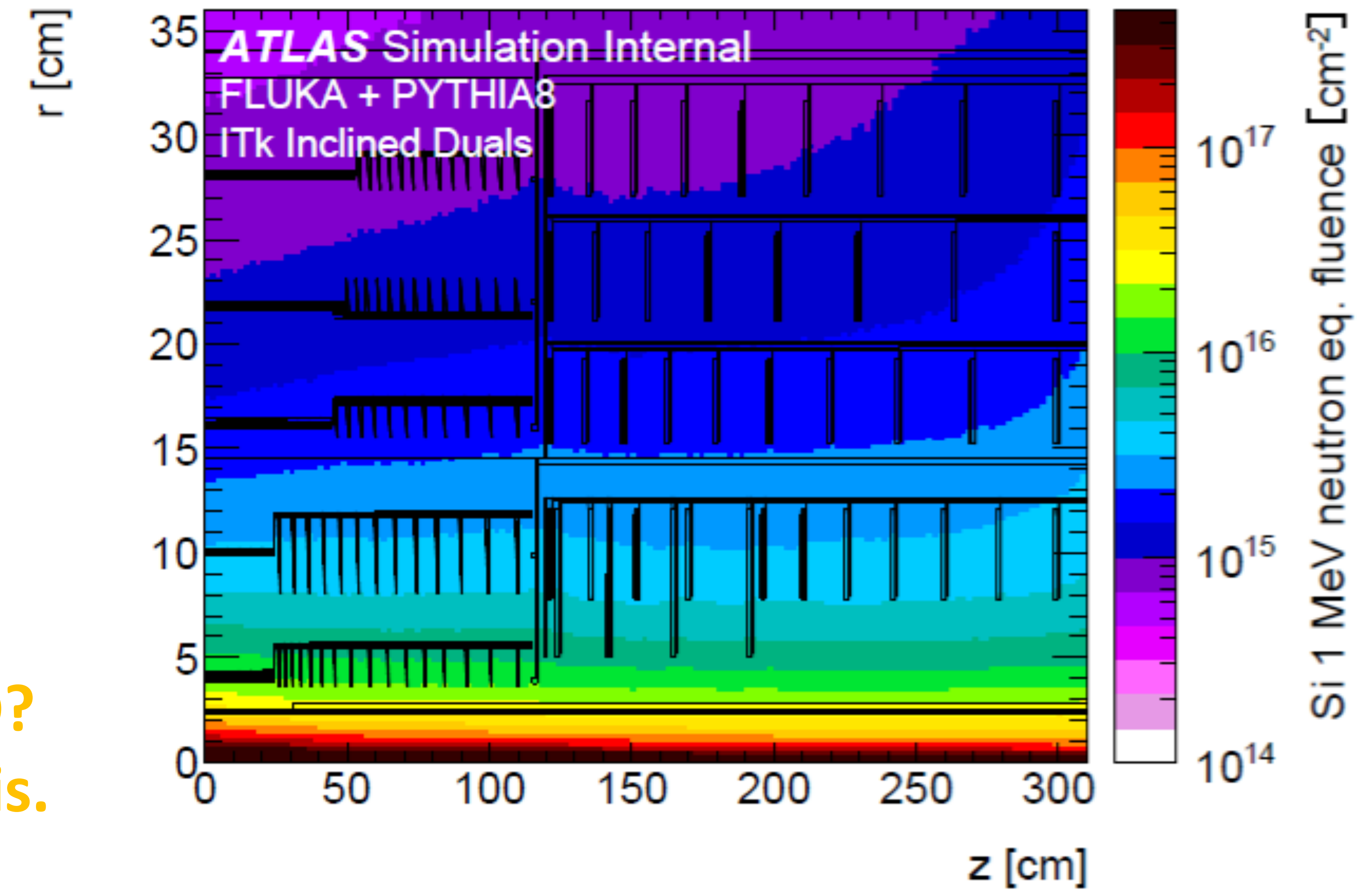
Outer tracker layers of ILC are also possibly LGAD?

LGAD for CAL should work with current LGAD as is.

Better timing resolution helps for PID?

- Expected radiation level for $4000fb^{-1}$
  - Non Ionizing Energy Loss (NIEL):
    - 3^{rd} layer: $2.8 \times 10^{15}\ n_{eq}/cm^2$ 1^{st} layer : $2.6 \times 10^{16} neq/cm^2$
  - Total Ionizing Dose (TID) :
    - 3^{rd} layer : 1.6MGy 1^{st} layer : 19.8MGy

Could replace detector at the middle of runs.



Survive upto $1e16neq/cm^2$?

If we have LGAD sensor with these granularity and radiation tolerance, all tracker can be replaced by LGAD!

Future Semi-conductor Tracking Detectors

- **Further finer pitch pixel detector → Limited by front end Electronics (min : $50\times50um^2$)**
  - In addition to spatial resolution, **Timing resolution helps!**

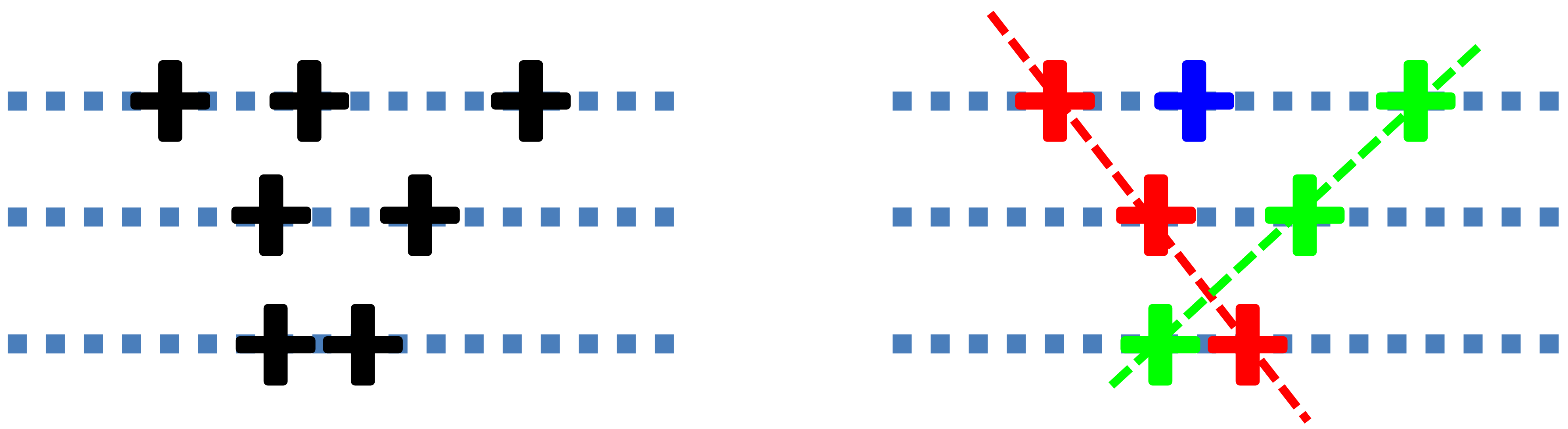
  →New generation of Tracking detector should have timing information for all hits!

- **Tentative Requirement**
  - **30ps timing resolution**
  - **~o(10)um spatial resolution (Pixel type).**
  - **(hadron collider) ~o(10^{16})n_{eq}/cm^2 radiation tolerance**

4D tracking!

Detector Hit

Tracking

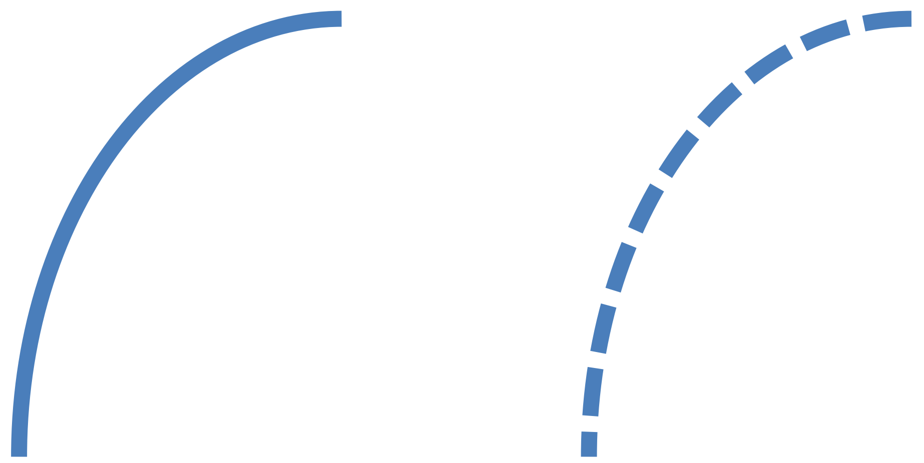


Solve pileup hits in an event

Particle identification

β = 1

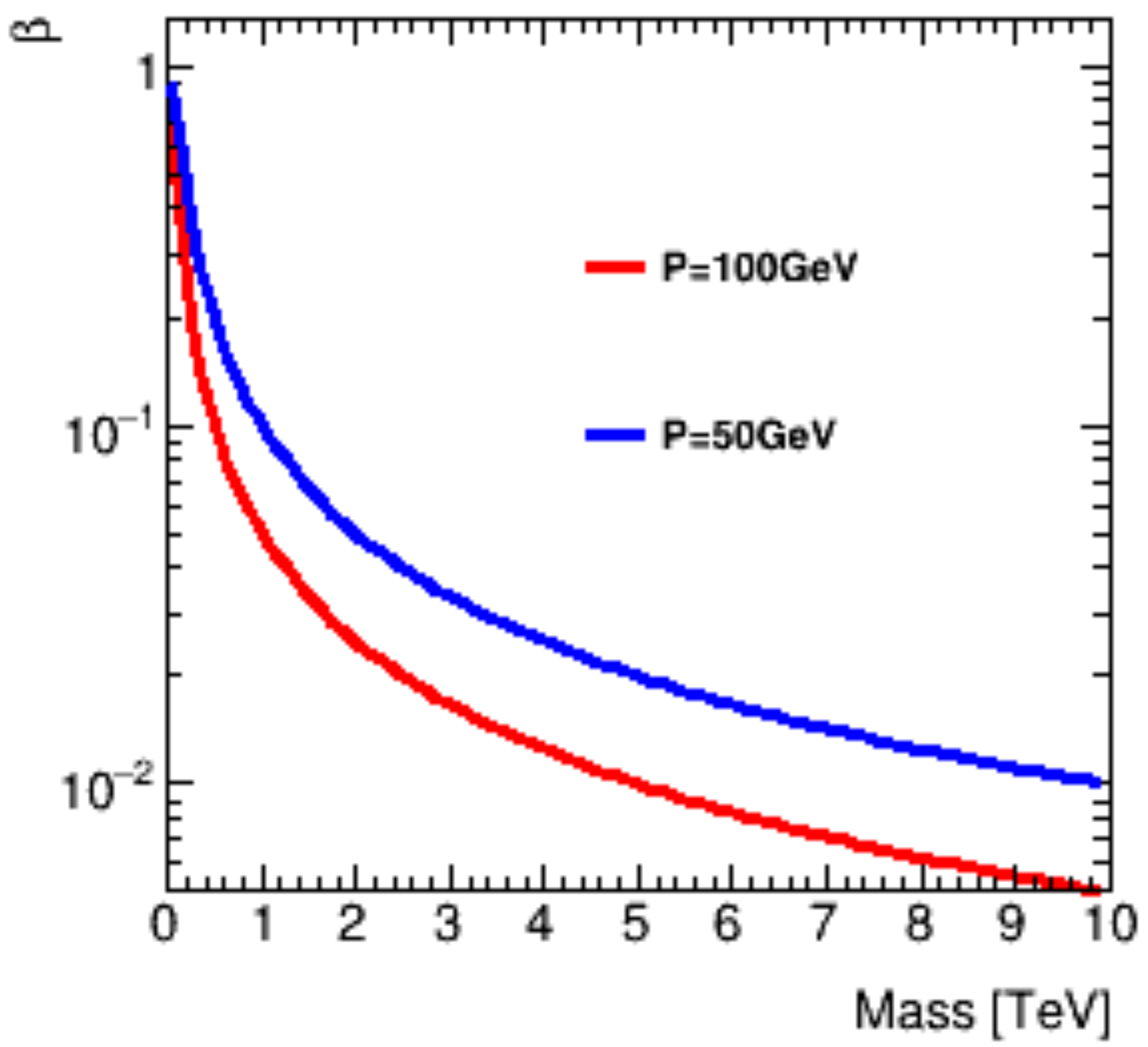
β = 0.95



150ps difference at R=1m

K+ π+ separation

Mass spectrum for new particle

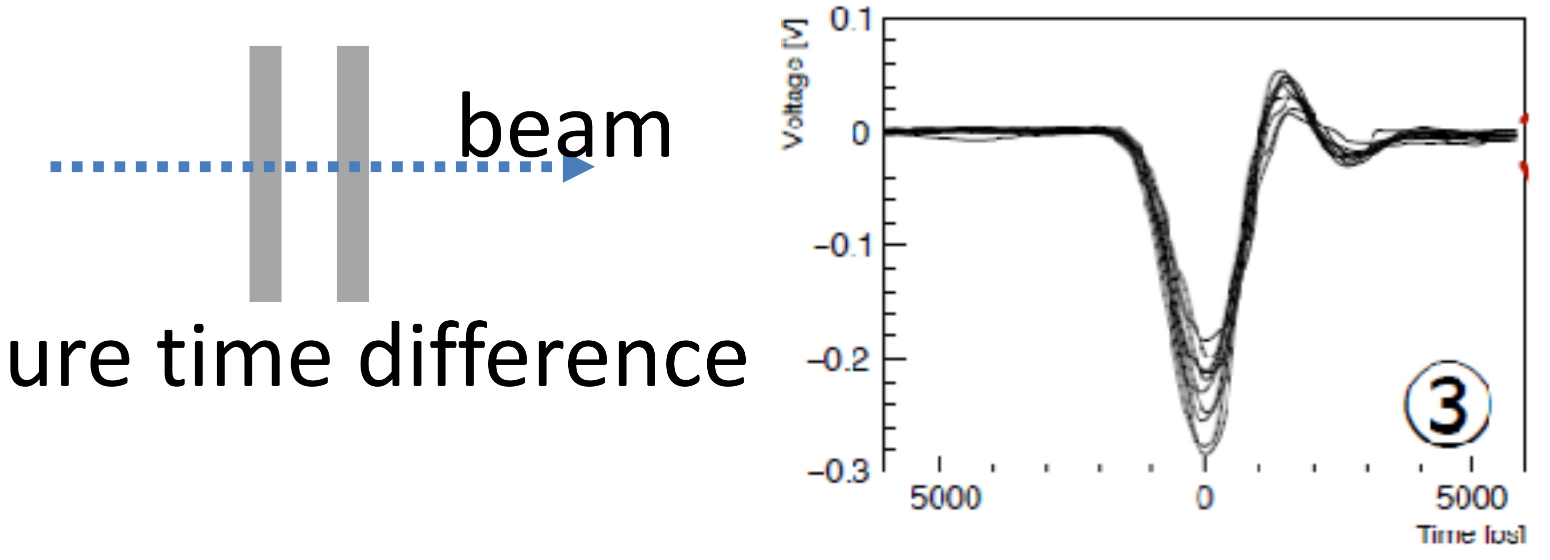


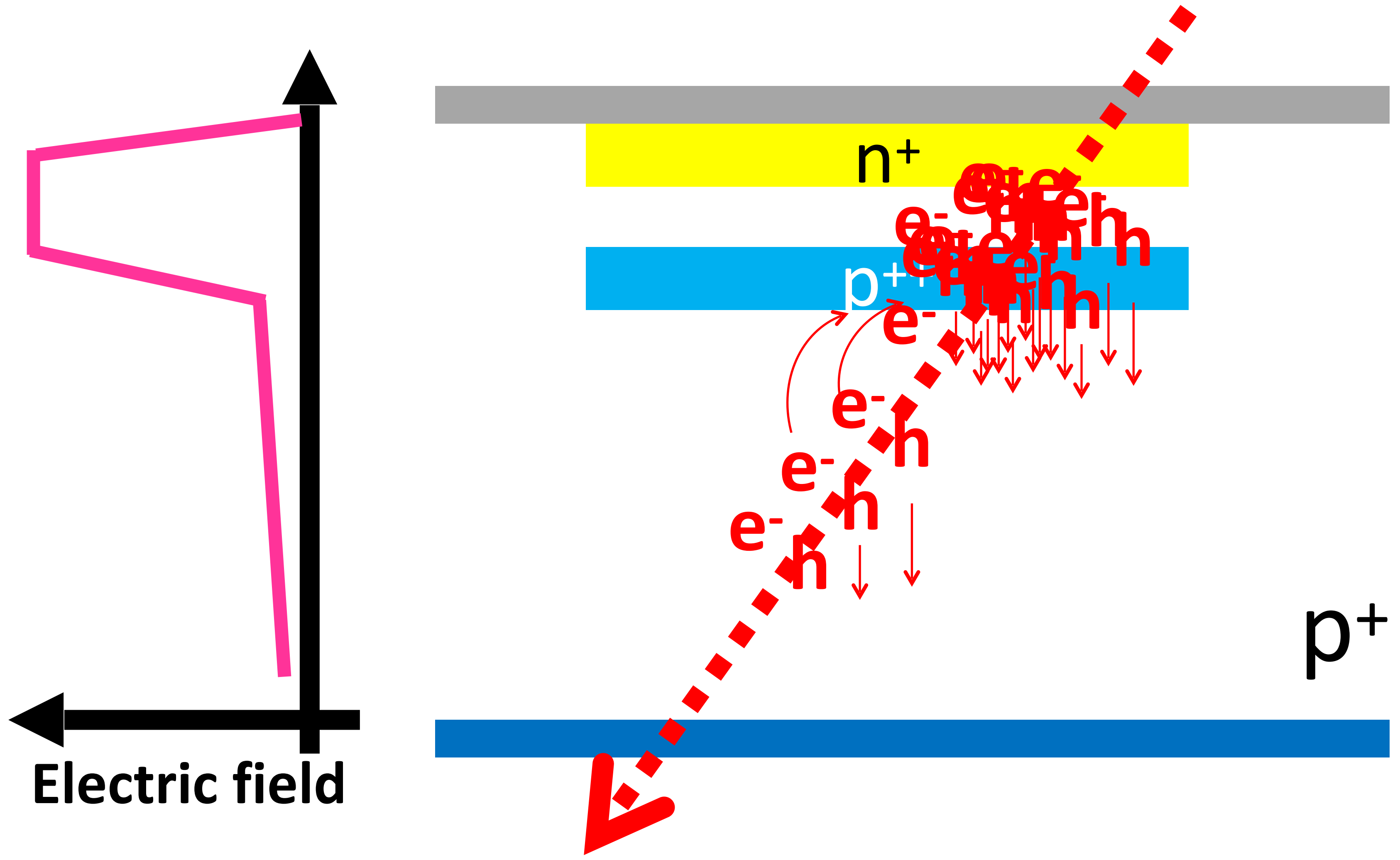
β measurement to obtain mass

e.g. Mass measurement for Long lived chargino

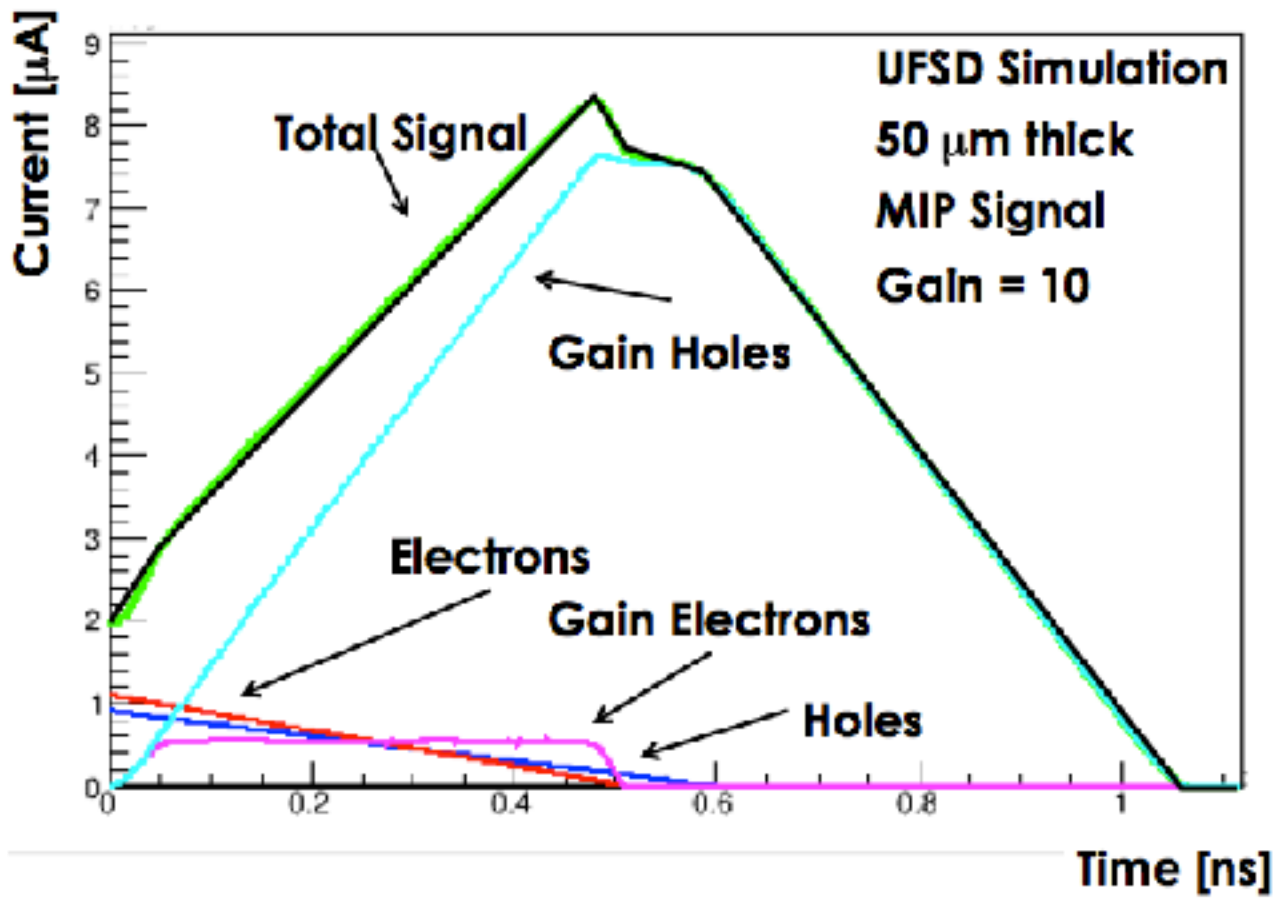
Low Gain Avalanche Diode (LGAD)

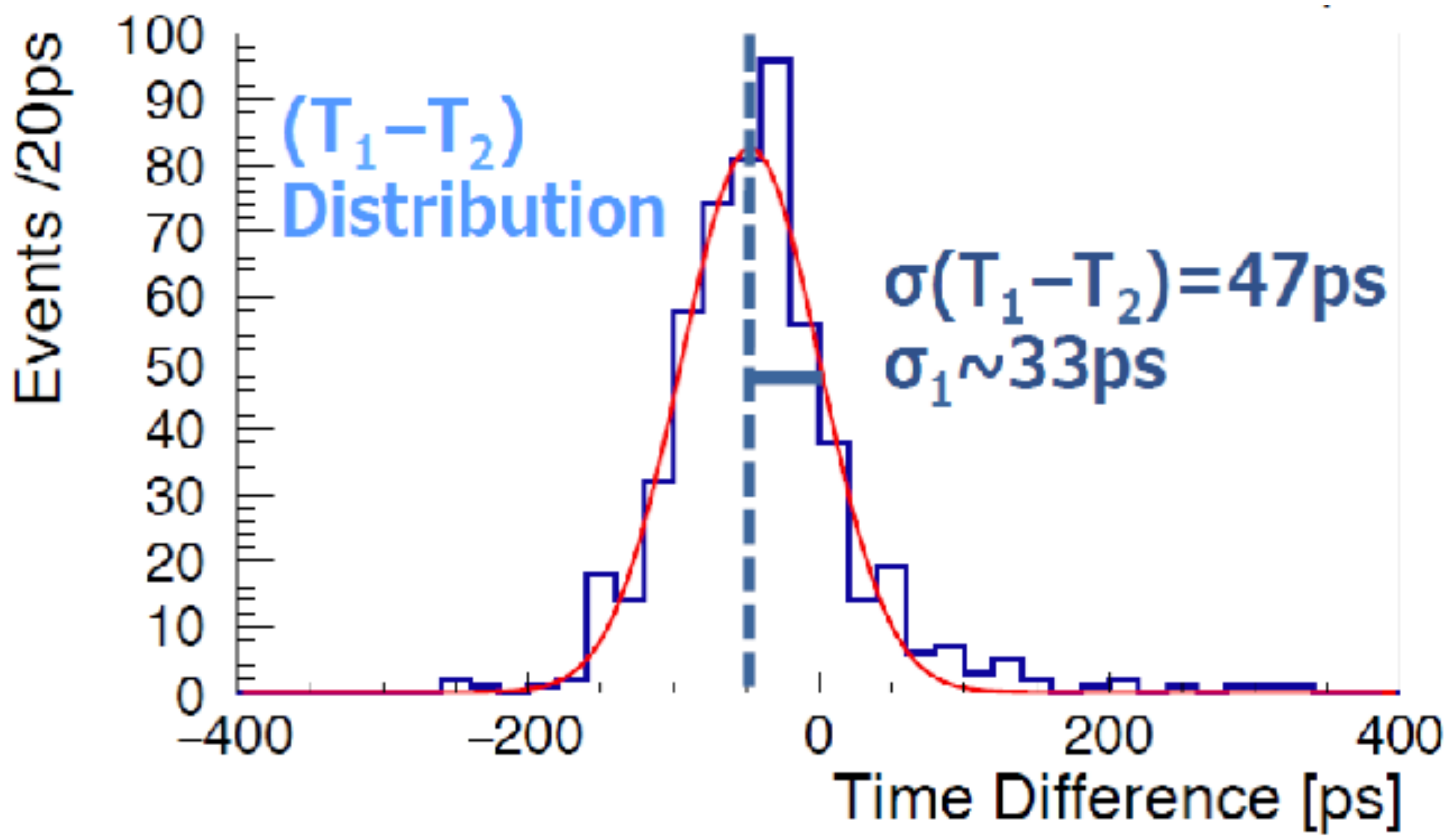
- Low gain Avalanche Diode (LGAD)
  - General n^+-in-p type sensor with p^+ gain layer under n^+ implant to make higher Electric Field → Good timing resolution.
  - **30ps timing resolution achieved already in 2015.**
  - Next development
    - **Finer electrode separation for spatial resolution**
    - **Radiation tolerance**





Signal drivers : **Gain Holes**



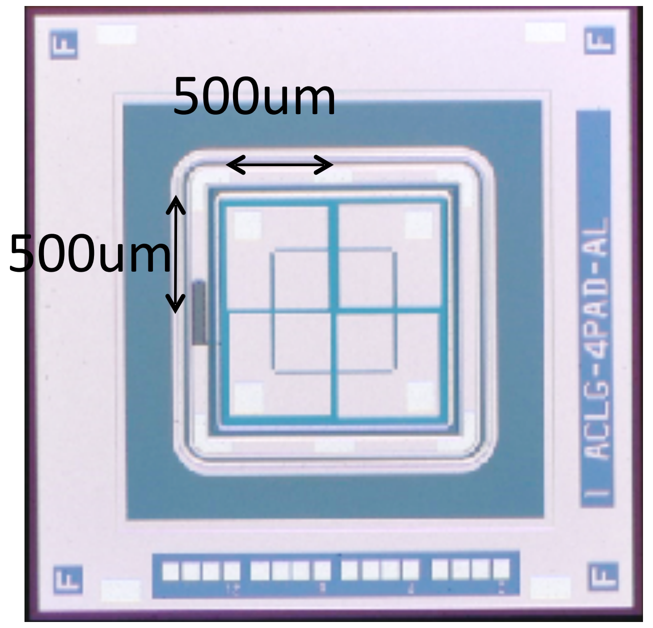


HPK LGAD development

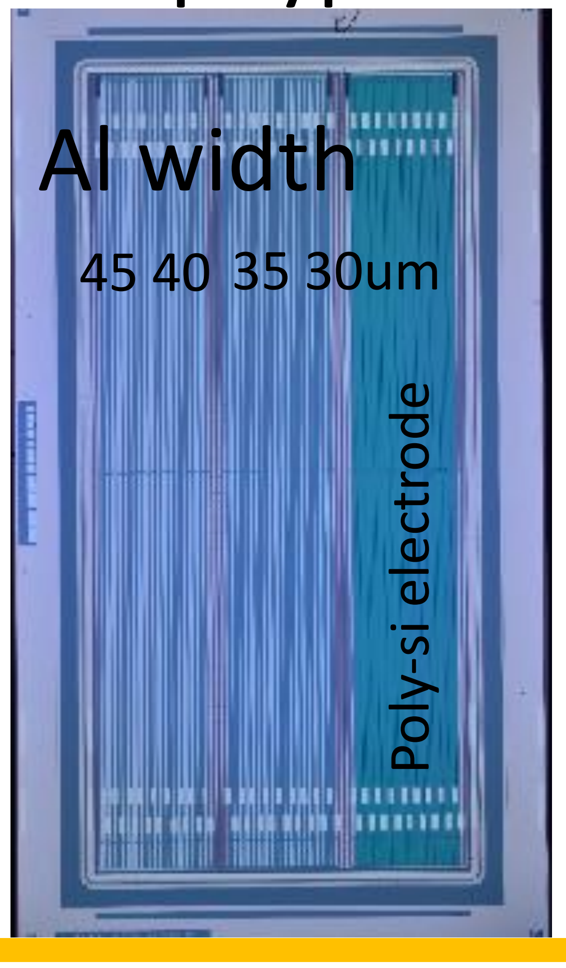
- JFY2015-JFY2018 DC-LGAD
  - **We contributed only first prototype.** HGTD took over.
- JFY2019, JFY2020 AC-LGAD production
  - Vary n+ and p+ dope (A-E, 1-3)
  - Vary thickness of SiO_2 (capacitance : C_b=1.5xC_a)
- Electrode type
  - Pad type: 500um sq. 4pad/sensor
  - **Strip type : 80um pitch**
  - Pixel type : 50um sq. 14x14 electrode

First goal

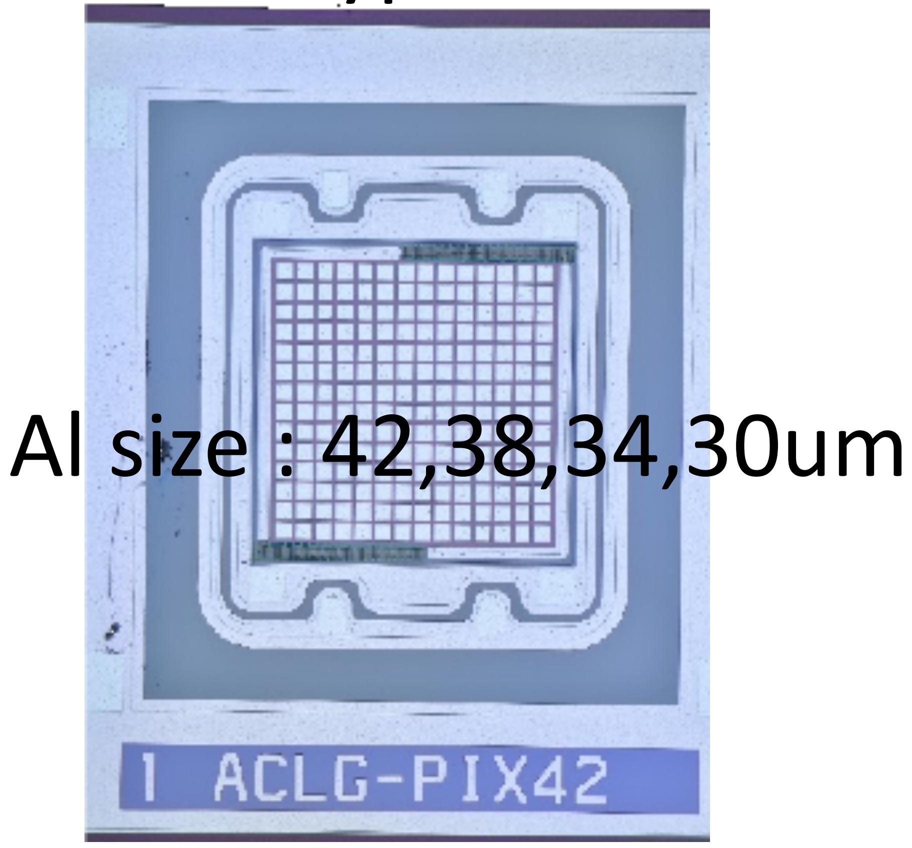
Pad type

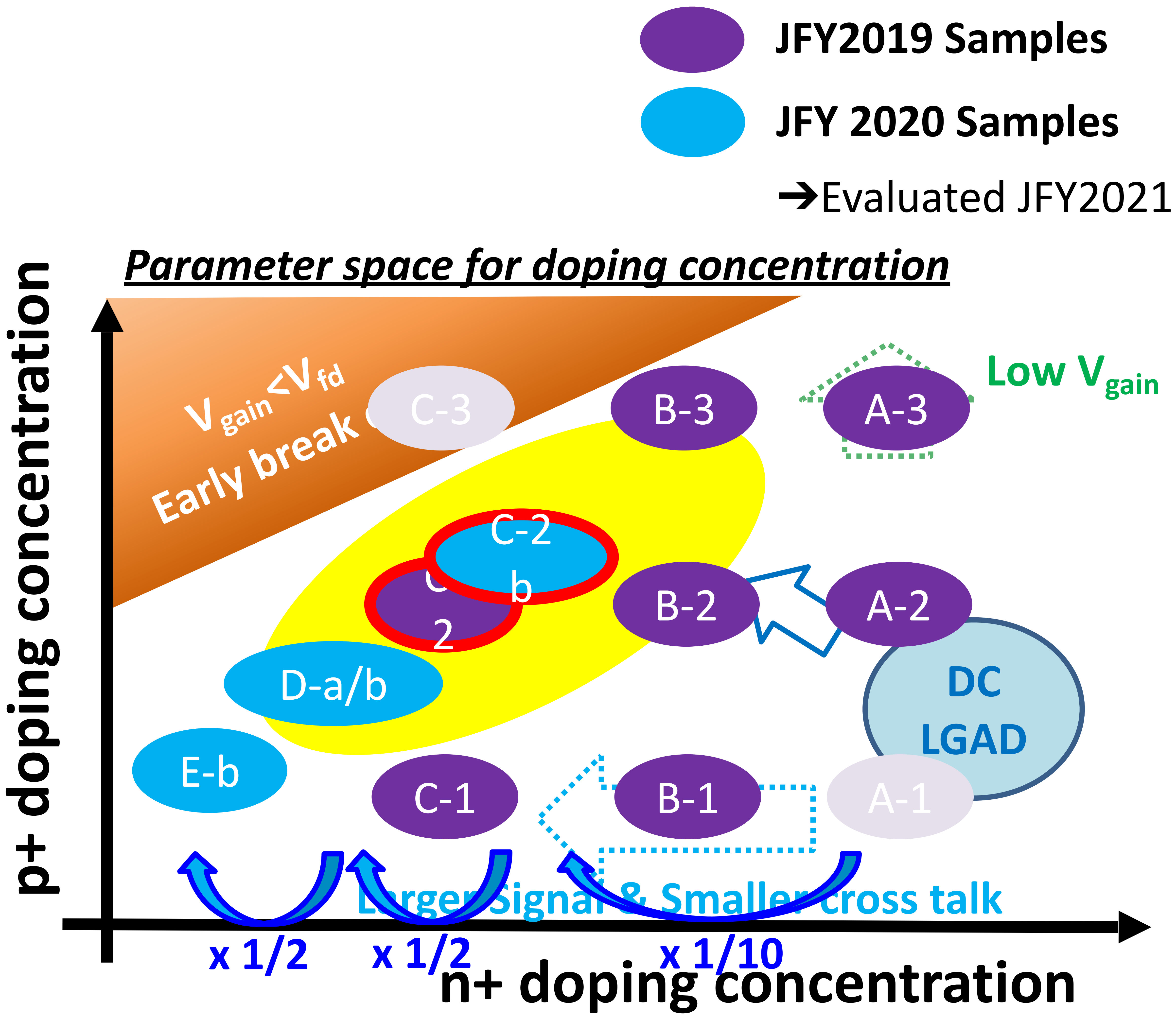


Strip type



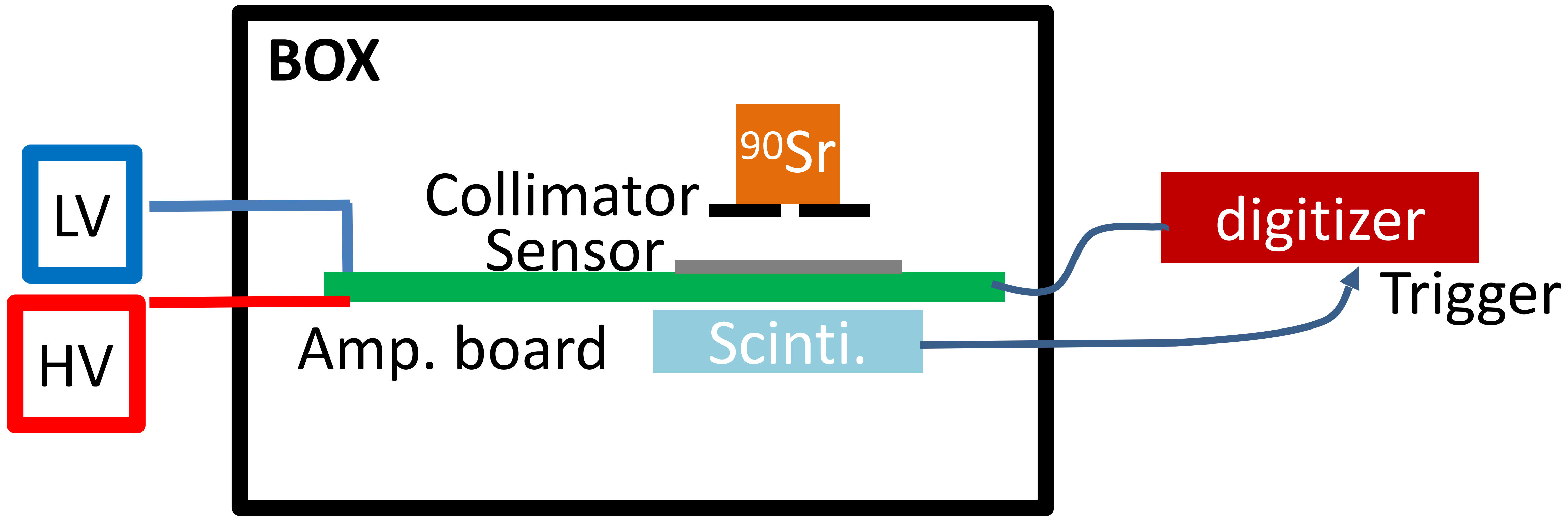
Pixel type



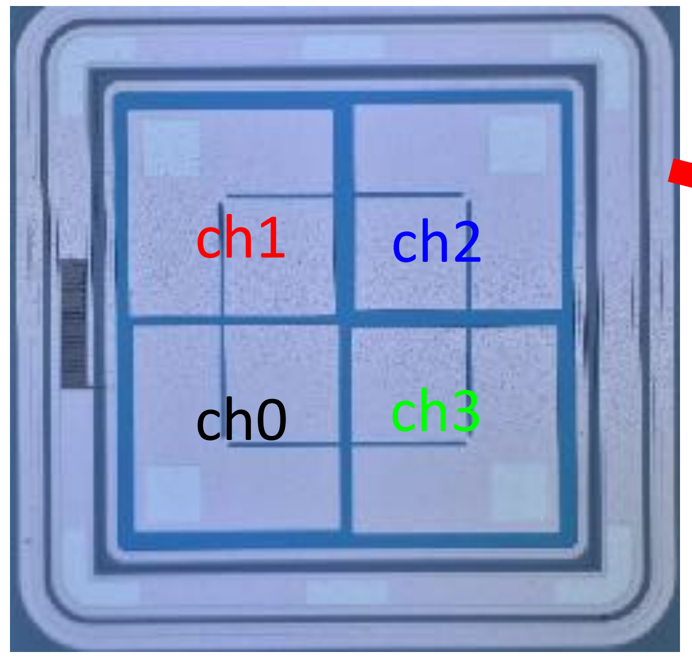


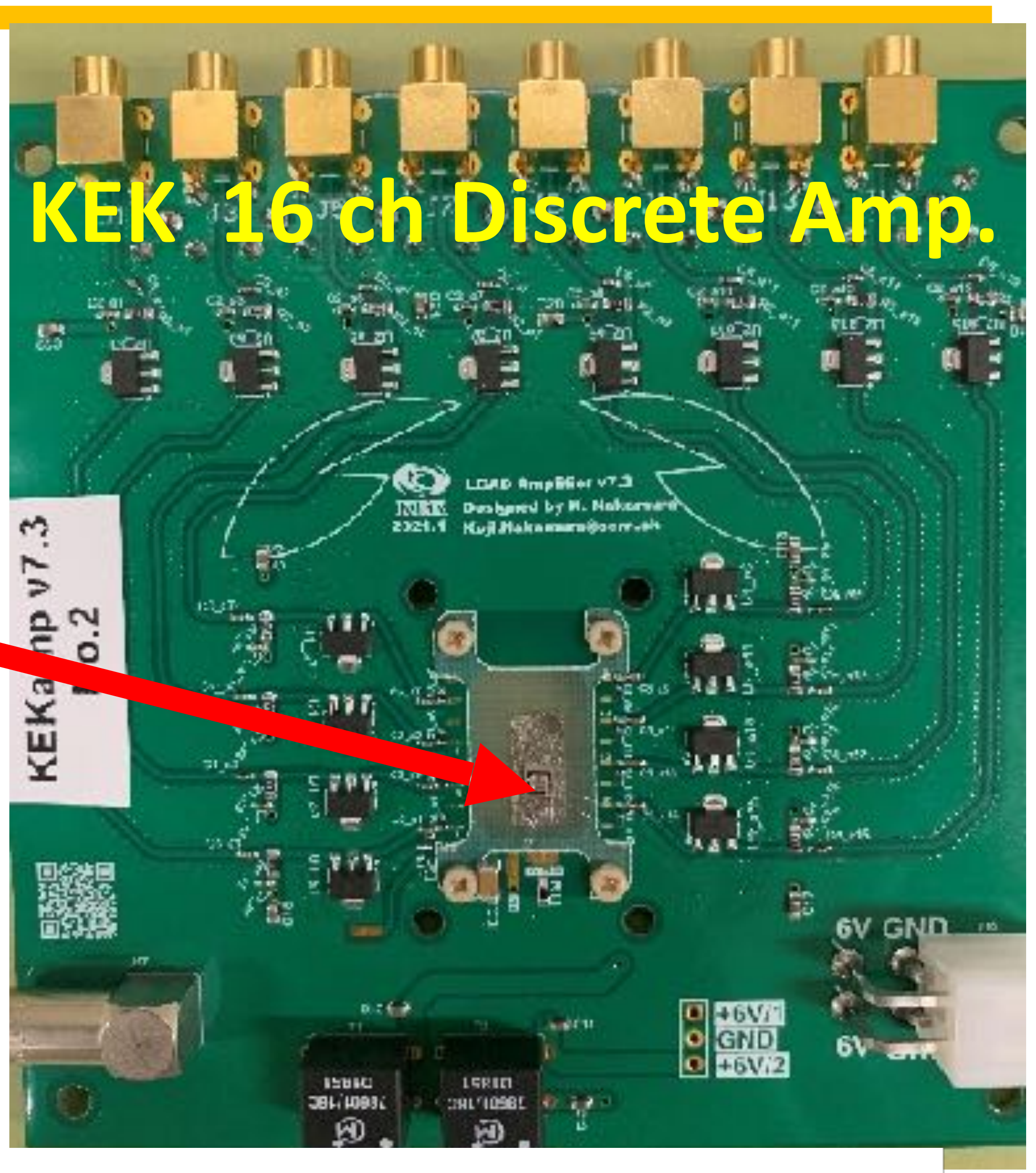
Measurement setup and signal observation

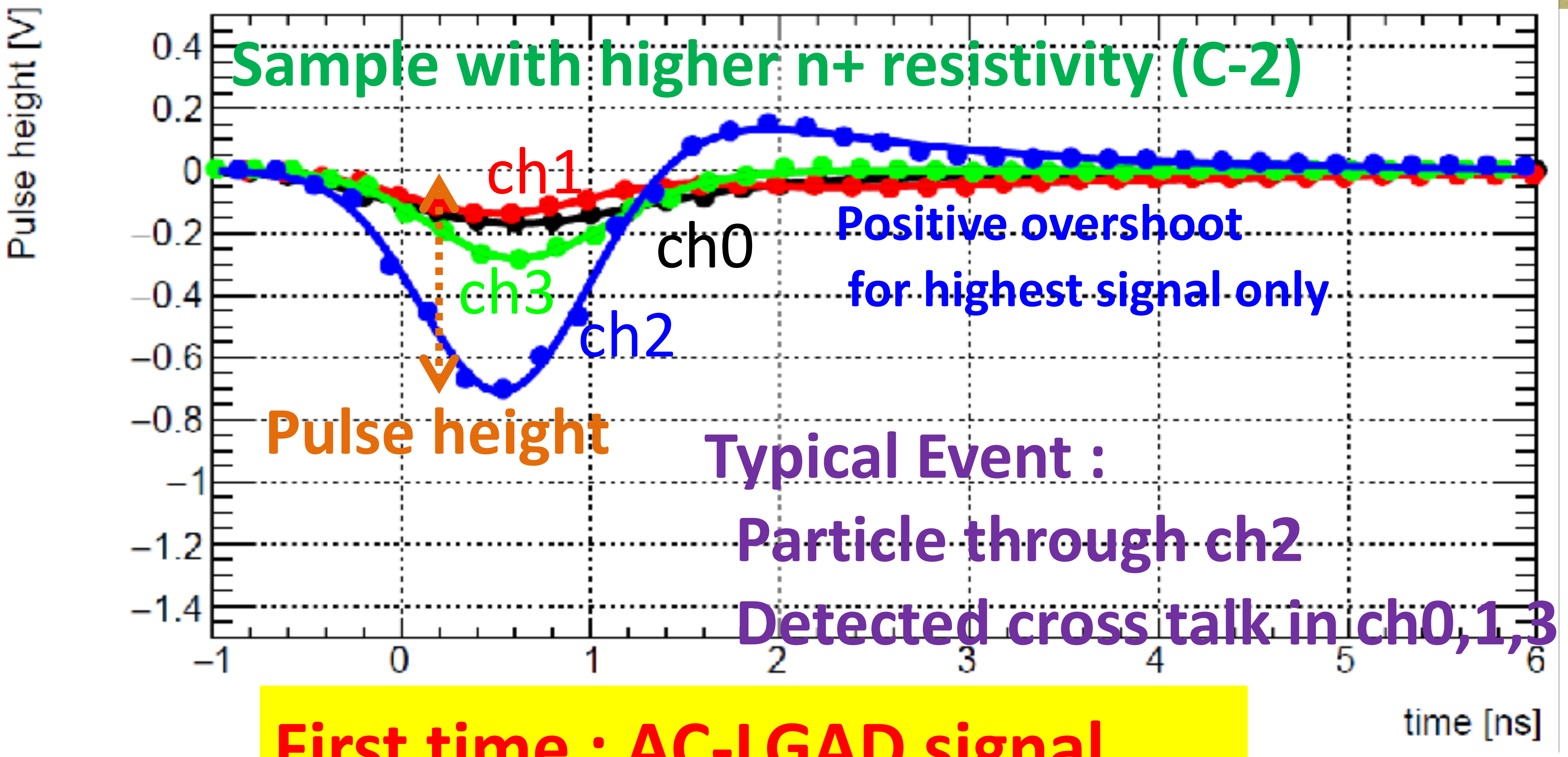
- Lab setup
  - Designed high speed amplifier board.
- Signal recorded by CAEN DT5742 digitizer or LeCroy WR8208HD scope
  - ^{90}Sr β lay source
  - Triggered by Scintillator (MPPC readout)



Pad Sensor

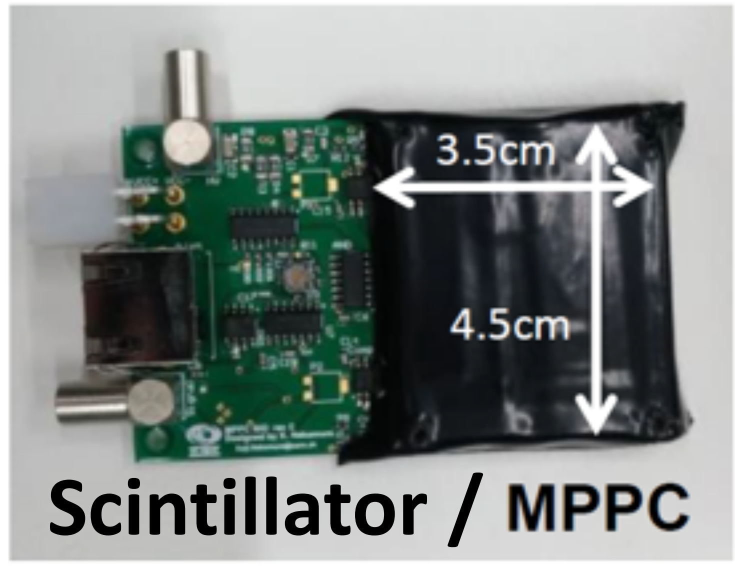






LeCroy WR8208HD scope
12bit, 10GSa/s, 2GHz
8 channel

CAEN DT5742
Desktop Digitizer
5GS/s 10bit
12bit ADC 2V full range



First time : AC-LGAD signal observed with small crosstalk

D_RD_23 LGAD: Plan in 2022

1. ASIC readout -> contacting Omega collaboration and HGTD group for ALTIROC
2. TCAD simulation on signal dependence of the sensor geometry and the doping concentration of the sensor fabrication (IJClab)
3. Prototyping new LGAD sensor with various parameters. Received new set of sensor in April and will test them. (Japan)
4. Move the design to the large size prototype based on the outcome of the optimal and finer special resolution. (Japan)
5. Large prototype can be bonded to the ASIC produced by Omega.

Reference:

[1] Koji Nakamura, Sayuka Kita, Tatsuki Ueda, Kazuhiko Hara, and Hisanori Suzuki, "First Prototype of Finely Segmented HPK AC-LGAD Detectors", JPS Conf. Proc. 34, 010016 (2021) [9 pages], Proceedings of the 29th International Workshop on Vertex Detectors (VERTEX2020)

Toward the technology choice for the TPC of the ILD detector (D_RD_18)

KEK-JAPAN

CEA - Saclay

- The feasibility of a TPC for the LC was demonstrated in D_RD_2 project
- D_RD_9 project addressed the main design issues through the construction of the Large Prototype (LP) of the TPC
- **D_RD_18 project started in 2018 and focused on**
  - measurement of momentum and dE/dx resolution of the Large Prototype
  - mitigation of ExB effects at design level (field distortions)
  - design optimization of the GEM-like gating device
  - **2-phase CO2 cooling !! 2022 highlight**
  - simulation of the effect of the resistive anode layer for MM
  - GEM gain uniformity and minimisation of the GEM discharge rate

French Group

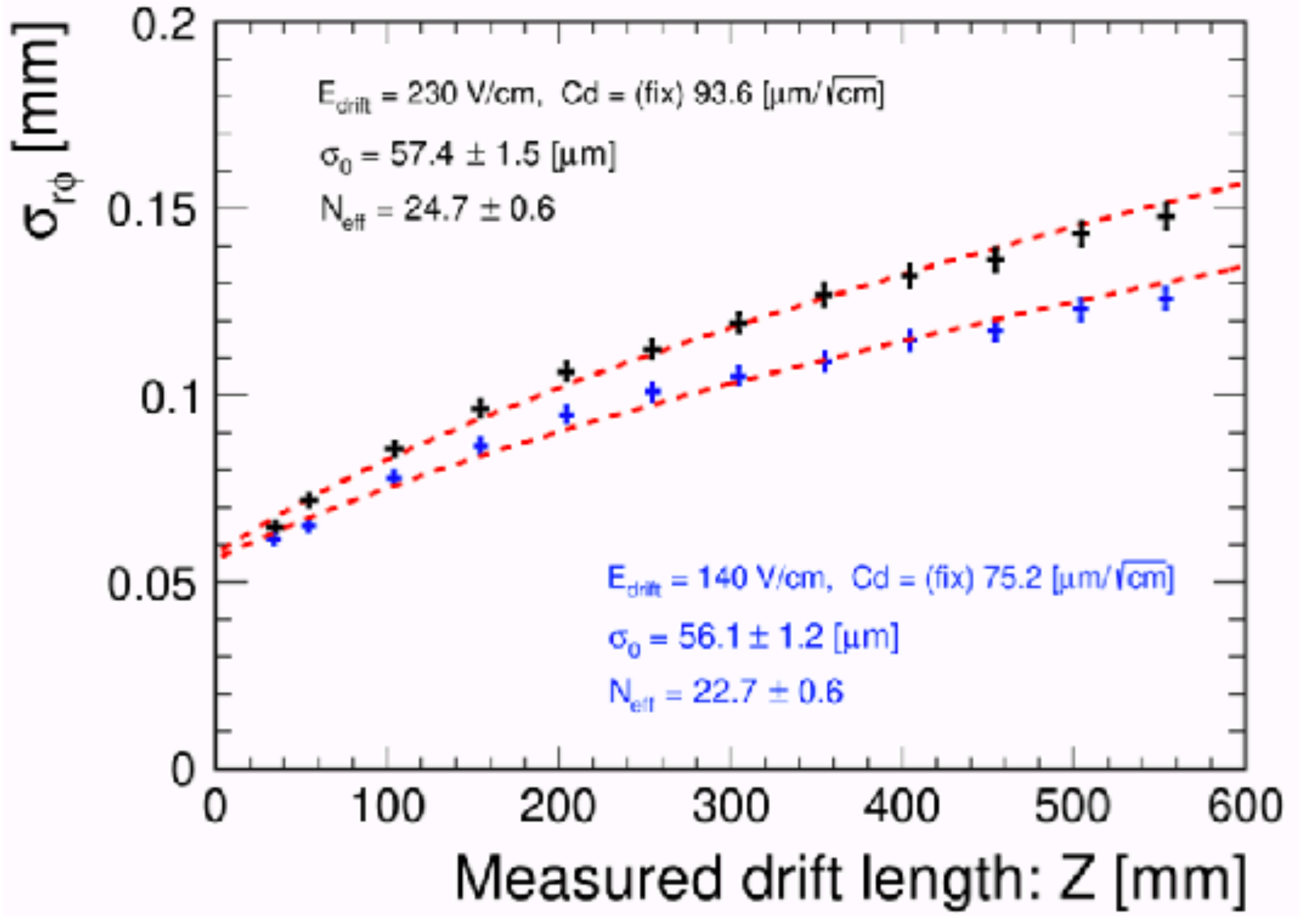
S. Ganjour	IRFU/CEA
P. Colas	IRFU/CEA
D. Attie	IRFU/CEA
I. Giomataris	IRFU/CEA
M. Titov	IRFU/CEA
B. Tuchming	IRFU/CEA

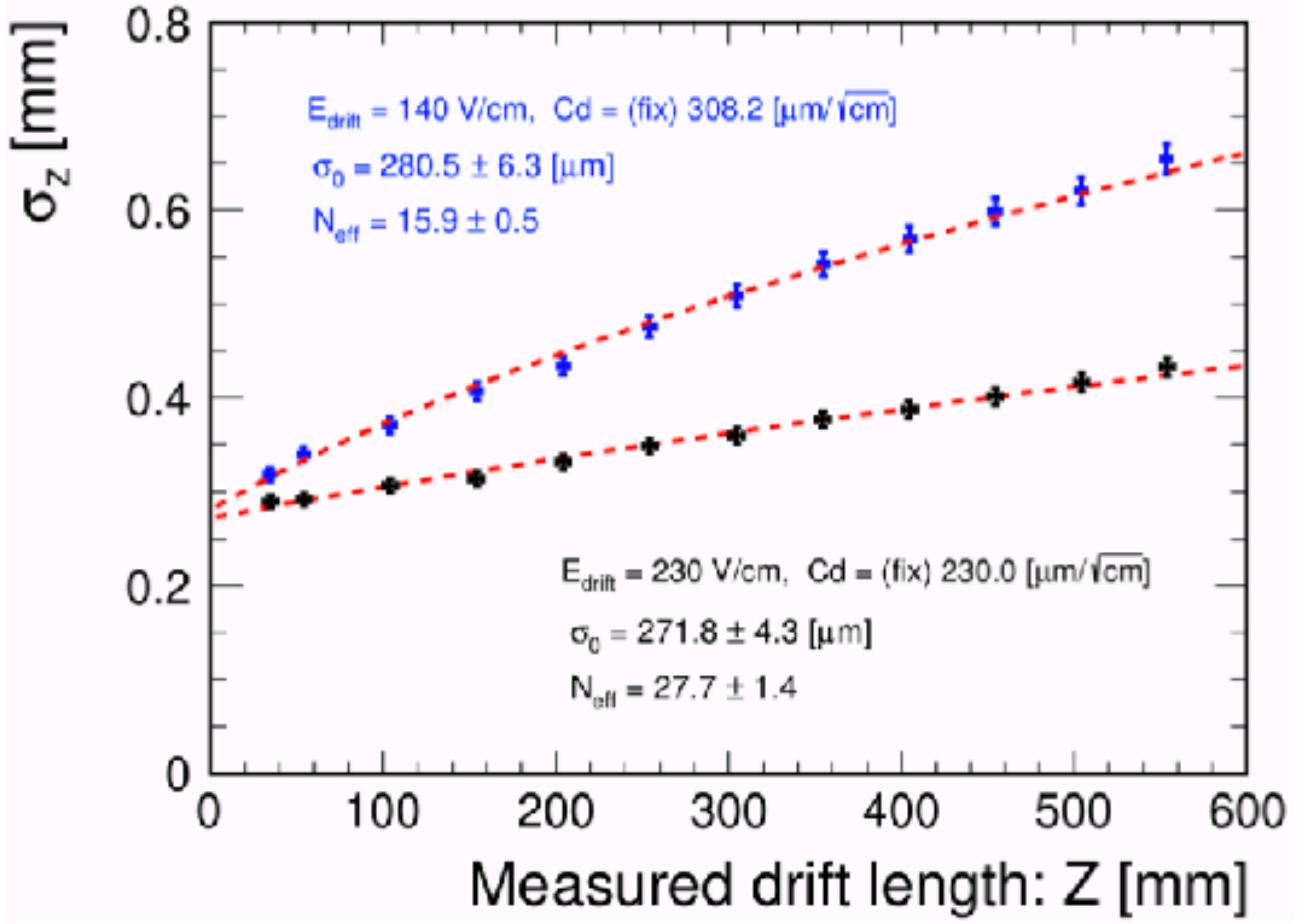
Japanese Group

S. Narita	Iwate Univ.
K. Fujii	IPNS/KEK
D. Jeans	IPNS/KEK
T. Fusayasu	Saga Univ.
Y. Kato	Kinki Univ.
M. Kobayashi	IPNS/KEK
T. Matsuda	IPNS/KEK
A. Sugiyama	Saga Univ.
T. Takahashi	Hiroshima Univ.
T. Watanabe	Kogakuin Univ.
Y. Aoki	IPNS/KEK
K. Yumino	Sokendai/KEK
J. Nakajima	Sokendai/KEK

D_RD_18 Project

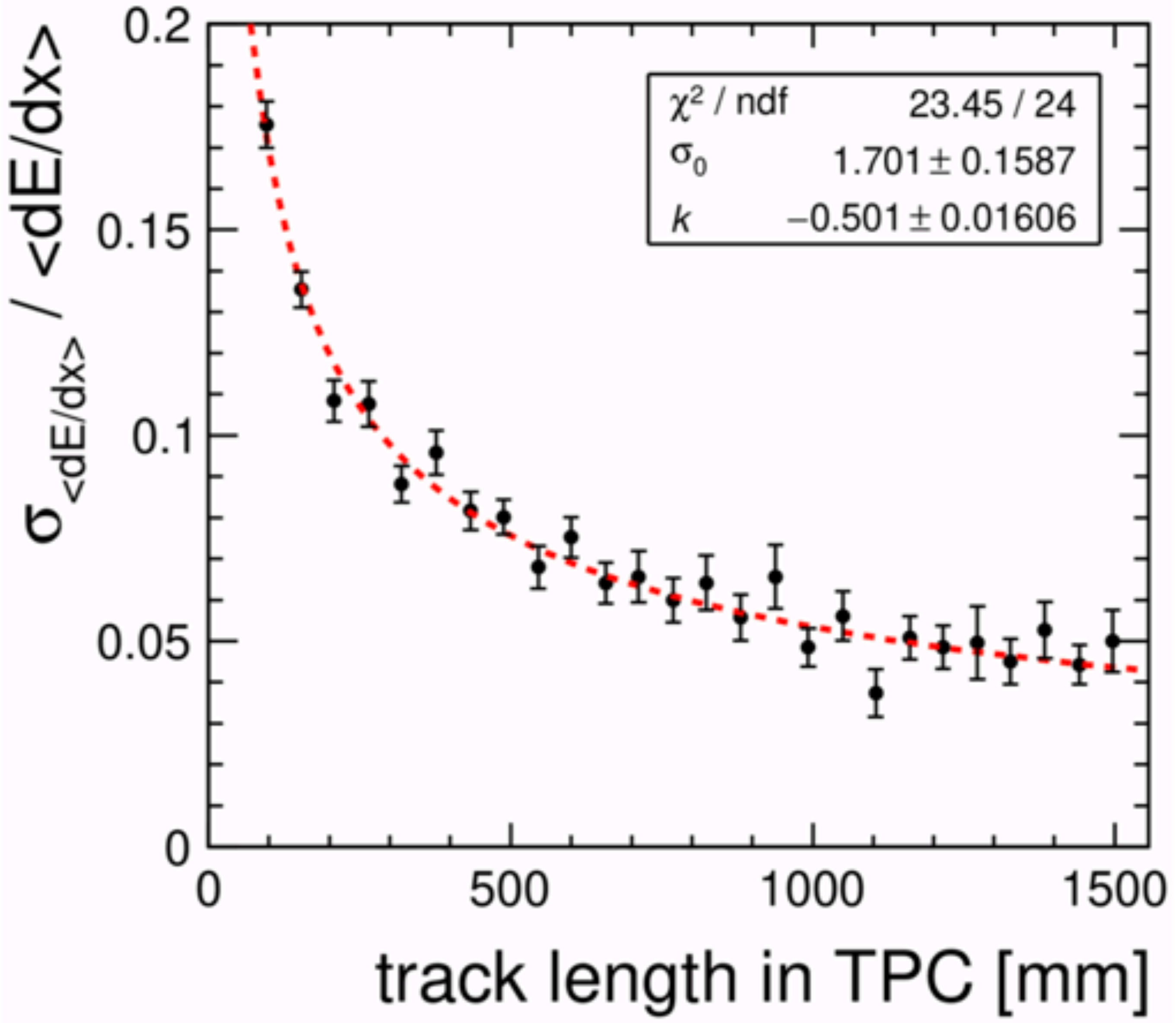
Transverse and Longitudinal Resolutions





Extrapolation to a magnetic field of 3.5 T and 2.35 m drift length yields to a maximum 100 μm over the full drift length

dE/dx Resolution



dE/dx resolution measured with LP and extrapoled to ILD TPC

GEM:

- $\sigma_{dE/dx}$ = 4.1% for 220 hits
- no degradation due to gating GEM

Micromegas:

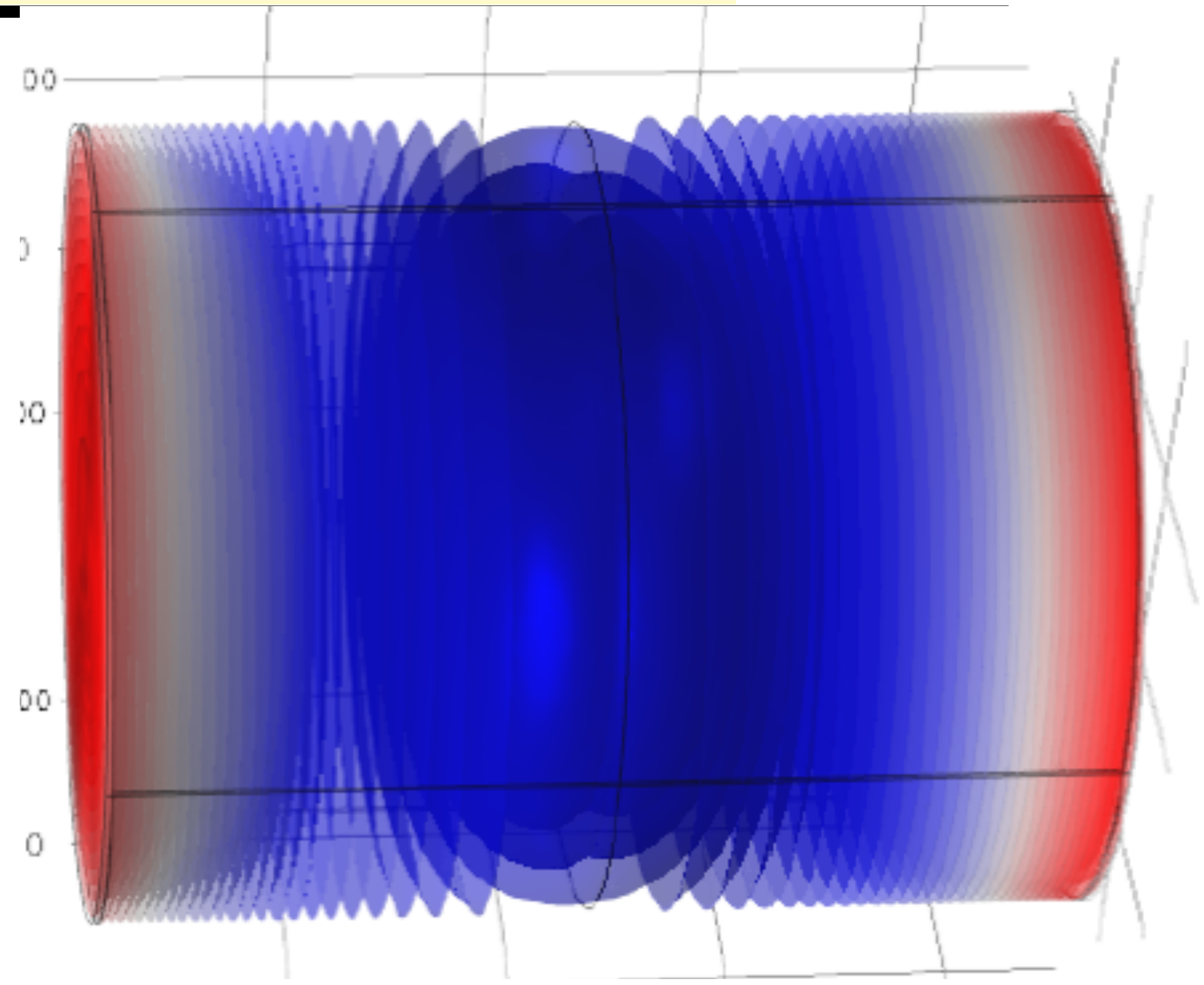
- $\sigma_{dE/dx}$ = 4.8% for 192 hits
- no degradation due to resistive foil

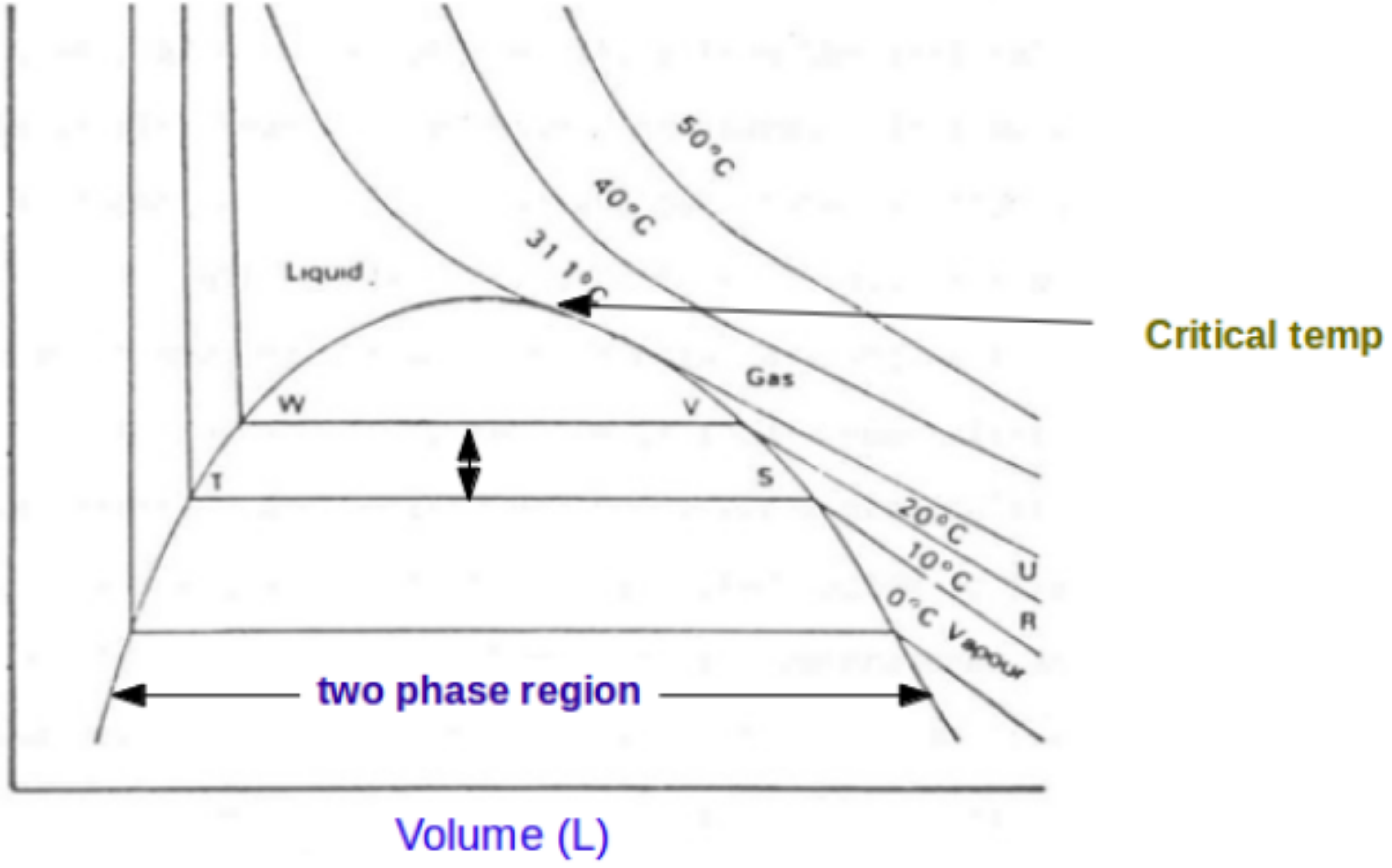
.

TPC cooling

- To avoid temperature gradients in the gas, the TPC needs to the cooled at room temperature. This also avoids condensation.
- TPC heat budget: 6kW / 60 kW per endcap in the pad and pixel options, respectively
- An efficient way to cool at room temperature is to use 2-phase CO_2 at high pressure:
  - At 60 bar the temperature is about 20°C, at 15 bar it is -20°C (used for Si detectors)
  - Other advantages are : low viscosity of CO_2, not risk of water leak,…

Simulation without cooling 72°C to 32°C





D_RD_18 Project

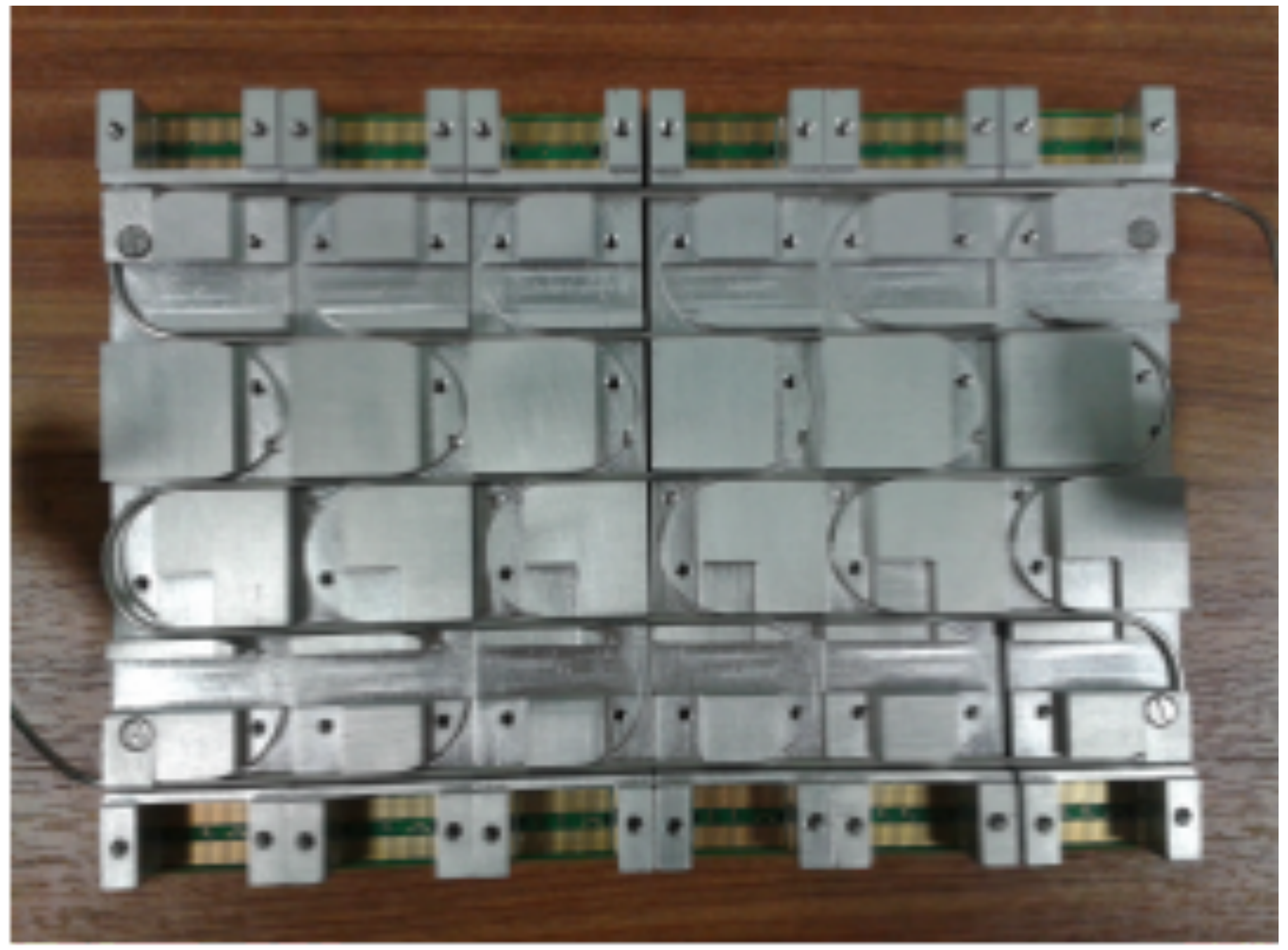
Transportable Refrigeration Apparatus for CO2 Investigation (TRACI)

Designed by a Nikhef-CERN collaboration (Bart Verlaat, T. Szwarc, L. Zwalinski,…)
1 unit purchased by KEK and installed at DESY

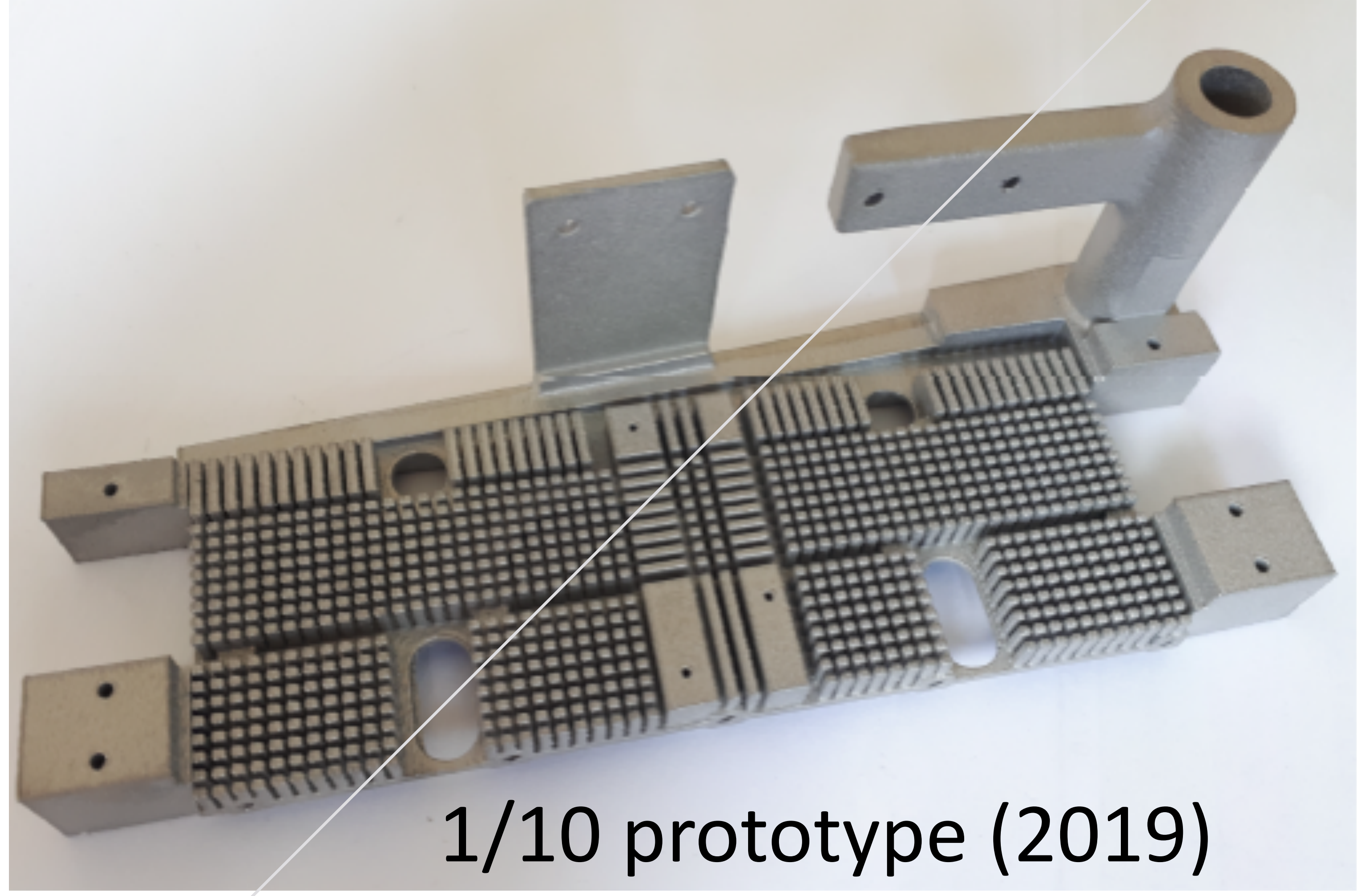
Refrigerent power ~300 W
1 kg of CO_2
Nominal flow rate 2.5 g/s

Implementations:

Stainless-steel pipe (2013-2018)



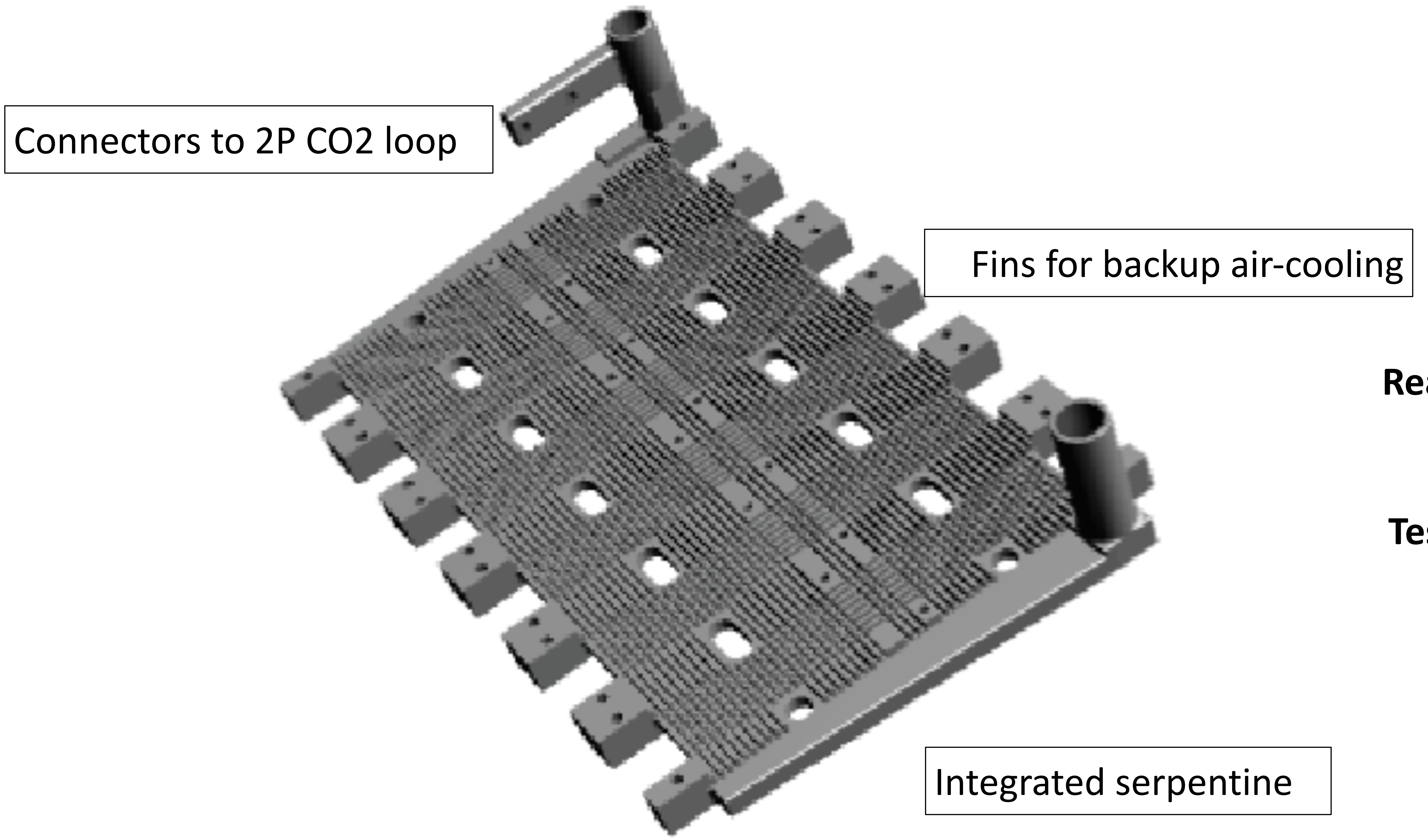
3D-printed Aluminum (2019-2021)



1/10 prototype (2019)

Integrated serpentine
Drastic safety measures for Al 3D printing (flamable Al powder)

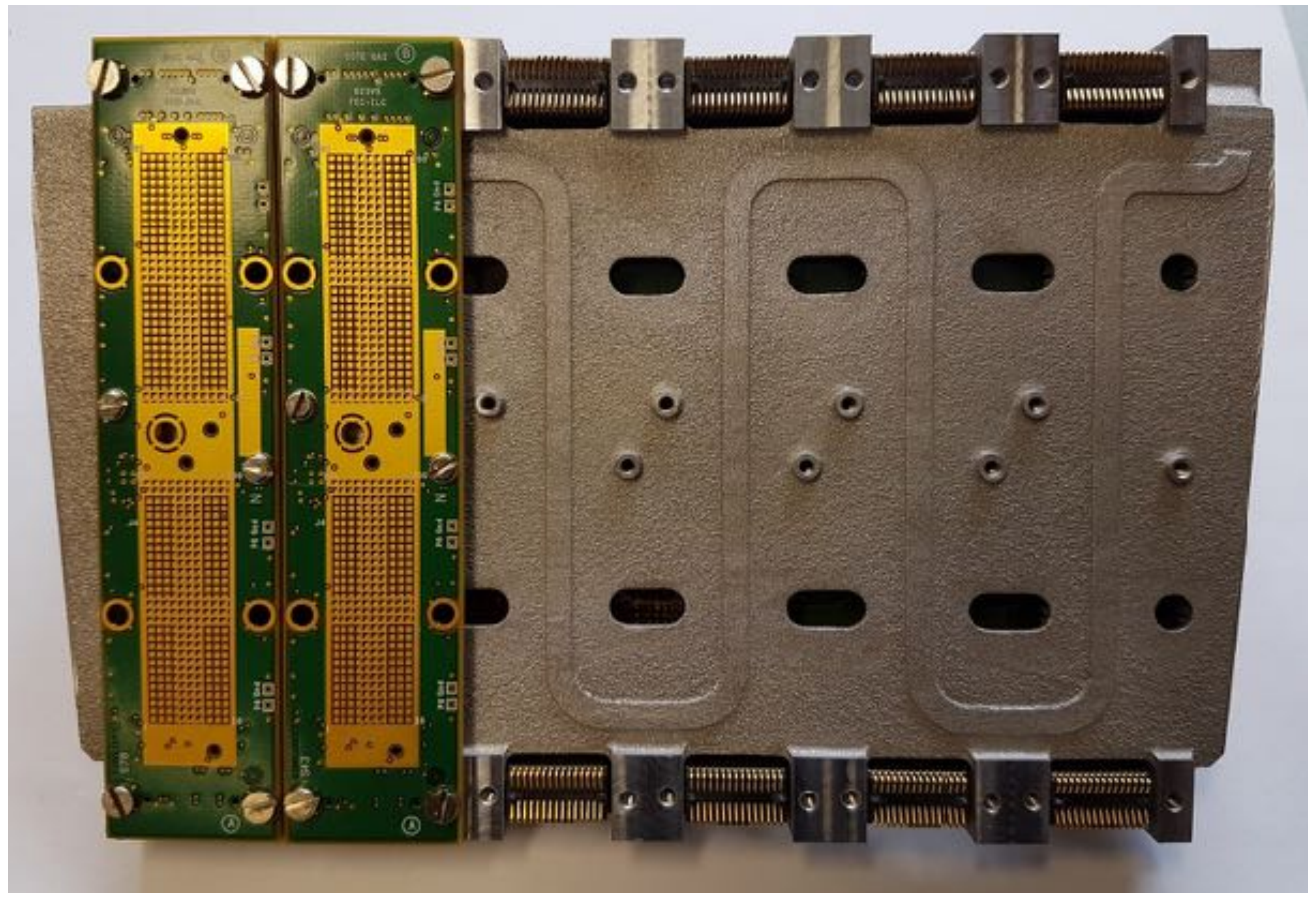
D_RD_18 Project



Realized at Saclay within a R&D project on metallic additive manufacturing (COSTARD)
Tested at DESY in October 2021

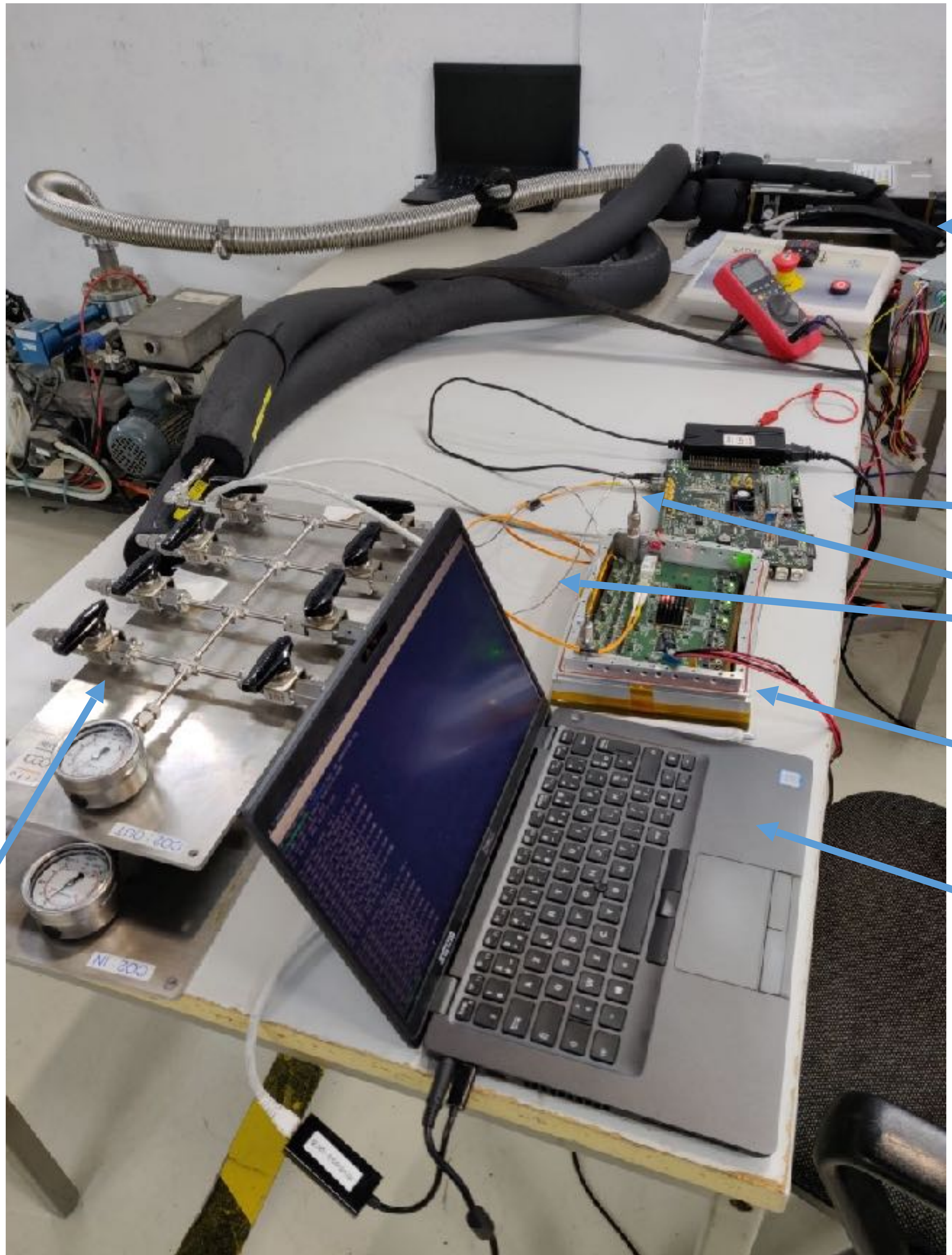
M. Riallot, O. Tellier, Y. Jan

Experimental setup

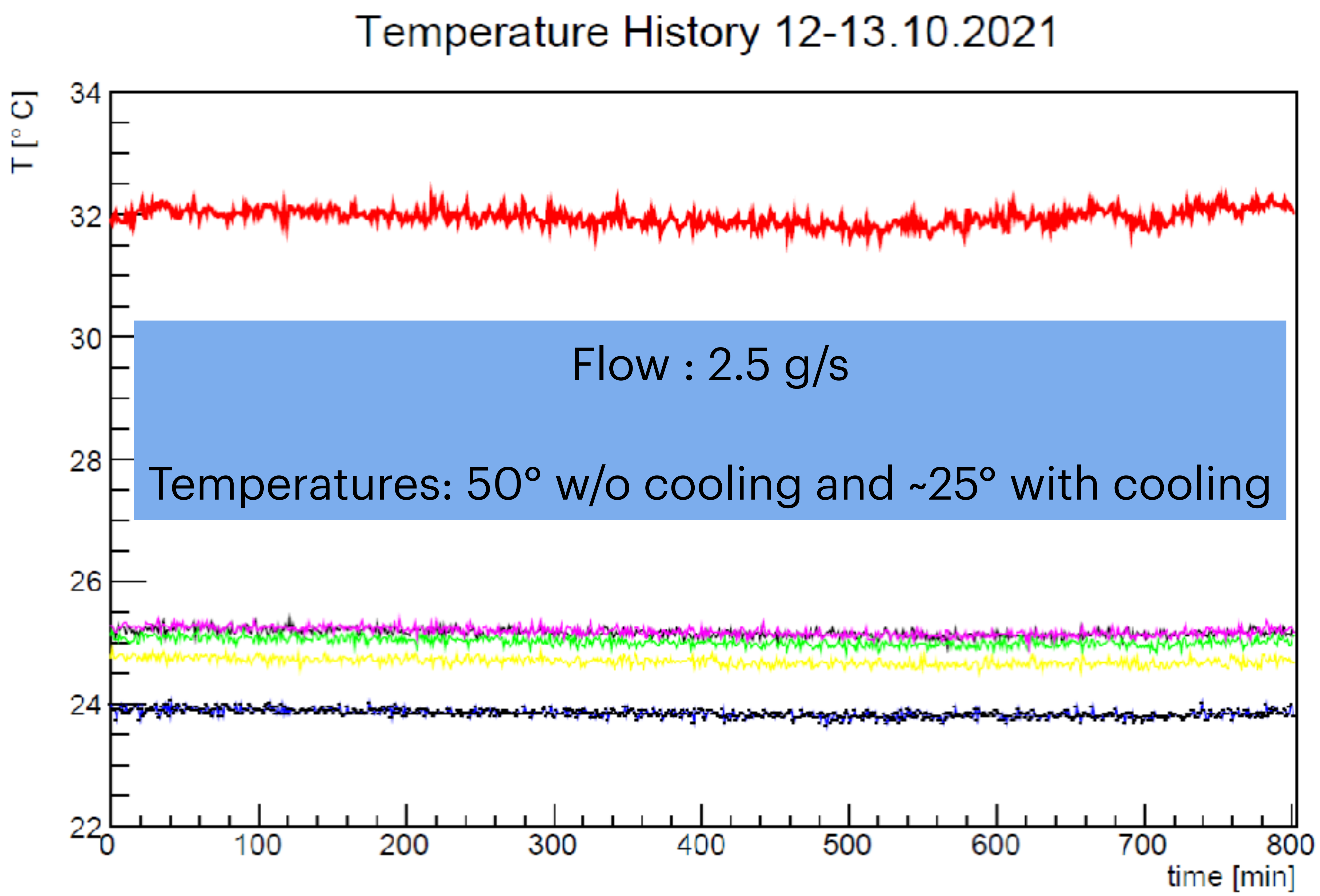


Cooling plate equipped with 2 Front-End Electronic Cards out of 6

Each Front-End card and the mezzanine module card (which includes ADC, FPGA and voltage regulators) are temperature monitored.

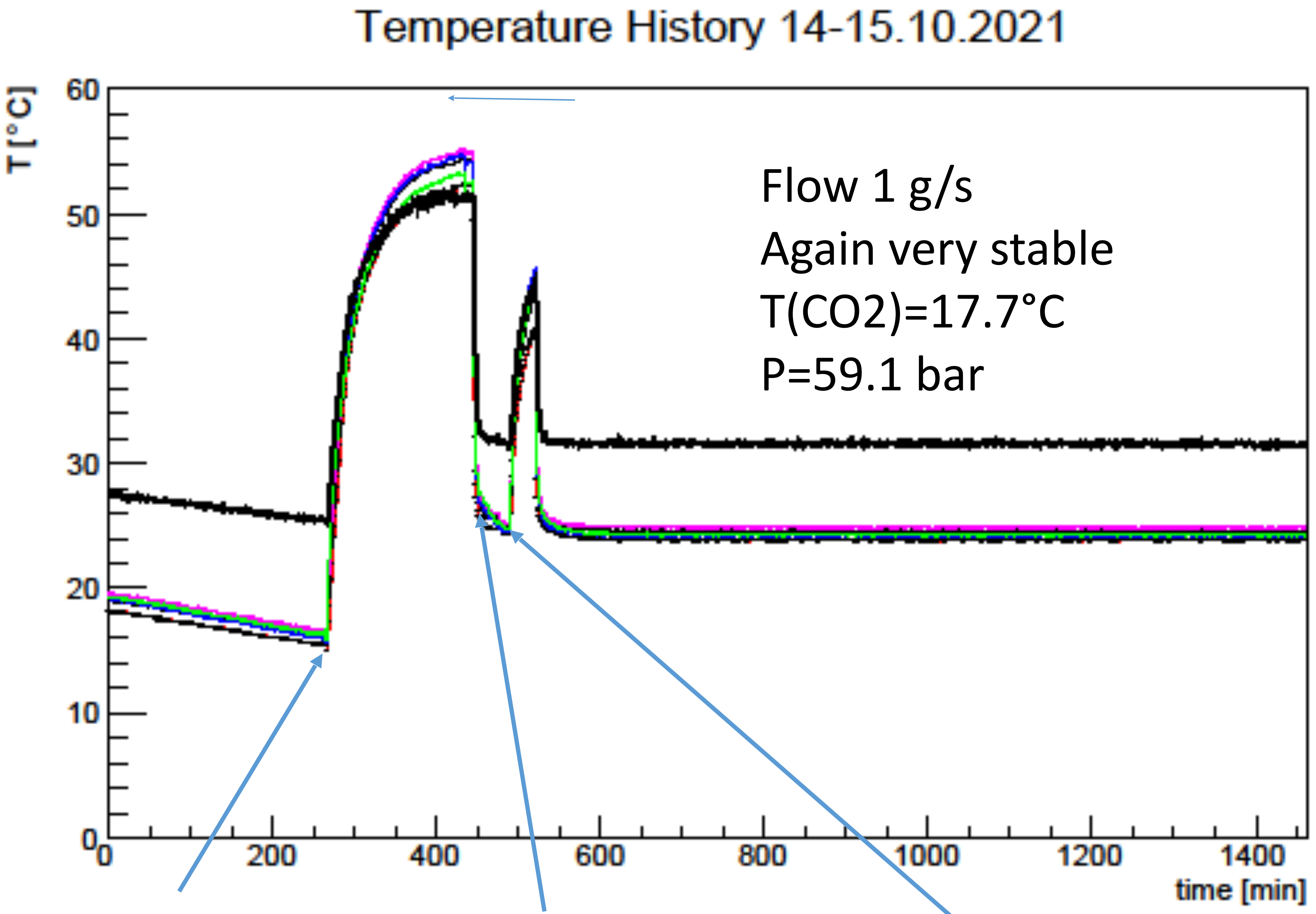


D_RD_18 Project



Mezzanine
stable within 0.2°C

Front-end cards
stable within 0.1°C



Stop flow to
re-fill

Resume flow from
0 to 2.4 g/s

Off/On again

Temperature stable during 25 hours

CONCLUSION

- Successful test of a new 3D-printed cooling plate for CO_2
- Simpler than a pipe
- Efficient back-up air cooling

- Ready to provide the cooling for the common LCTPC module

Possible implementation in ILD TPC

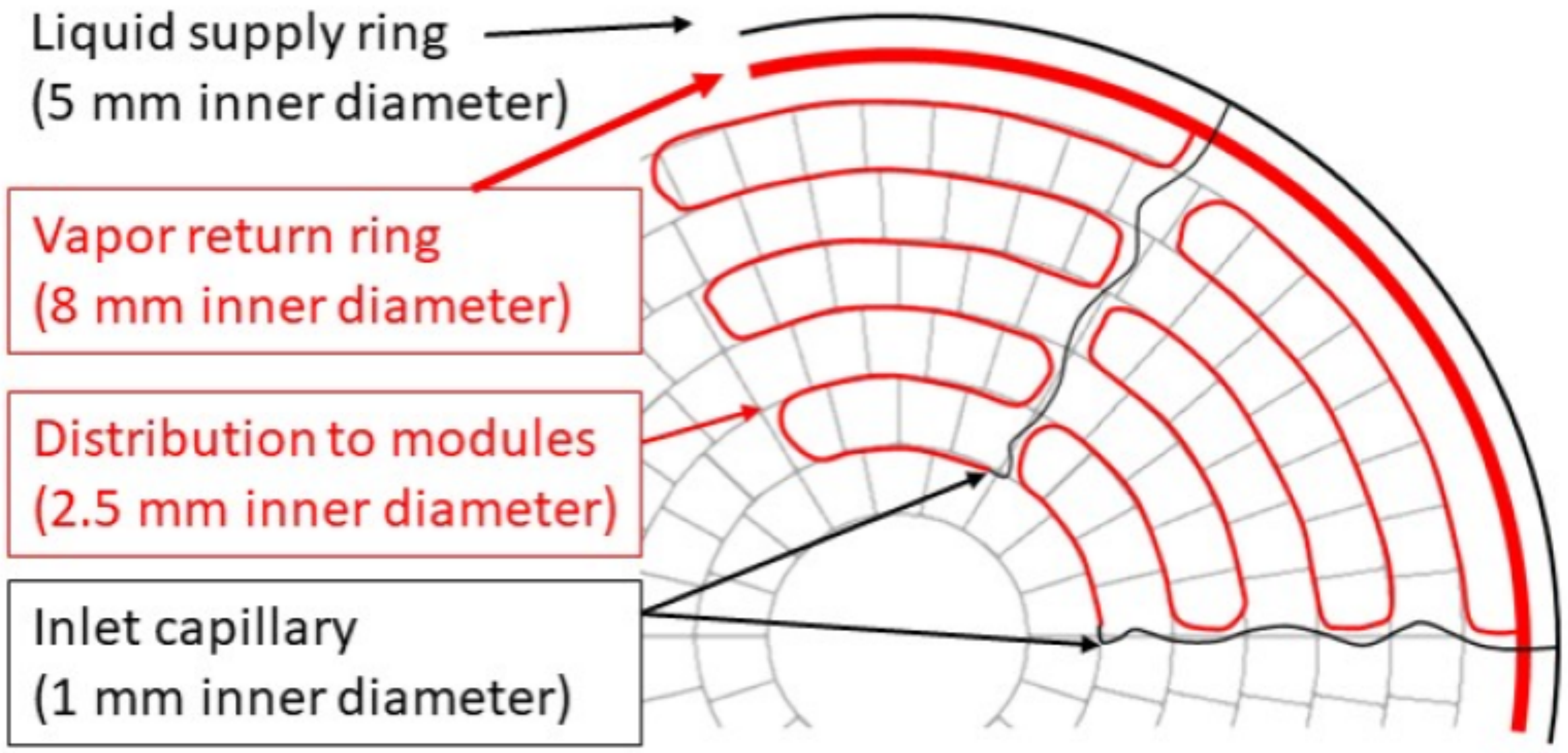


Figure 6.18. Sketch of a TPC cooling system with tube routing on the TPC end plate. Figure courtesy of Bart Verlaat, Nikhef.

ID : HEP_15	Title: Testbeams with the highly granular SiW ECAL and implementation of timing information					
	French Group			**Japanese Group**		
	name (Family name, First name)	**title**	**lab.**	**name** (Family name, First name)	**title**	**lab.**
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	BOUDRY, Vincent	Dr.	LLR	JEANS, Daniel	Assoc. Prof.	KEK
PIs: **Members:**	JIMENEZ, Fabricio	Dr.	LLR	KAWAGOE, Kiyotomo	Prof.	Kyushu Univ.
	KUNATH, Jonas	PhD	LLR	YOSHIOKA, Tamaki	Assoc. Prof.	Kyushu Univ.
	OKUGAWA, Yuichi	PhD	IJCLab/UPSaclay and Tohoku U	SANUKI, Tomoyuki	Assoc. Prof.	Tohoku University
	Dominique Breton	Dr.	IJCLab			
	Jihane Maalmi	Dr.	IJCLab			
	Jimmy Jeglot	Dr.	IJCLab			
	Stephane Callier	Dr.	OMEGA			

Status of R&D for thin PCBs for the CALICE SiW ECAL (FKPPL project)

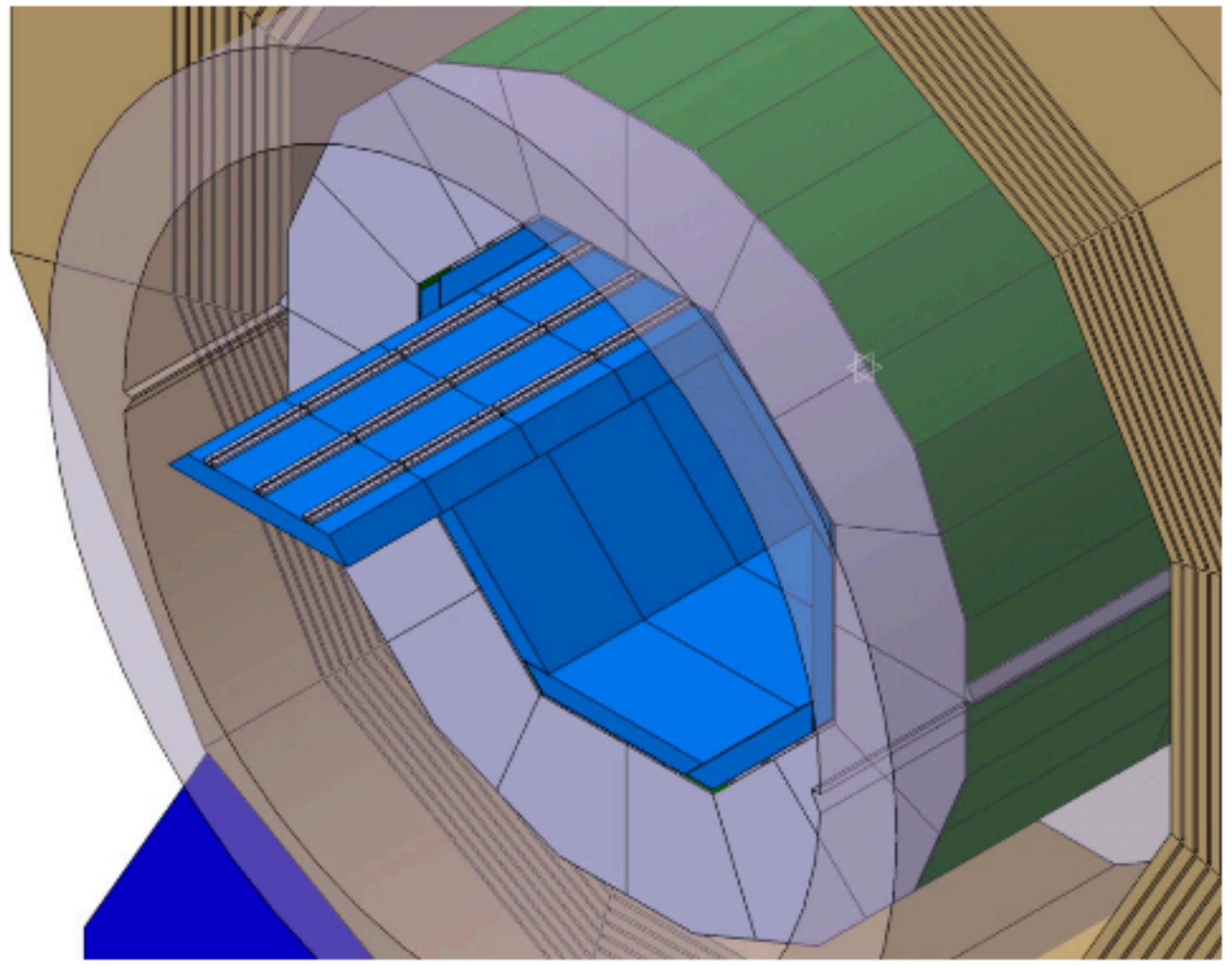
Roman Pöschl

On behalf of the SiW ECAL Groups in CALICE:

TYL/FJPPL – FKPPL – May 2022

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- $O(10^8)$ cells
- "No space"

=> Large integration effort

Basic Requirements:

- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

Basic Choices:

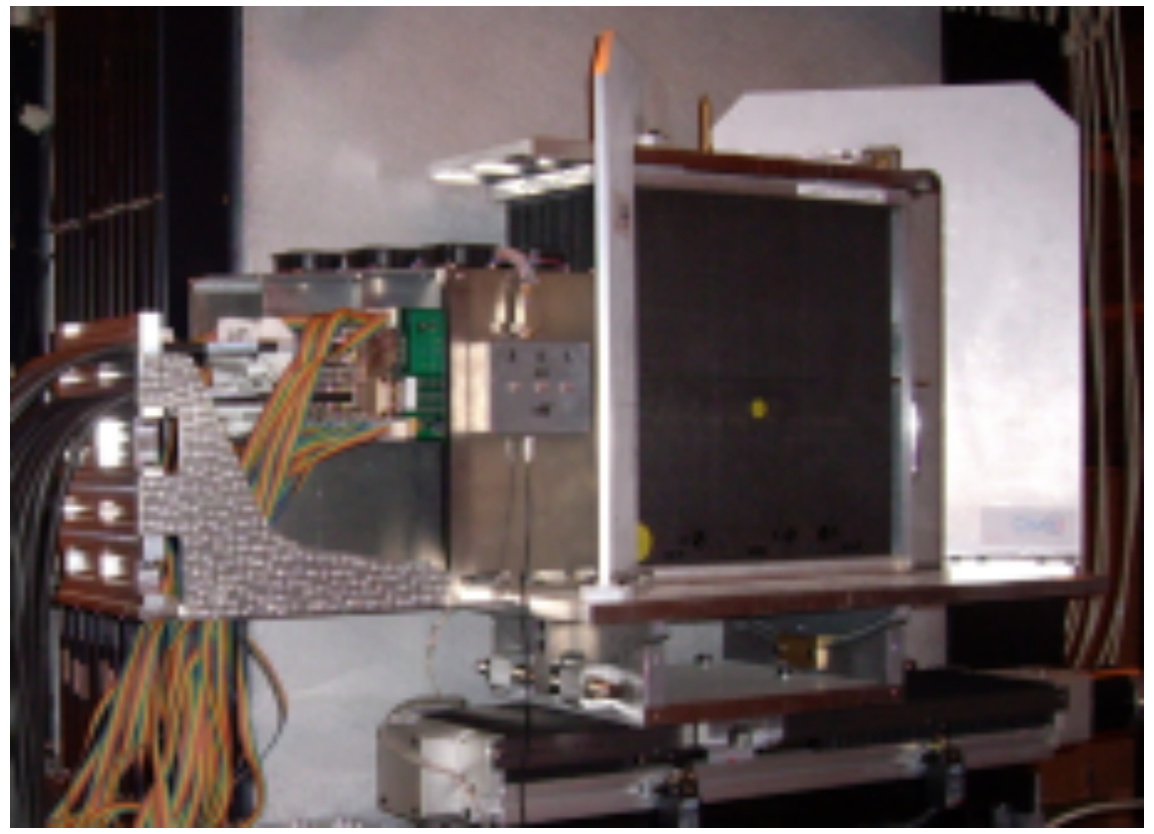
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 at MIP level as design value

- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

Steps of R&D

Physics Prototype

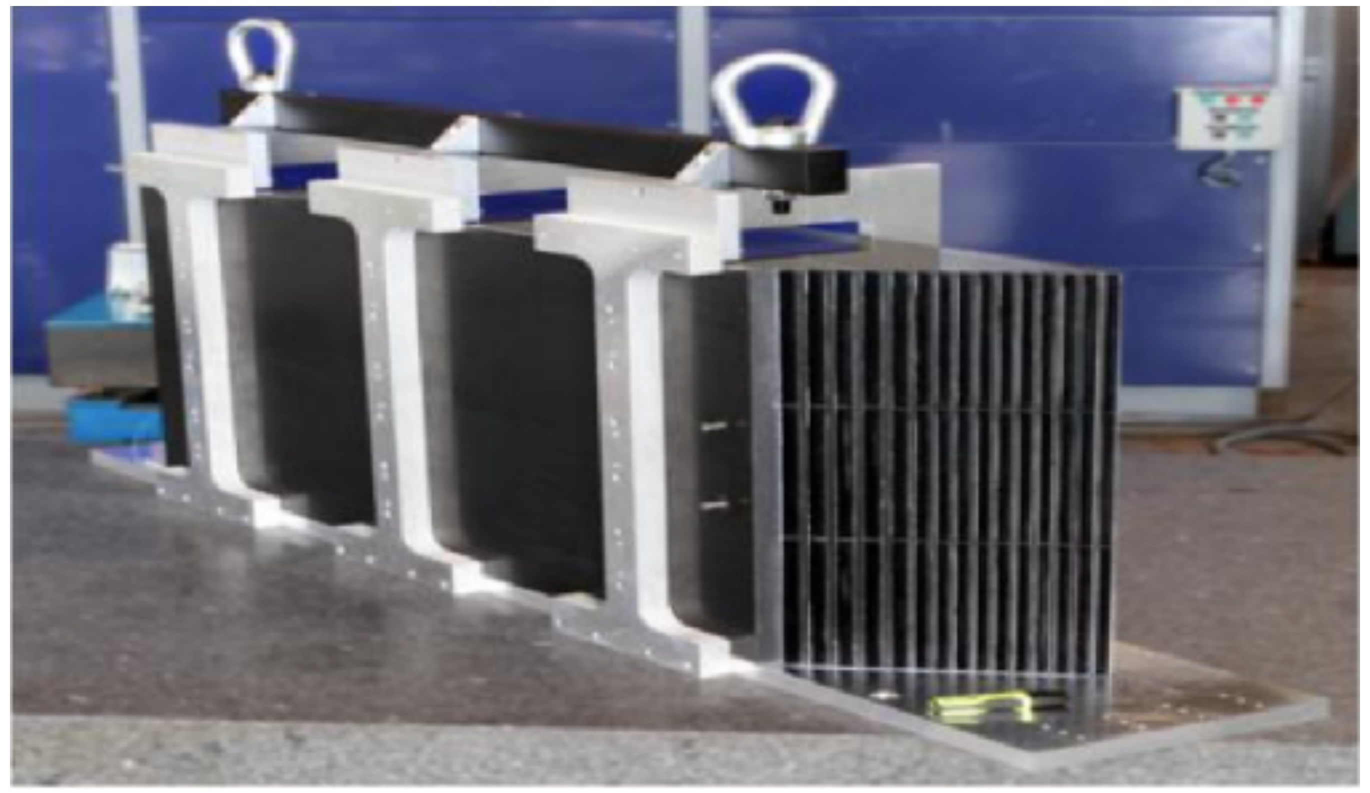
2003 - 2012



- Proof of principle of granular calorimeters
- Large scale combined beam tests

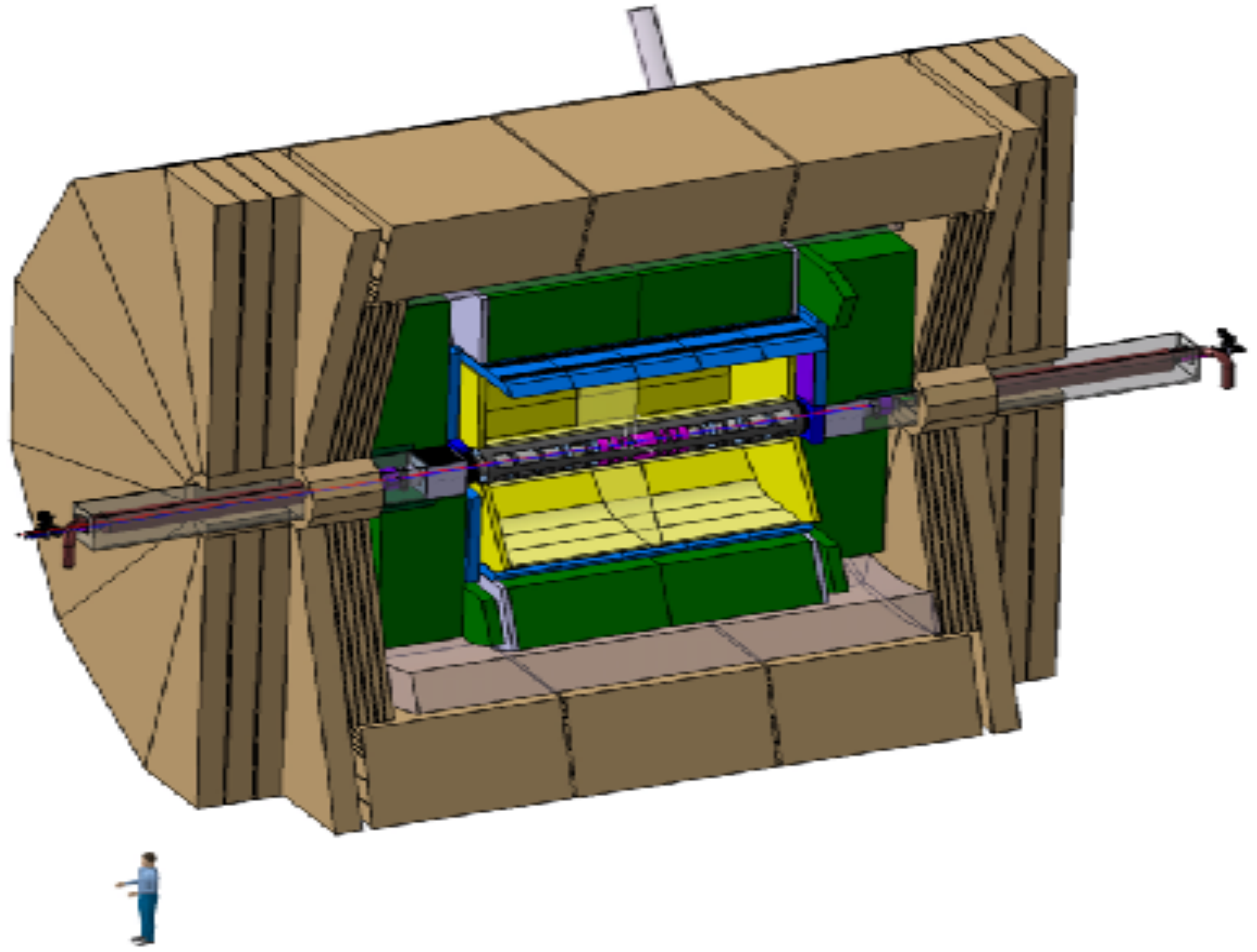
Technological Prototype

2010 - ...



- Engineering challenges
- Higher granularity
- Lower noise
- **Today**

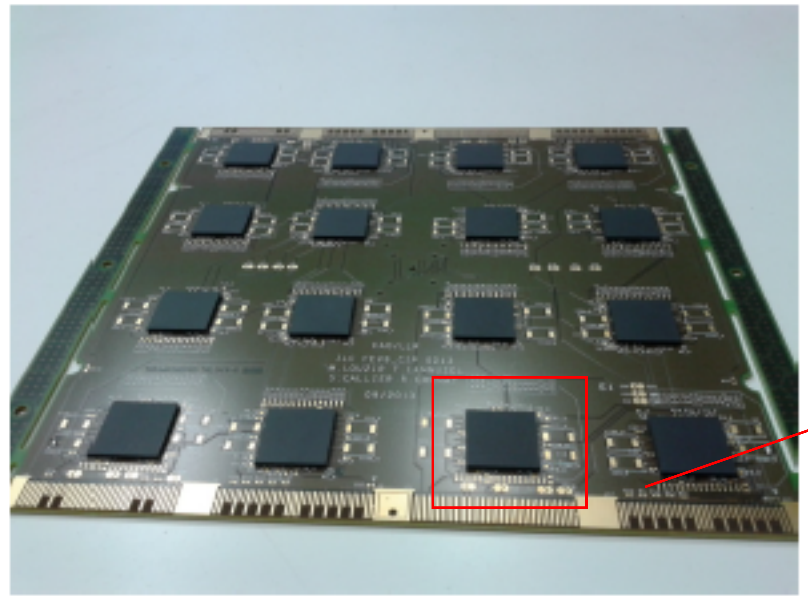
LC detector



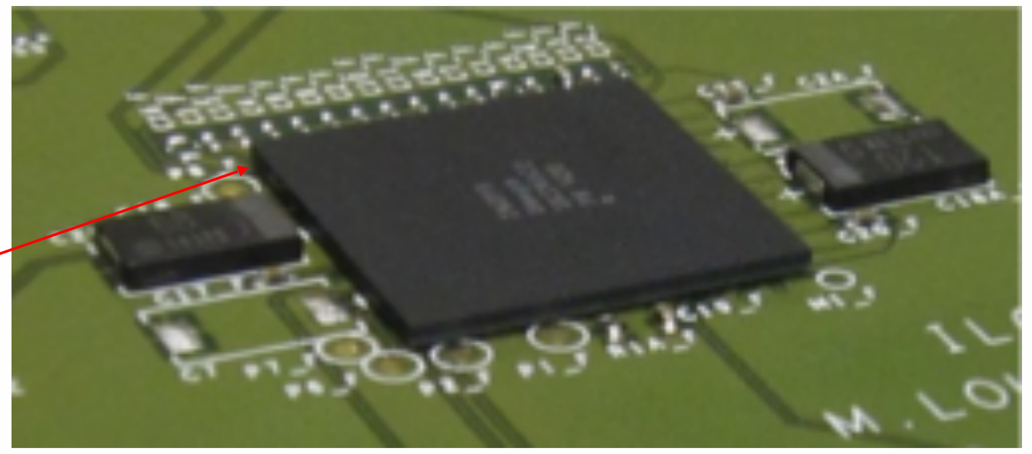
- The goal
  - Typically 10^8 calorimeter cells
- Compare:
  - ATLAS LAr ~10^5 cells
  - CMS HGCAL ~10^7 cells

SiW Ecal – Elements of (long) layer

ASIC+PCB+SiWafer
=ASU
Size 18x18 cm²
(IJCLab, Kyushu, OMEGA, LLR, SKKU)

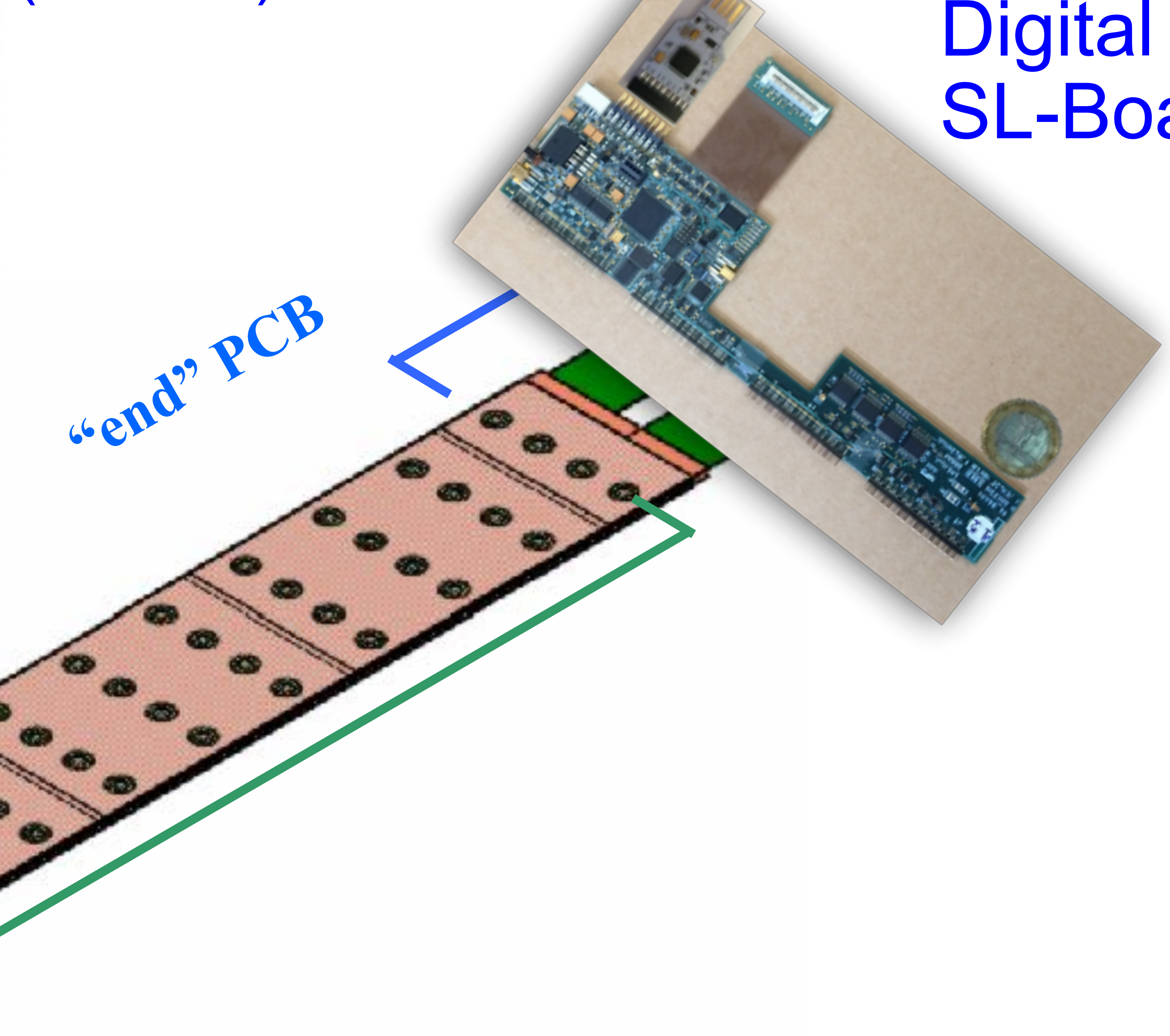


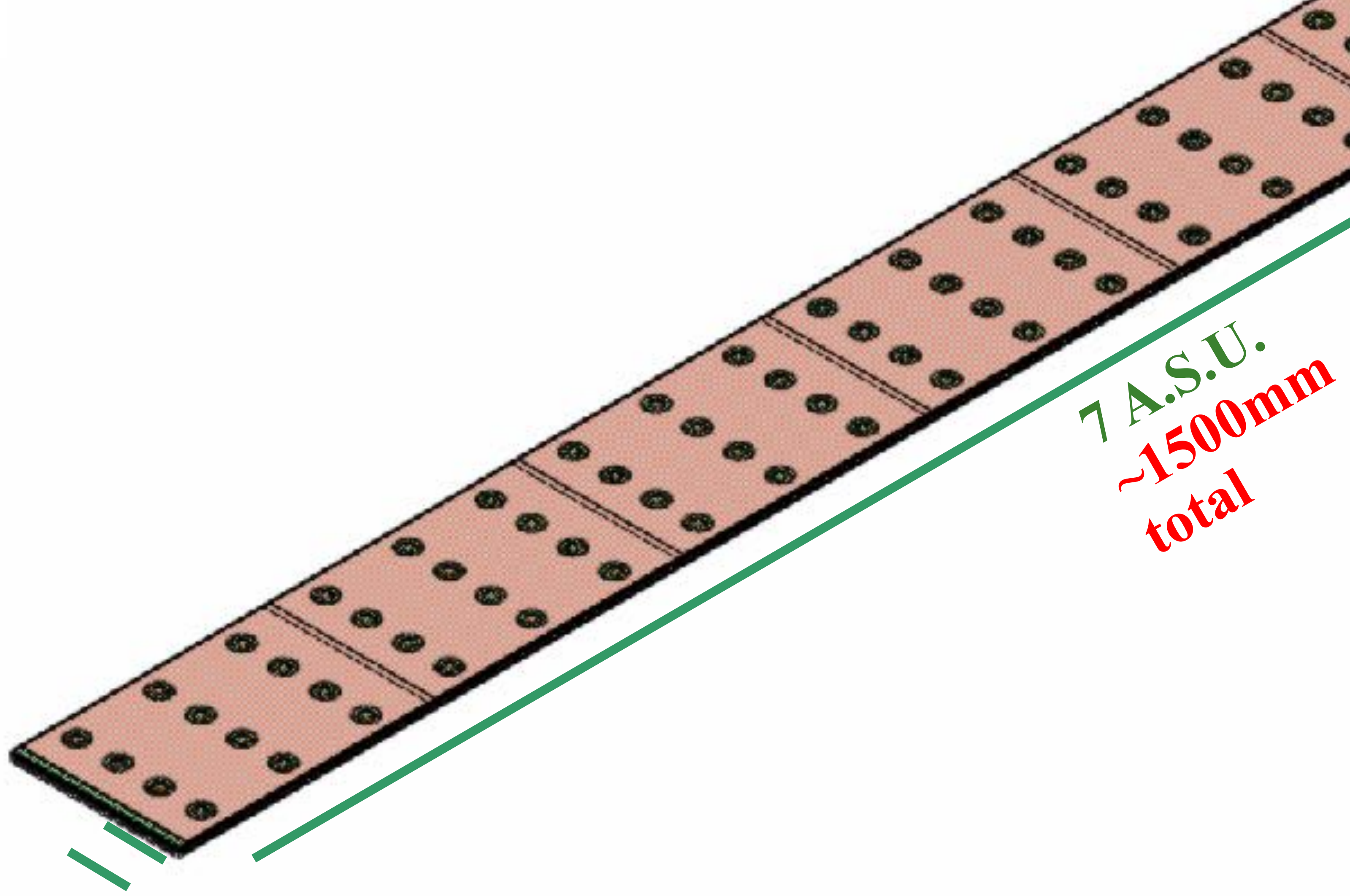
ASIC SKIROC2(a)
(OMEGA)
Wire Bonded or
In BGA package
(IJCLab, Kyushu, LLR)



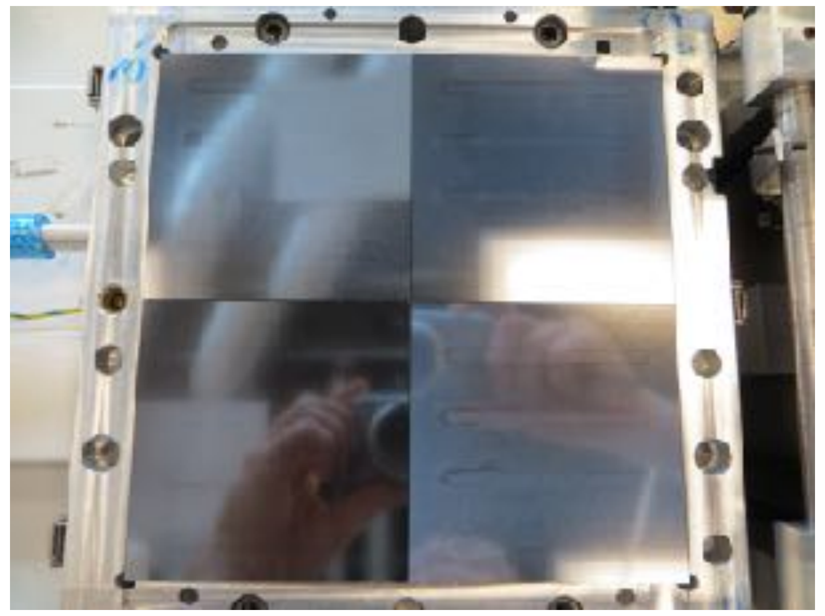
Interconnection
(IJCLab)

Digital readout
SL-Board (IJCLab)





SiWafers
glued
onto PCB
Pixel size
5.5x5.5 mm²
(LPNHE)

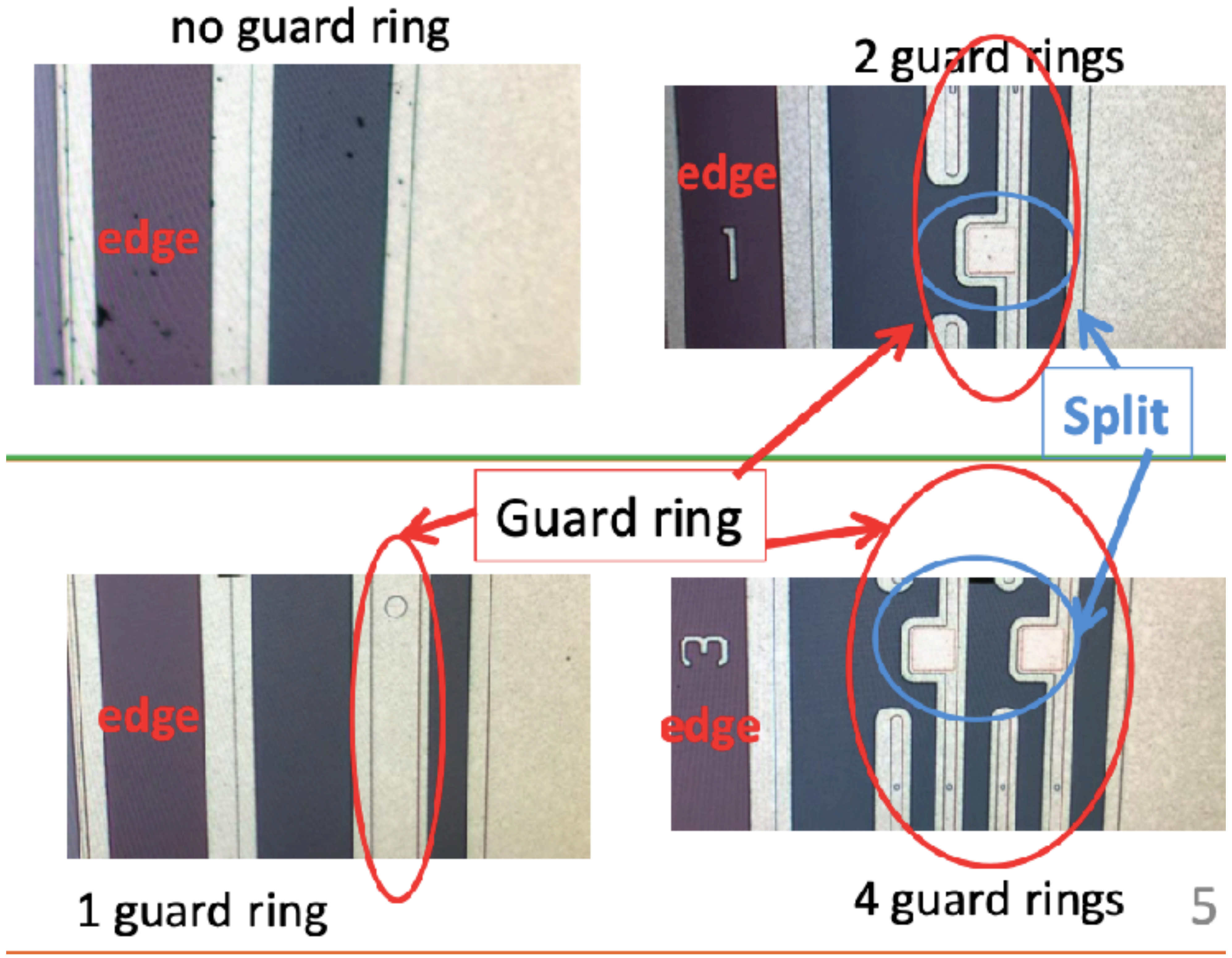


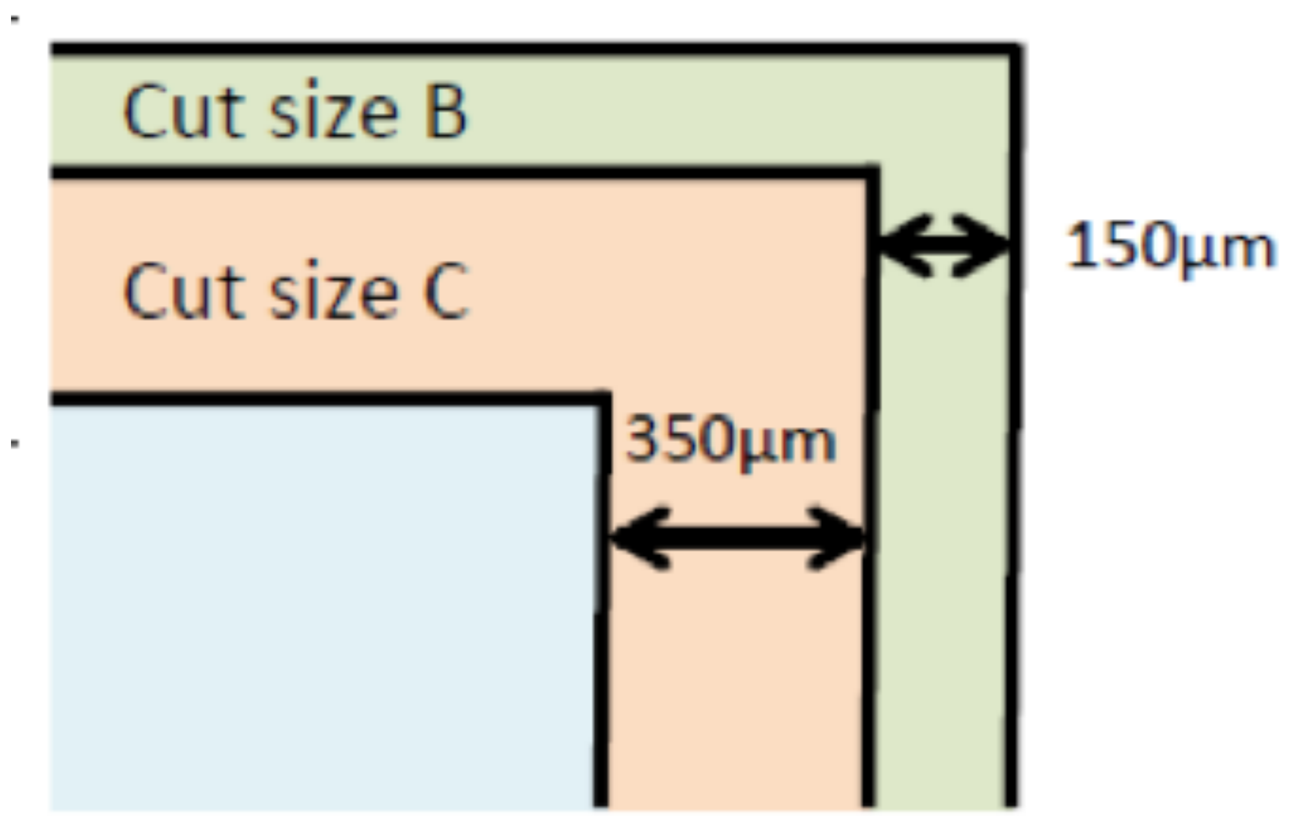
Note that an additional hub for hardware
Development is being set up at IFIC/Valencia

- The beam test set up will consist of a **stack of short layers** consisting of one ASU and a readout card each

SiW Ecal – Wafer R&D II

We (i.e. Mainly Kyushu) have tested several wafer types in previous years





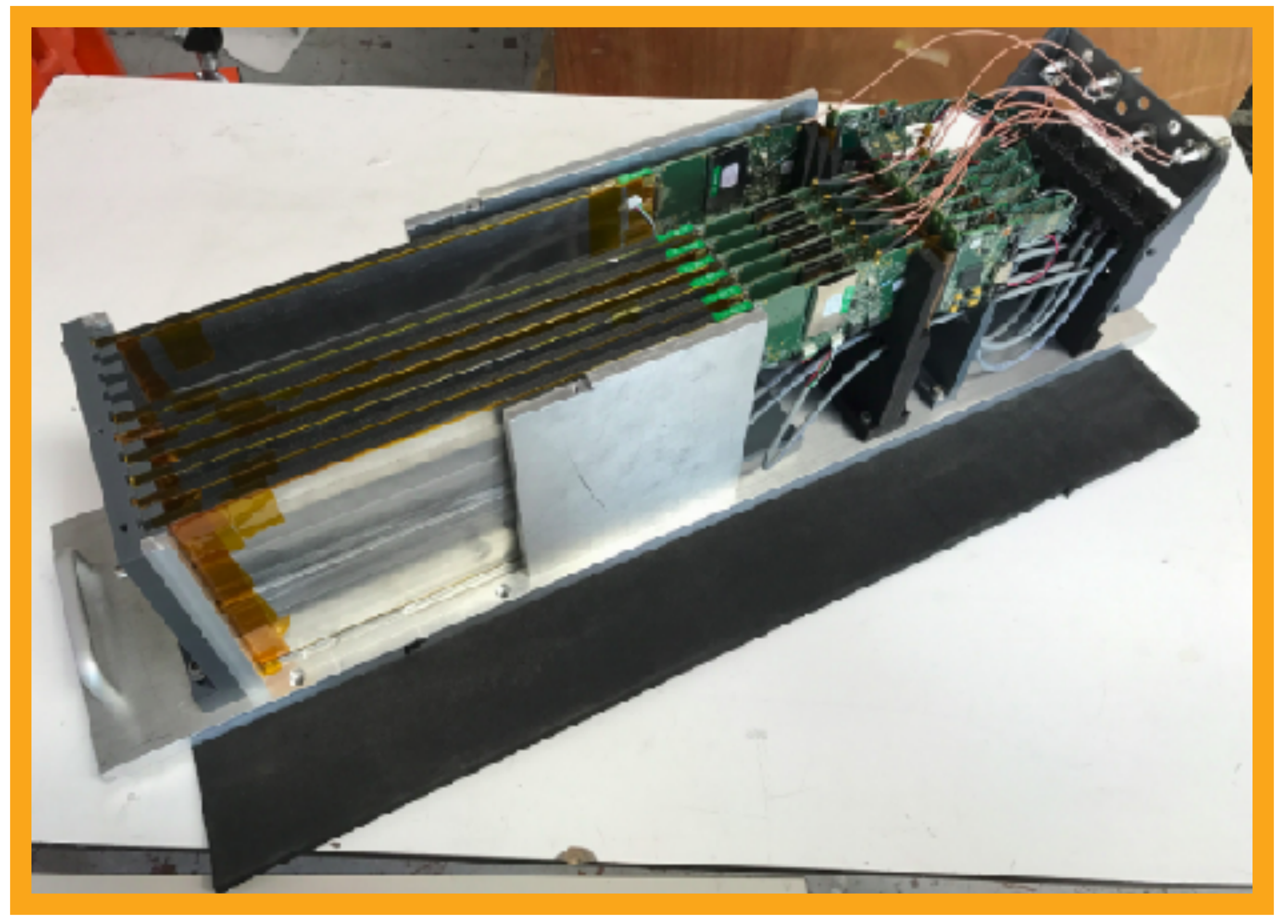
- Cut size determine the actual sensitive area of a wafer
- Different designs mainly on test samples of “baby wafers”
- The “Hamamatsu” standard is still 0 or 1 full guard ring
  - 0 is “fake 0” guard ring, in fact there is still a small guard ring

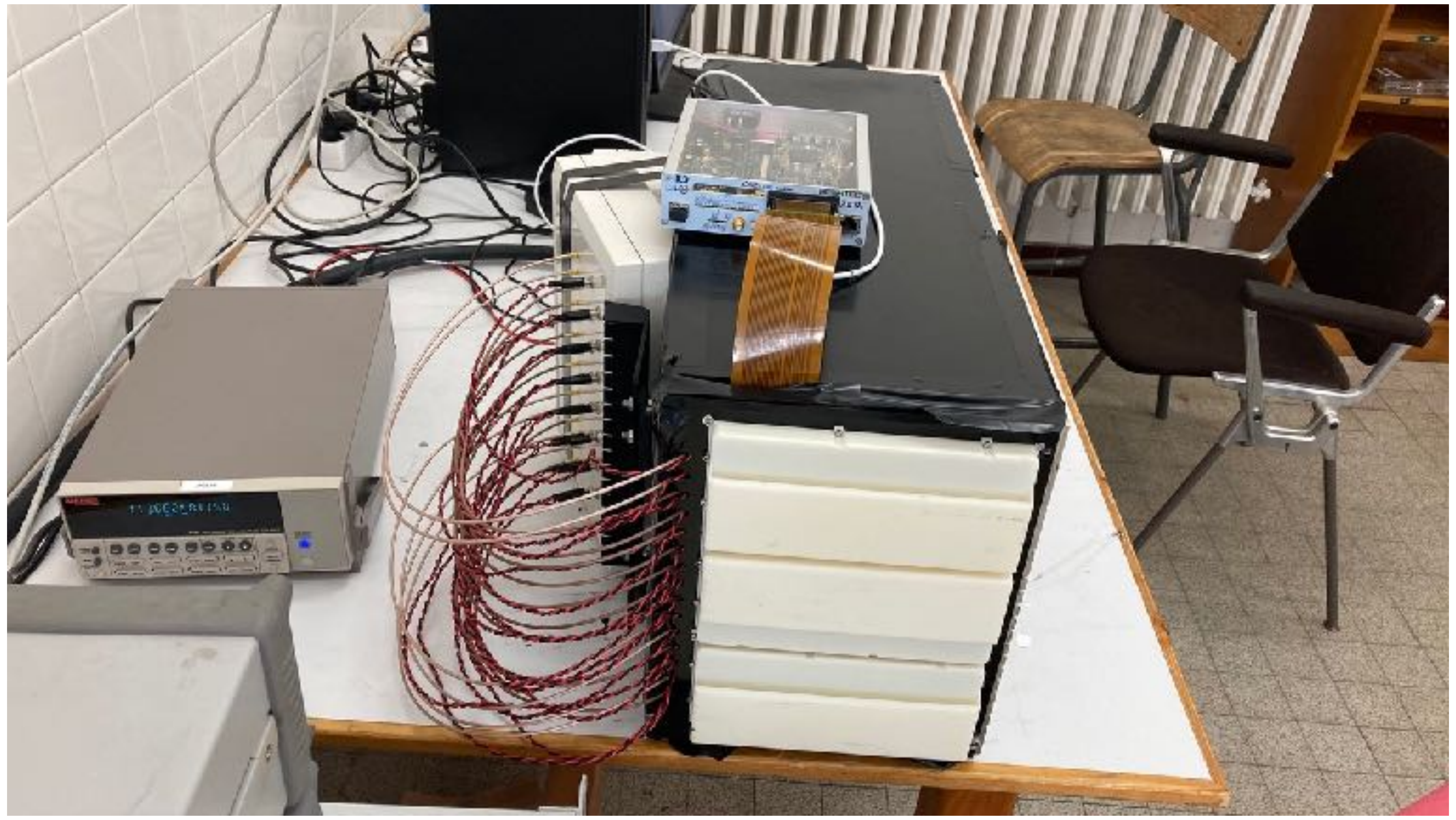
Observations in recent years (see also backup for more details)

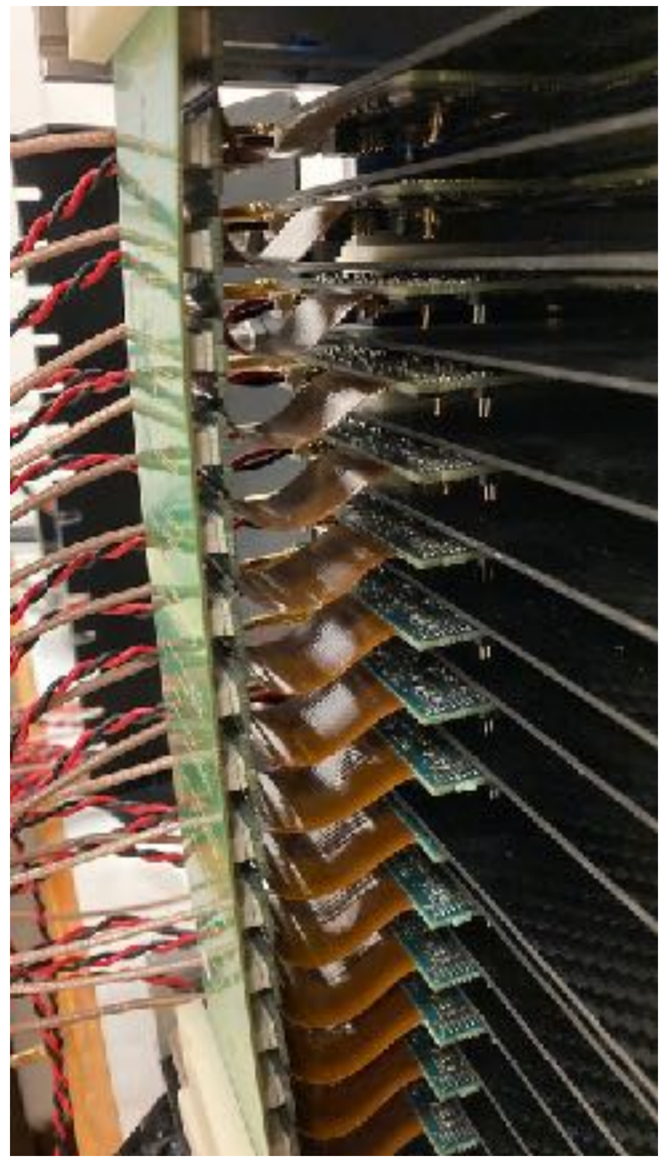
- Split or no guard ring lead to suppression of square events
- In prototype we still use full wafers with 0 or 1 guard ring
- General trend of reduction of bias voltage
- Can operate 500mum wafers at 60-80 V in full depletion

- Towards 8” wafers?
  - General trend (e.g. CMS) is to use 8” wafers
  - Larger surface/wafer =>smaller cost
  - Standard thickness 725mum
  - Impossible to get access to HPK production
  - Lines (CMS HGCAL Production)

SiW ECAL 2018 -> 2022







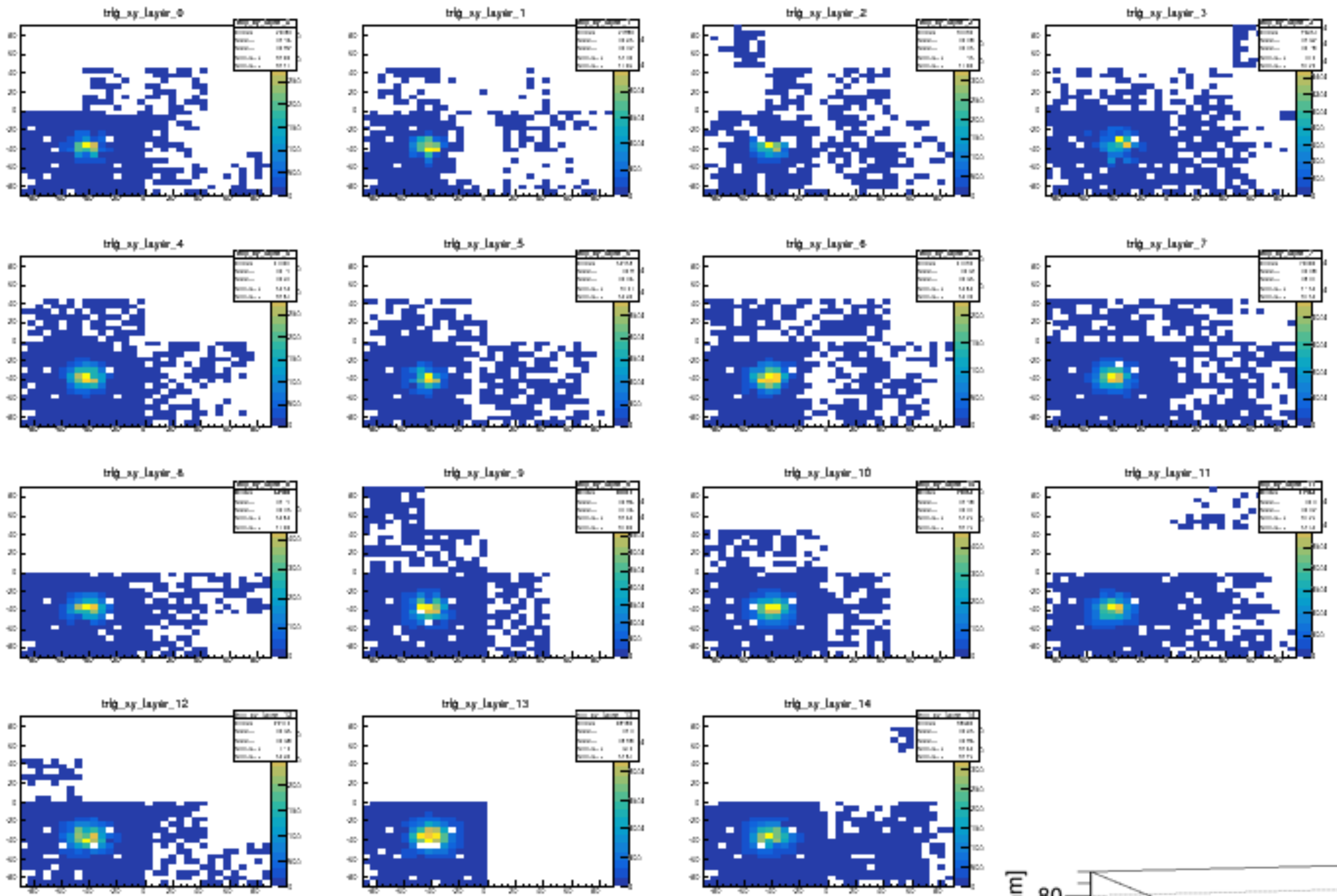
- 7 short layers (18x18x0.5cm^3)
- 1024 channels per layer => 7186 cells
  - Assembly chains in France and Japan
  - Beam tests at DESY and CERN since 2016

- 15 layers equivalent to 15360 readout cells
- Overall size 640x304x246mm^3
  - Commissioned in 2020 and 2021
  - Testbeams (finally) in November 2021 and March 2022
  - 1.5 years in waiting loop due to pandemic

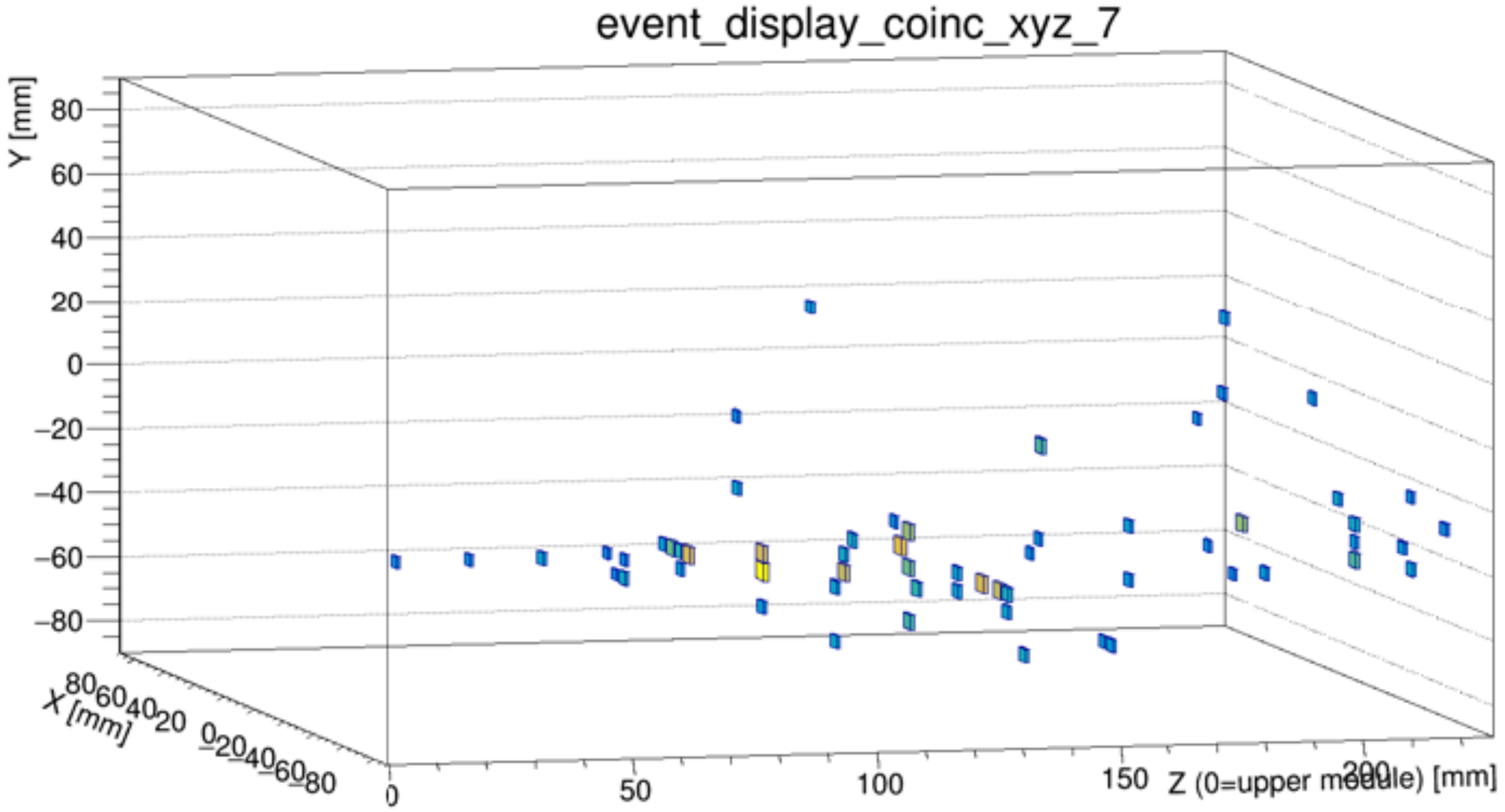
SiW-ECAL in beam test @ DESY

Detector Setup

Detector in beam position

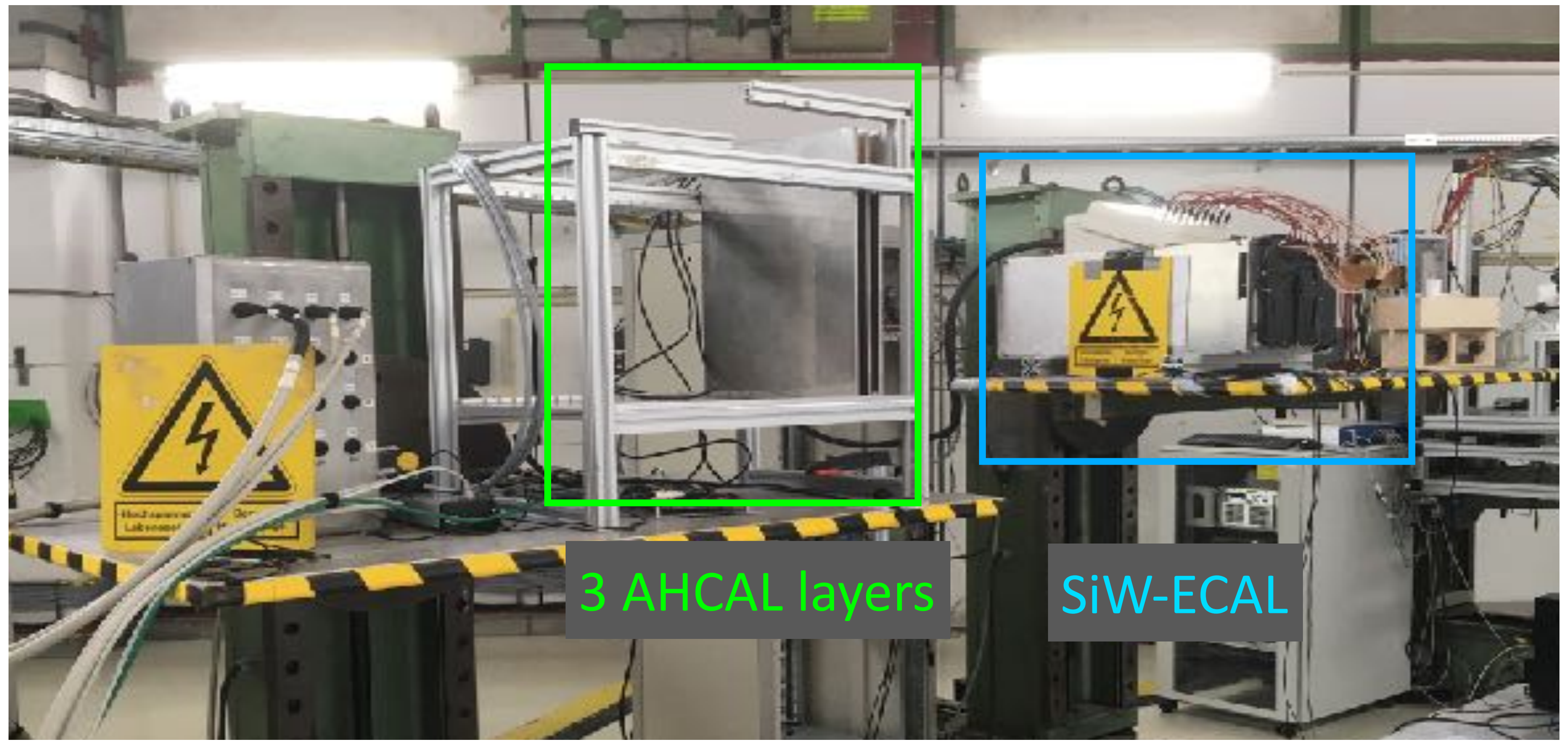


- Stack operational
- Beam spot in 15 layers



Common testbeams

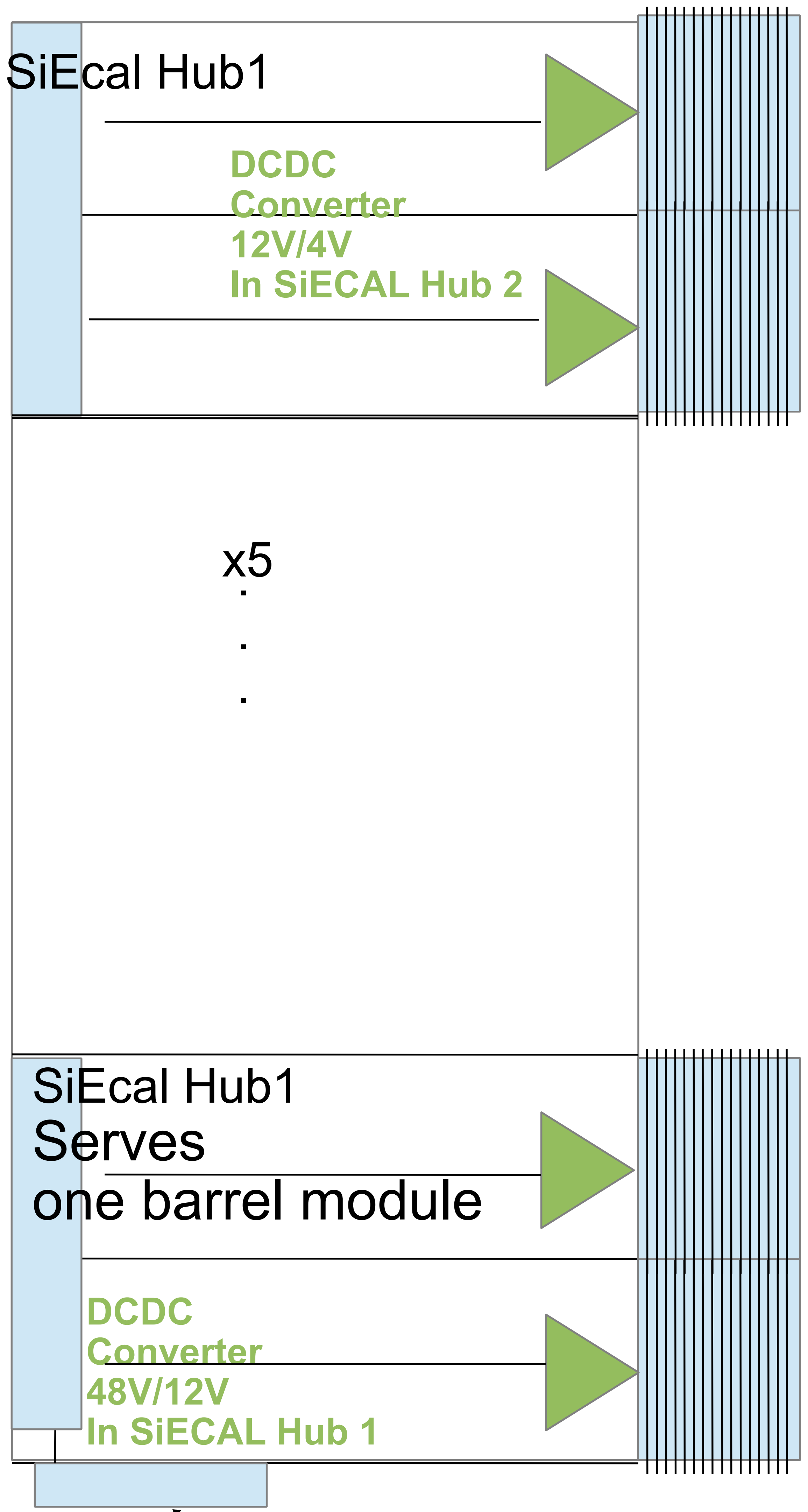
Preparation for common SiW-ECAL AHCAL beam test



SiW-ECAL + AHCAL DAQ test @ DESY in March 2022

- Successful synchronisation of data recorded with SIW-ECAL and AHCAL
- Common running makes full use of EUDAQ tools (developed within European projects)

Powering concept/management – ILD SiECAL



Slab column
15x600mA, 36 W

SiECALPatch panel
Current ~25A

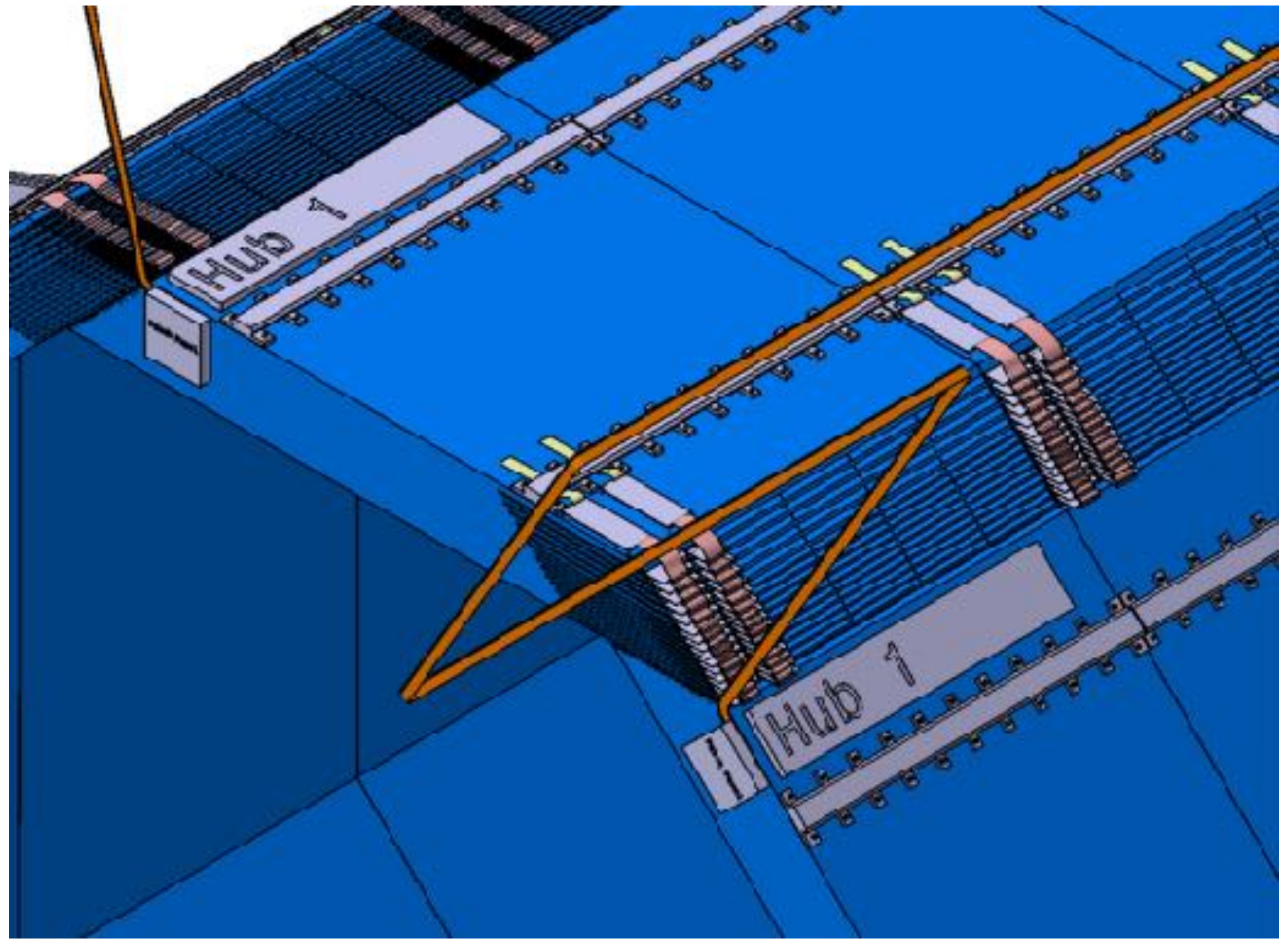
Reminder IDR

The **local** power storage is at the heart of the powering concept of the ILD SiECAL

Power cable trailer <-> SiECAL Patch panel

PowerSource
~52 V

Zoom into ILD Ecal barrel



- Total average power consumption **20 kW** for a calorimeter system with 10^8 cells*
  - Only possible through PP
- The art is to store the power very locally
- Issue for upcoming R&D

*Compare with 140 kW for CMS HGCAL FEE $6x10^6$ cells

Summary and outlook

- Two fully equipped COB Boards (finally) produced in 2021/22
- First systematic study of Chip-on-Board PCB in beam
  - Encouraging results - no serious issues discovered
  - Results comparable with those obtained for BGA based PCBs
- The successful beam test in March 2022 concludes the first R&D cycle on the COBs
  - Proof of principle that these PCBs can be built and operated
  - Real R&D success and it was clearly the continuous support by FKPPL / FJPPL that made this success possible!
  - Thank you very much

    Complete interruption due to pandemic
- Evaluate the gain of going to 4D tracking (timing) against further technological challenges