AIDA innova

CALICE

Status of R&D for thin PCBs for the CALICE SiW ECAL (FKPPL project)

Roman Pöschl

cnrs IN2P3 Les deux infinis

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

P2IO Physique des 2 Infinis et des Origines

université PARIS-SACLAY

INVESTISSEMENTS D'AVENIR

On behalf of the SiW ECAL Groups in CALICE:

SUNG KYUN KWAN UNIVERSITY

ΩMEGA Microelectronics

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

LLR

LPNHE PARIS

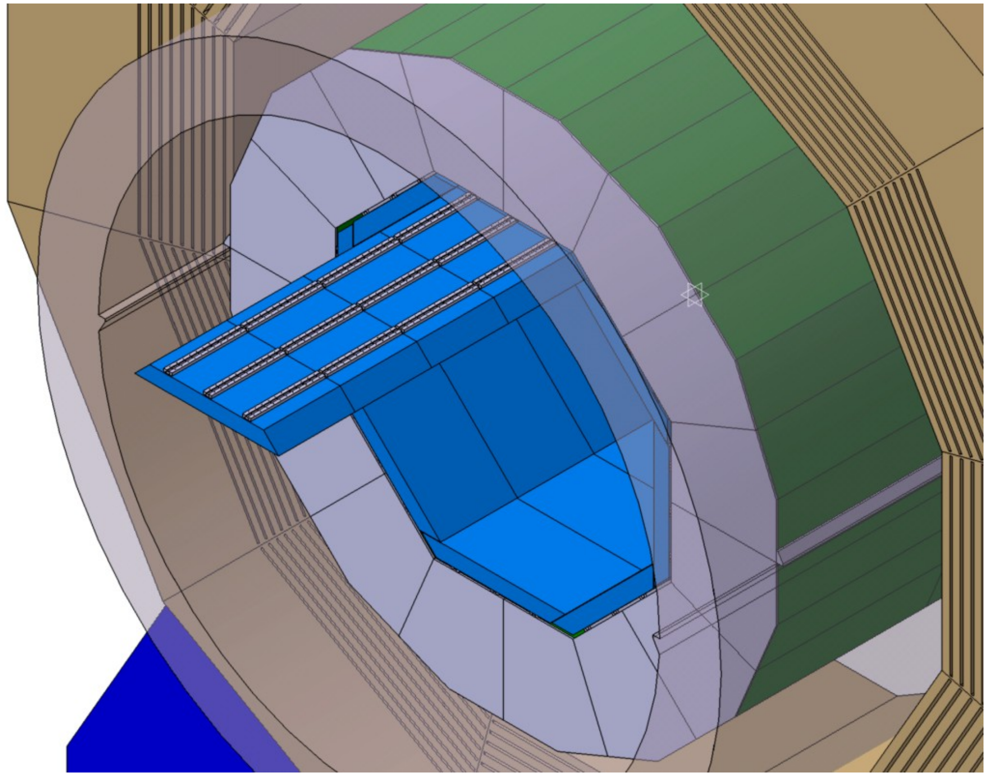
LPSC Grenoble

IFIC INSTITUT DE FÍSICA CORPUSCULAR

TYL/FJPPL – FKPPL – May 2022

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- O(10^8) cells
- “No space”
=> Large integration effort

Basic Requirements:

- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

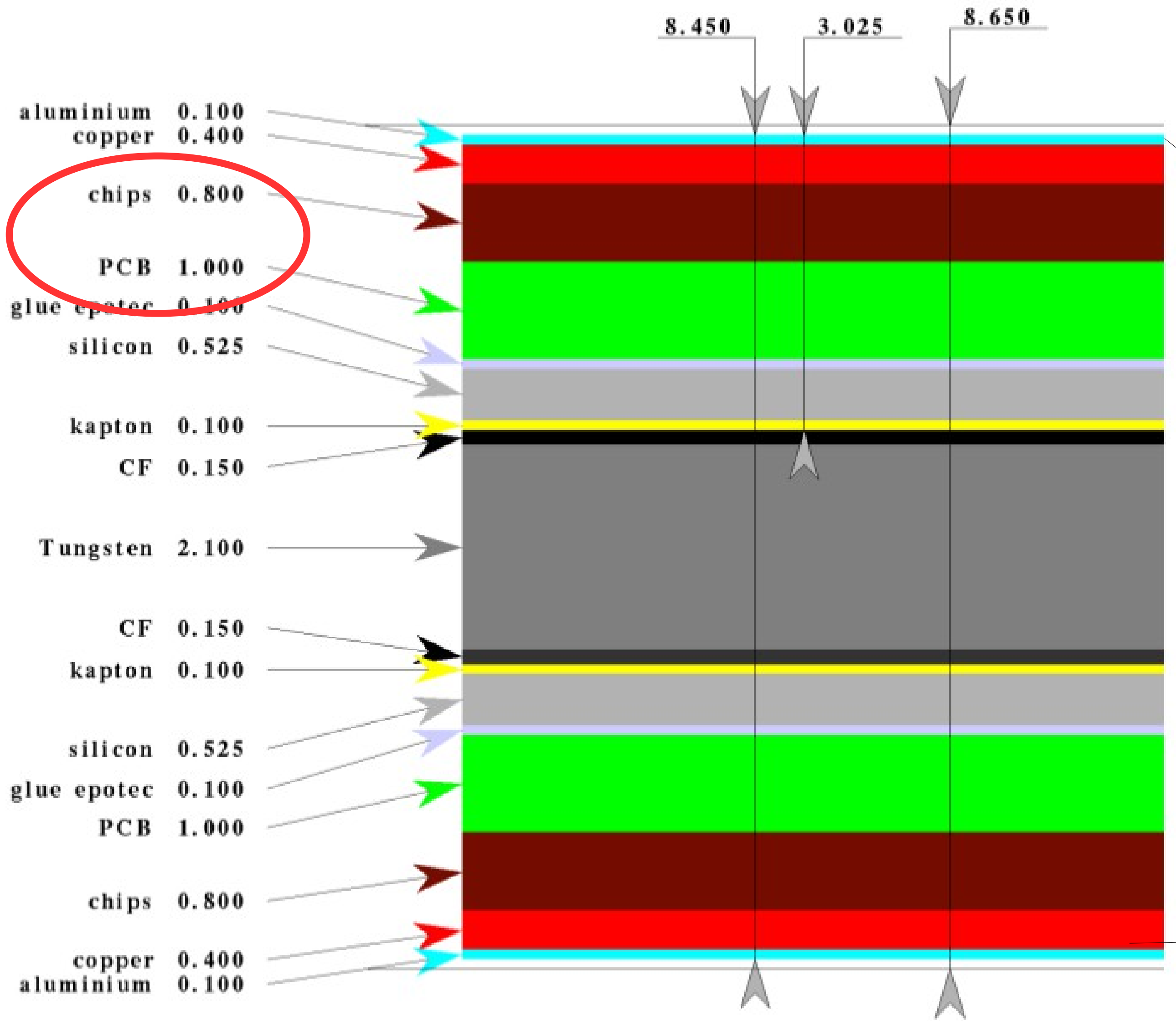
Basic Choices:

- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 at MIP level as design value

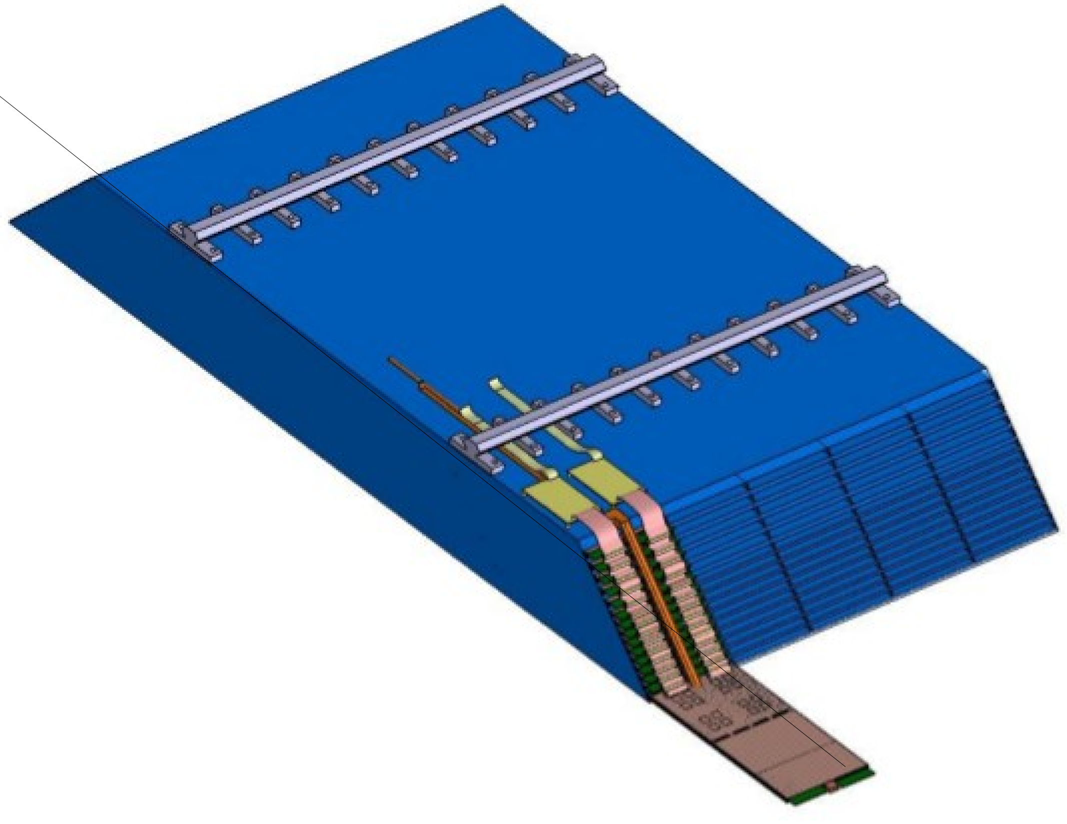
- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

Silicon Tungsten electromagnetic calorimeter

Zoom into layer



Ecal alveolar structure

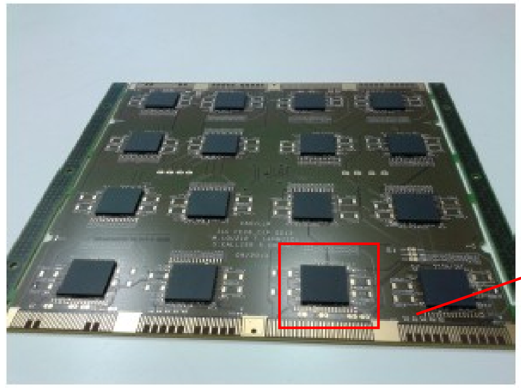


Drawings by Henri Videau for SiW Ecal Technical Design Document

Design: Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)

SiW Ecal – Elements of (long) layer

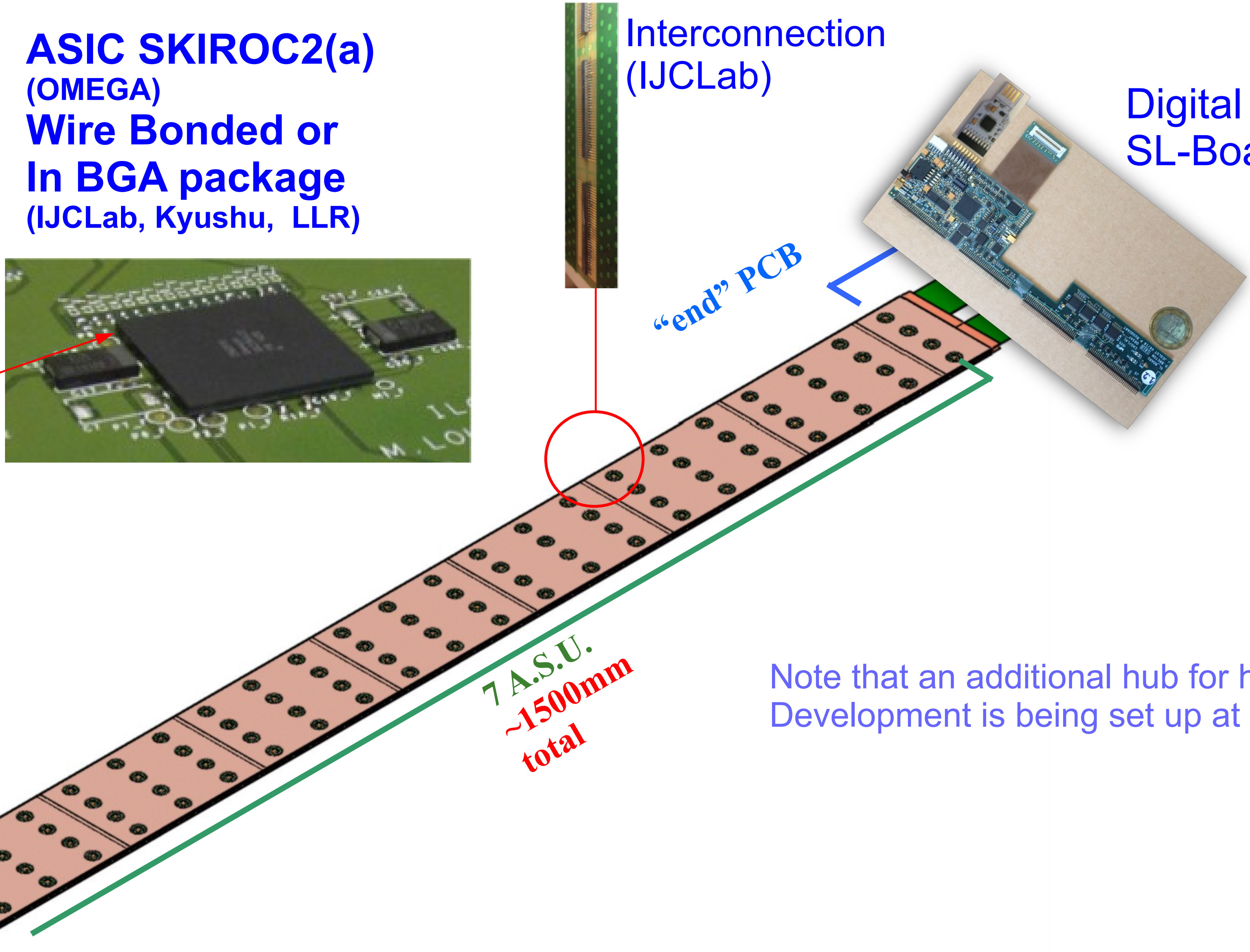
ASIC+PCB+SiWafer
=ASU
Size 18x18 cm²
(IJCLab, Kyushu, OMEGA, LLR, SKKU)



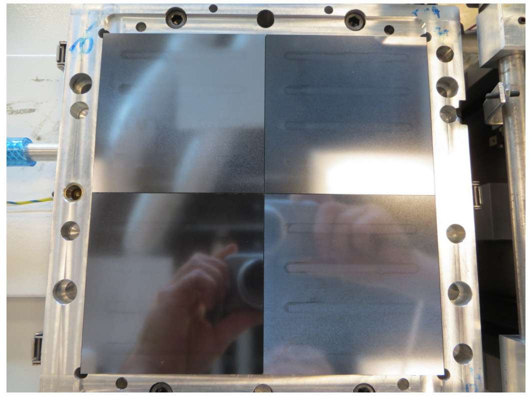
ASIC SKIROC2(a)
(OMEGA)
Wire Bonded or
In BGA package
(IJCLab, Kyushu, LLR)

Interconnection
(IJCLab)

Digital readout
SL-Board (IJCLab)



SiWafers
glued
onto PCB
Pixel size
5.5x5.5 mm²
(LPNHE)



Note that an additional hub for hardware
Development is being set up at IFIC/Valencia

- The beam test set up will consist of a **stack of short layers** consisting of one ASU and a readout card each

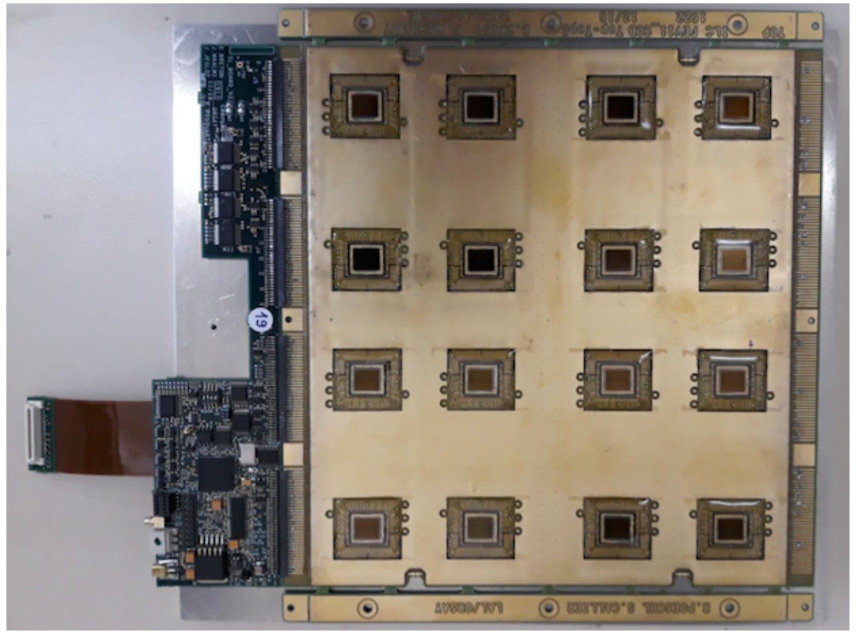
Prologue – “The FEV Zoo”

- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

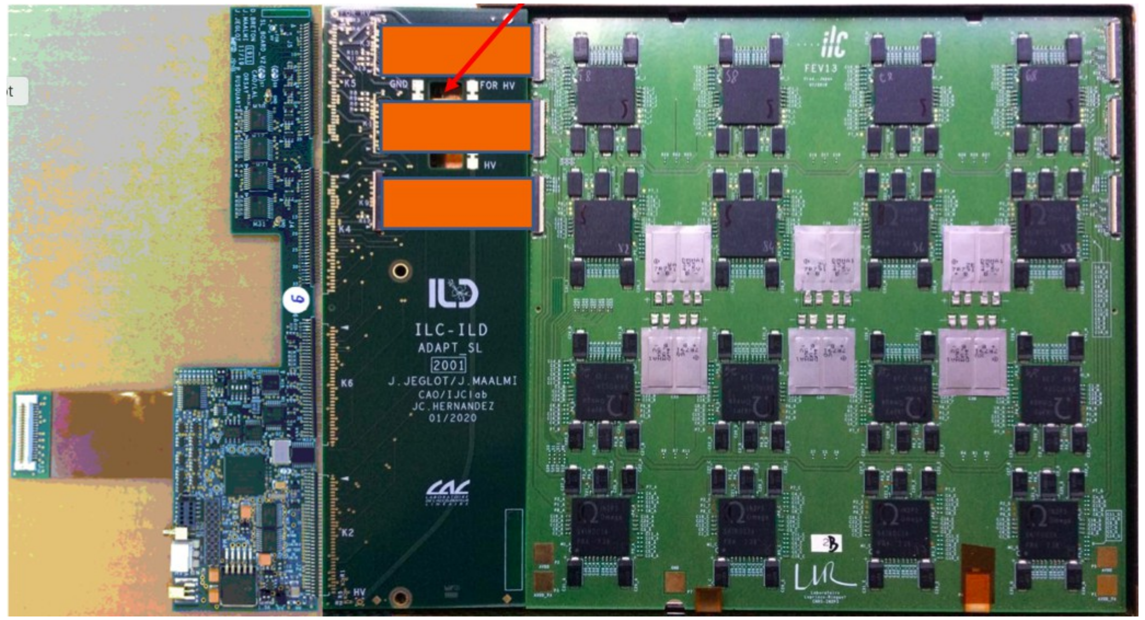
- ASICs in BGA Package
- Incremental modifications From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Current prototype (see later) is equipped with all of these PCBs

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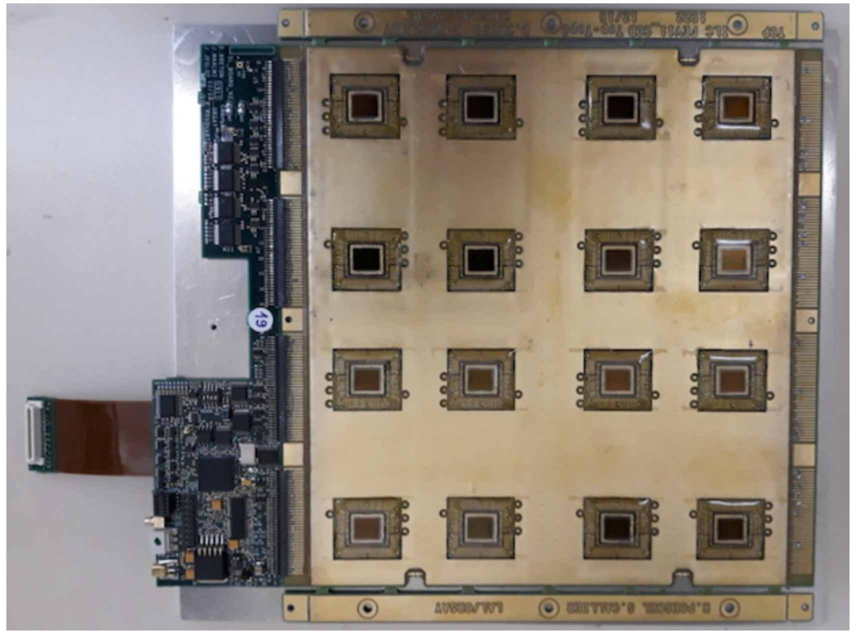

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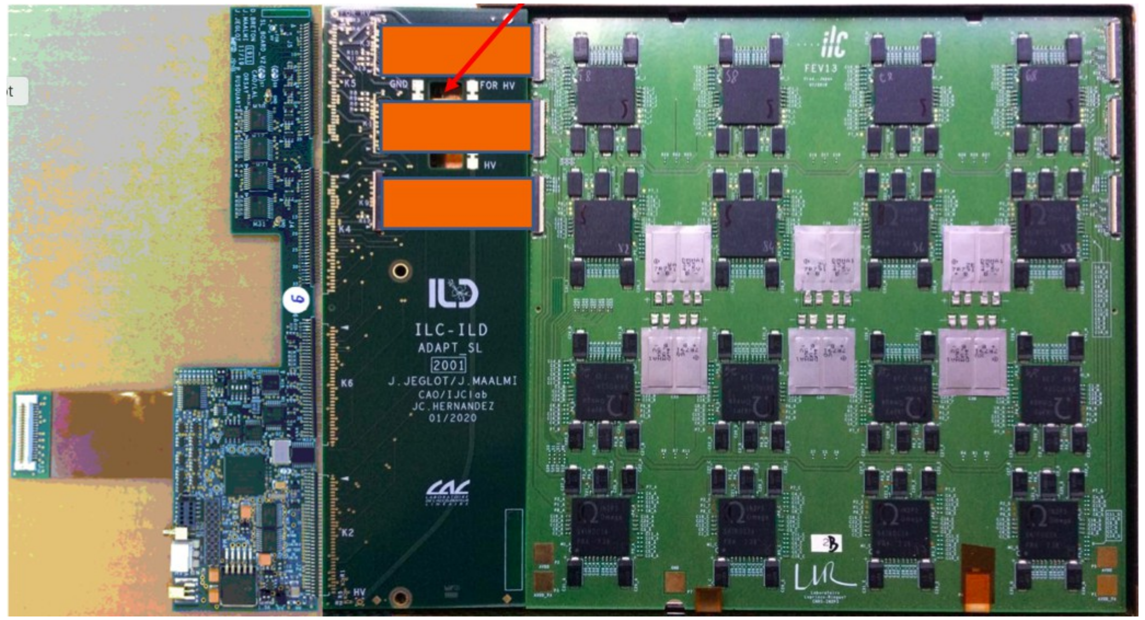

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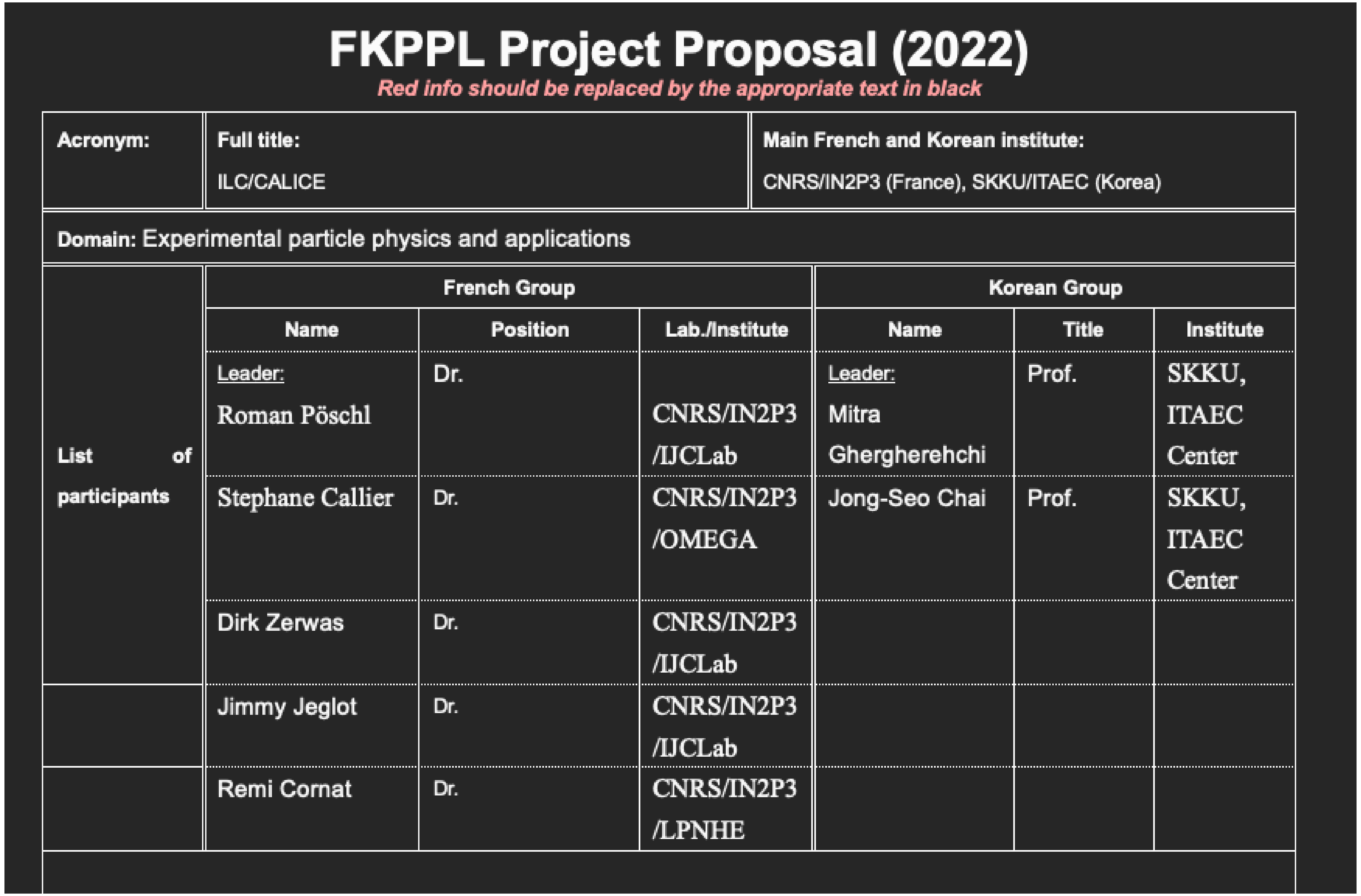
CALICE/FKPPL – The current team



FKPPL Project Proposal (2022)

Red info should be replaced by the appropriate text in black

Acronym:	**Full title:**	**Main French and Korean institute:**
	ILC/CALICE	CNRS/IN2P3 (France), SKKU/ITAEC (Korea)

Domain: Experimental particle physics and applications

	French Group			Korean Group		
	Name	**Position**	**Lab./Institute**	**Name**	**Title**	**Institute**
List of participants	Leader: Roman Pöschl	Dr.	CNRS/IN2P3 /IJCLab	Leader: Mitra Ghergherehchi	Prof.	SKKU, ITAEC Center
	Stephane Callier	Dr.	CNRS/IN2P3 /OMEGA	Jong-Seo Chai	Prof.	SKKU, ITAEC Center
	Dirk Zerwas	Dr.	CNRS/IN2P3 /IJCLab			
	Jimmy Jeglot	Dr.	CNRS/IN2P3 /IJCLab			
	Remi Cornat	Dr.	CNRS/IN2P3 /LPNHE			

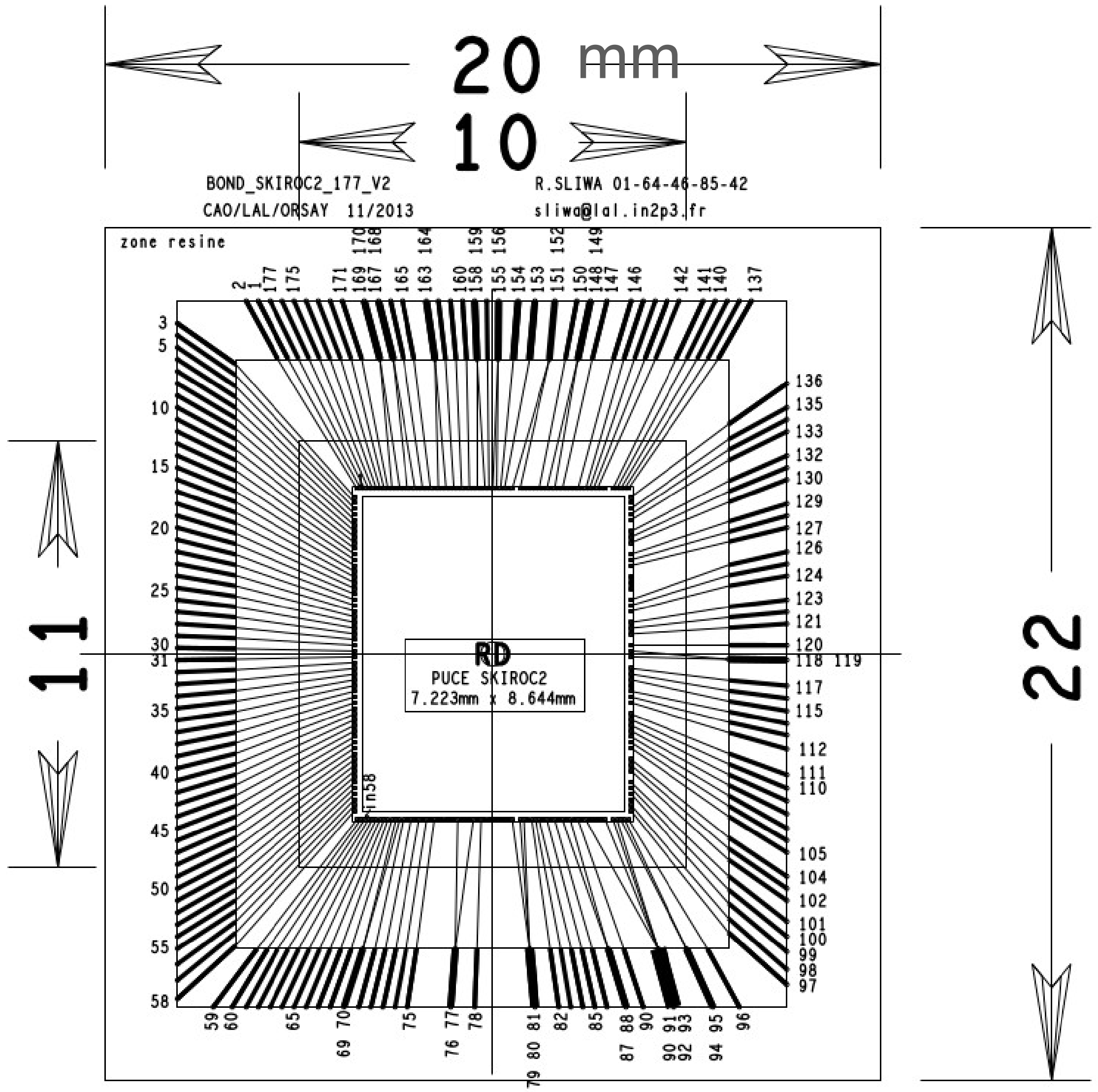
The CALICE SiW ECAL receives aleo great support via TYL/ FJPPL

More information in talk by Cristina on Wednesday morning

+ Yuichi Okugawa (IJCLab and Tohoku U)
Allow me to add Adrian Irles (member until 2020, now IFIC) w/o whom many of the results shown today would not have been possible

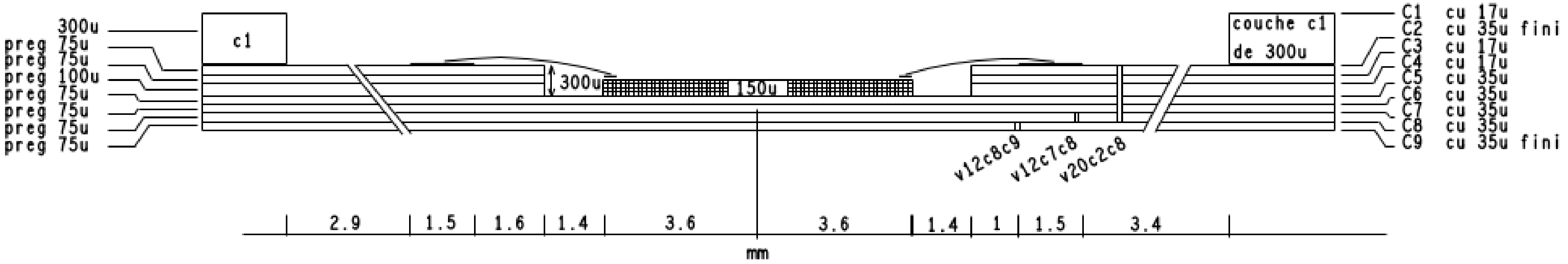
FEV11_COB – Some Technical Details

Bonding scheme



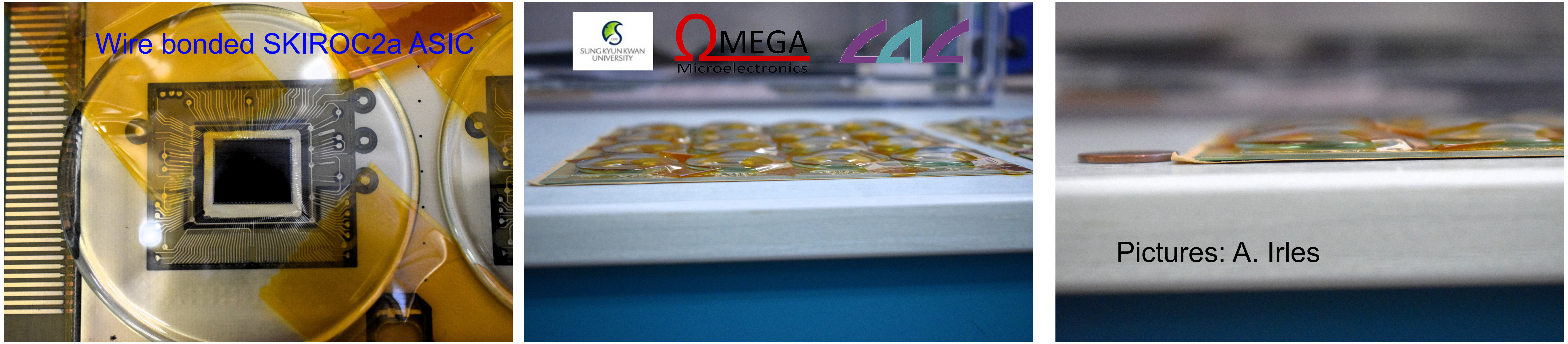
- ~177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings

Side view



- 9+2 layers board
- Overall height ~1.2mm
- ASICs buried in cavities to ensure overall flatness
  - Need to make sure that bonding wires don't pass board surface

FEV_COB – A bit of history



Pictures: A. Irles

- **Produced by EOS Company in South-Korea under supervision by SKKU**
  - European producers failed or refused to produce this kind of board
  - Let me point out the excellent communication with the company, they really cared!!!!

- Height 1.2mm
  - Thin multilayer board => Thermal stress during board production => Planarity was an issue

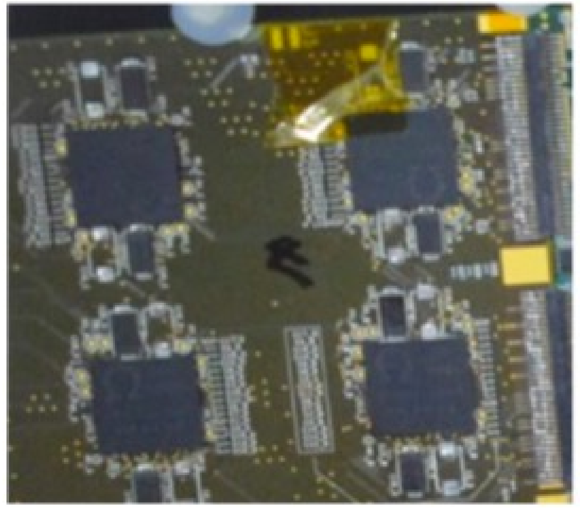
- Series of boards delivered at the beginning of 2018

- Planarity within specs for 80% of the boards
  - Less than 0.5mm bending after production
  - Planarity important for wafers gluing
  - Boards well rectangular

- First beam test in Summer 2019 with two boards (after many years of development)
- Only one wafer per board
- Full equipement for beam tests 2022

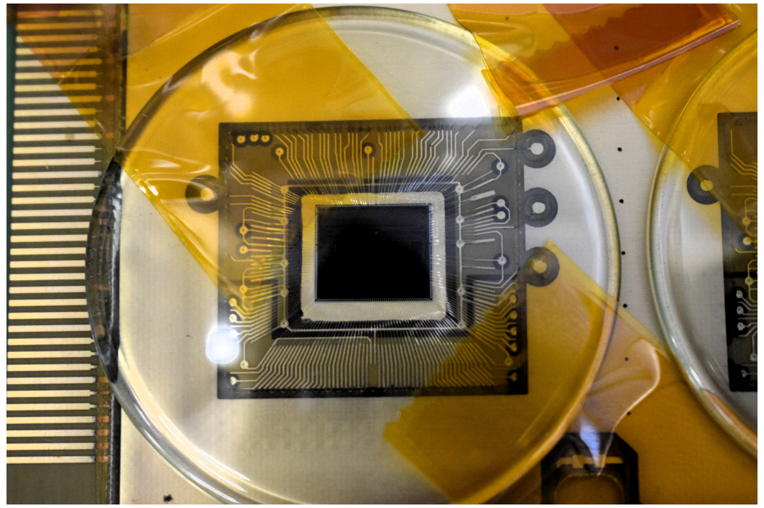
FEV11_COB – Particularities

BGA-type PCB feature
decoupling capacitances



- FEV12/11/13 At least two cap (120 and 150uF) per chip

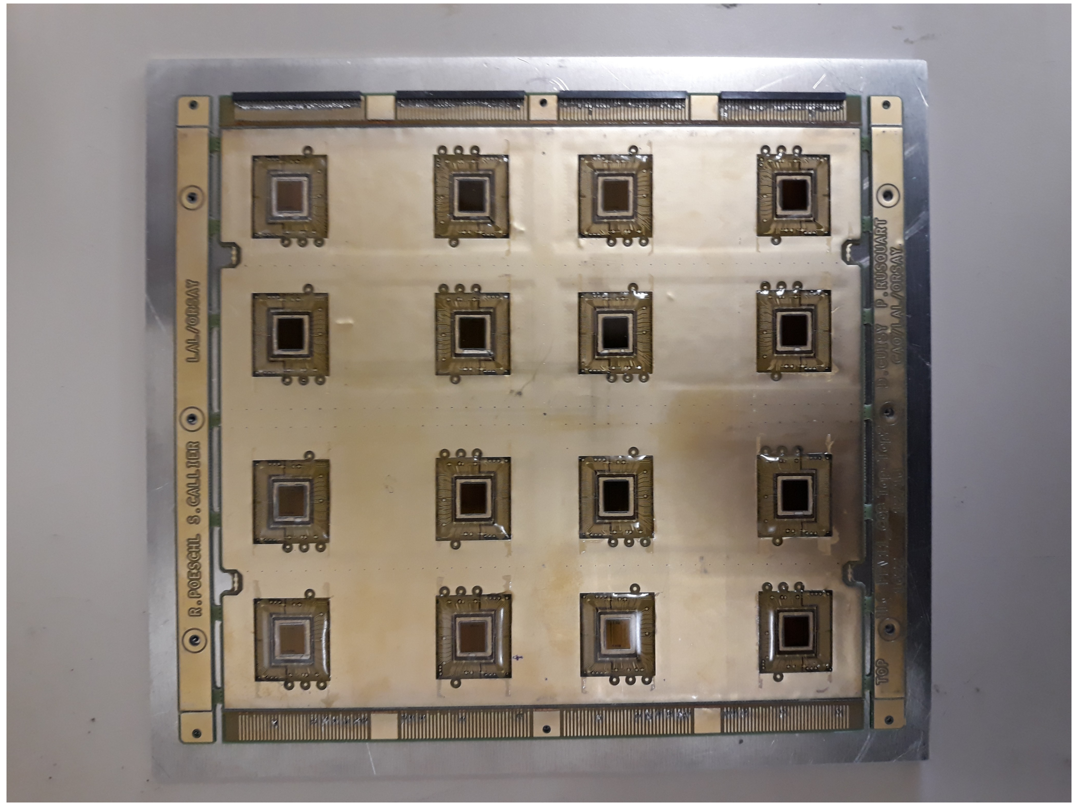
In first place COB does
not feature decoupling capacitances



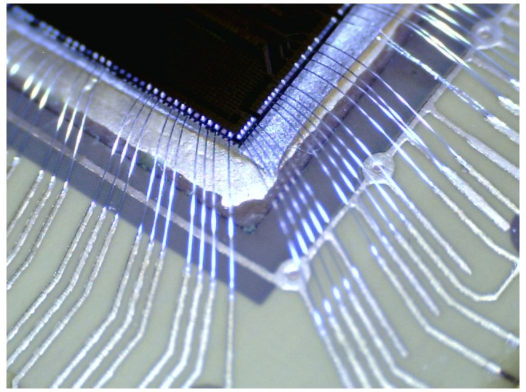
- The Ecal layers will measure signals down to the MIP level
  - i.e. as small as 4 fC
- An ASU comprises 1024 cells
  - => dense board with many noise sources
- We had to equip the board with a minimal set of decoupling capacitances (not shown)
  - This first version of the board teaches us how many are really needed
  - In future versions capacitances could be added to the ASIC cavities
  - Challenging but possible

Encapsulation of ASICs

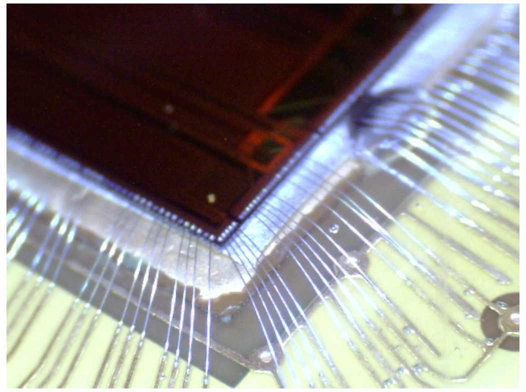
ASICs on COB have to be protected



- Catastrophy during encapsulation with GlobTop at private company
  - Curing at 160° over several hours
    => Deformation of boards, delamination of wafers
- Successful “in house” application of Epoxy (Loctite Hysol) on several boards
  - A masterpiece of work!
- No degradation of performance observed
  - e.g. no ASIC damage, ASICs fully operational after encapsulation
  - Well, 1/48 didn't work properly after encapsulation but not sure whether it's due to encapsulation
- Cooperation with Henkel/Loctite envisaged but interrupted due to pandemic
  - Still, NDA ready on CNRS side (thanks to services at IJCLab and CNRS-DR4)

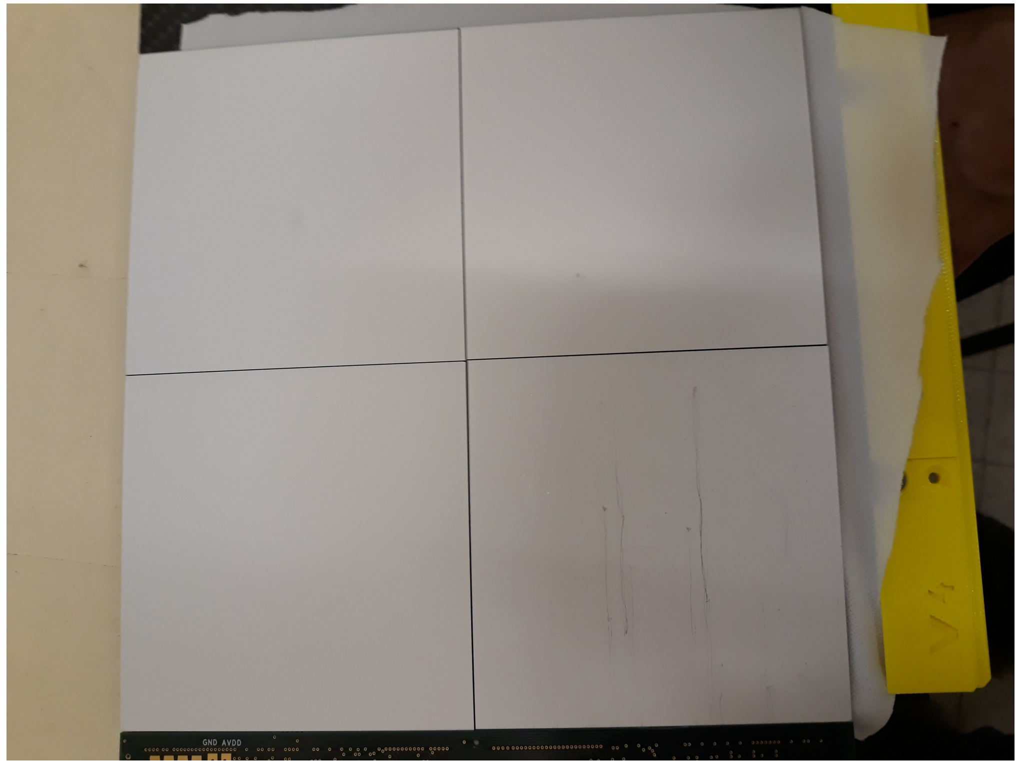


Before application of epoxy



After application of epoxy

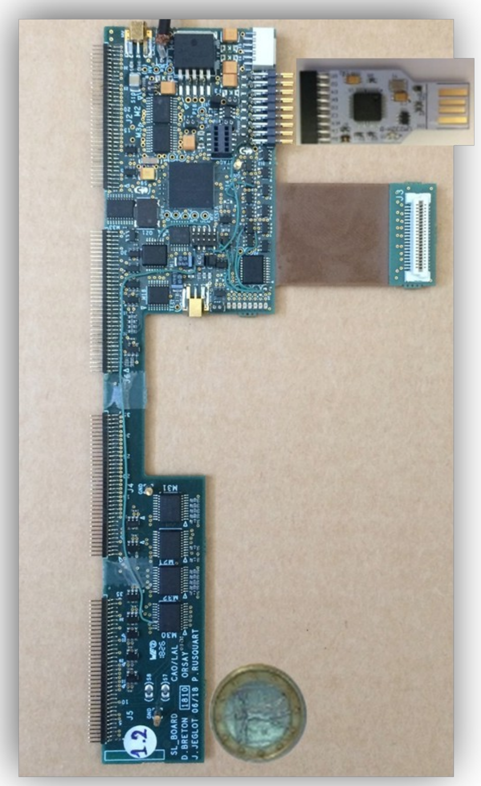
Gluing wafers onto COBs

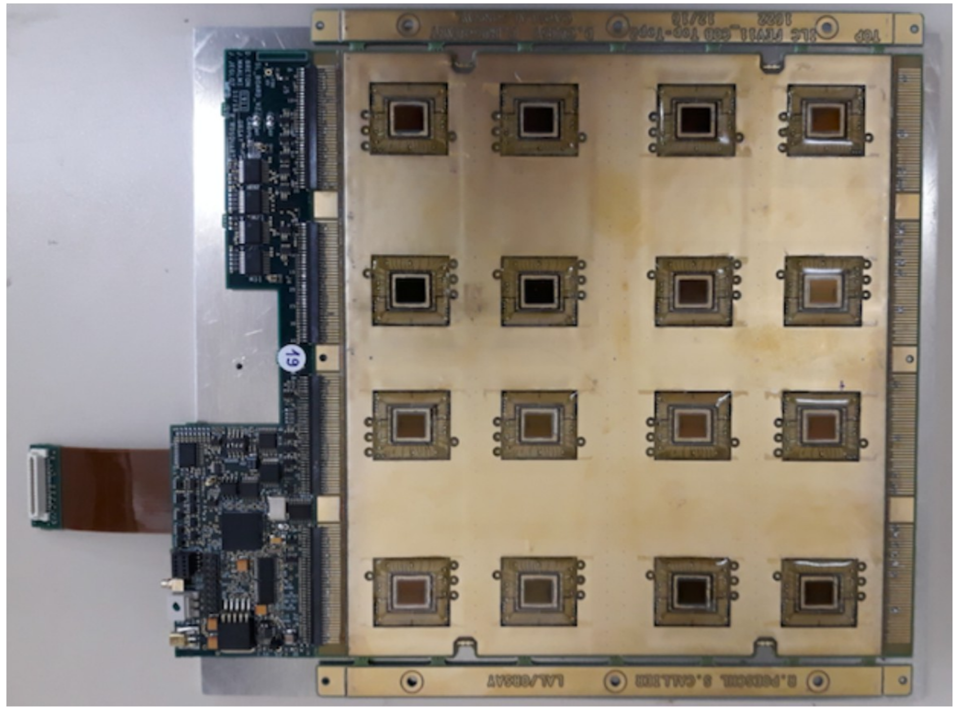


- Wafer gluing at LPNHE
- Since a decade it was a concern whether wafers could be glued on COBs due to potential deformations of thin, complex board
- Gluing of one wafer already in 2019
- Gluing of four wafers onto two boards during winter 2021/22

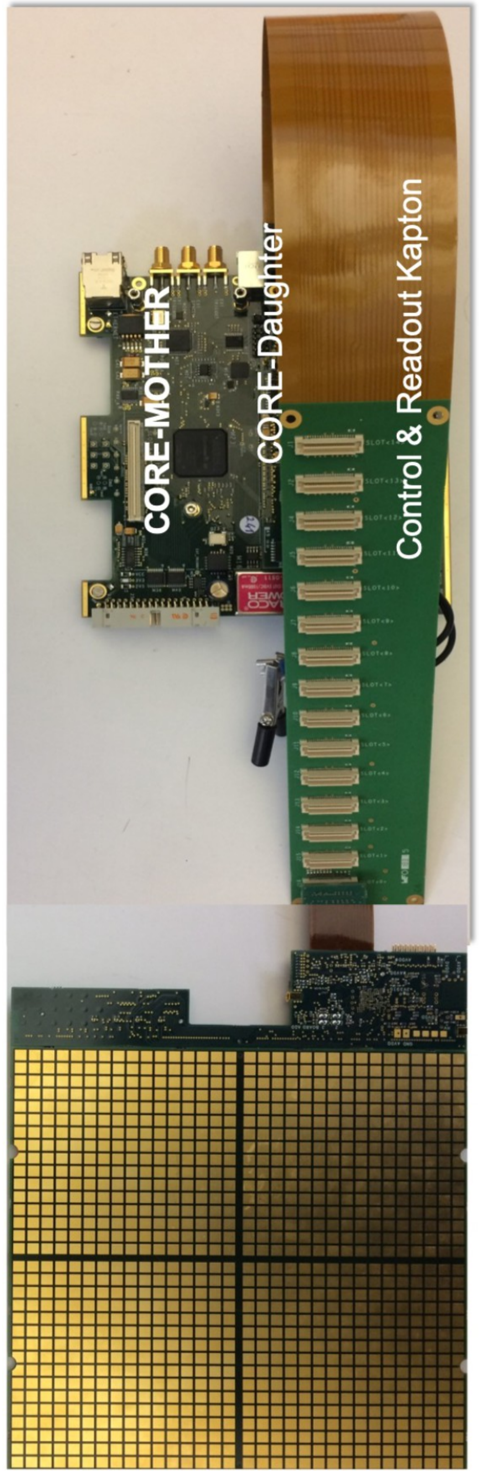
Gluing wafers onto COBs

Current detector interface card (SL Board) connected to COB





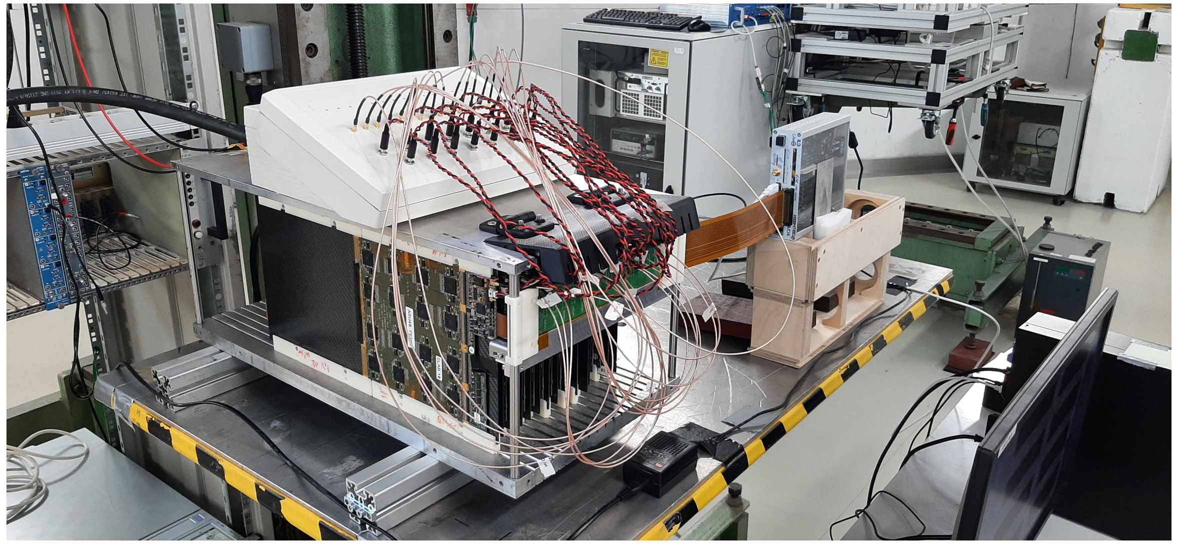
Complete readout system



- “Dead space free” granular calorimeters put tight demands on compactness
- Current developments in CALICE (IJCLab) meet these requirements
- Can be applied/adapted wherever compactness is mandatory
- Components will/did already go through scrutiny phase in beam tests

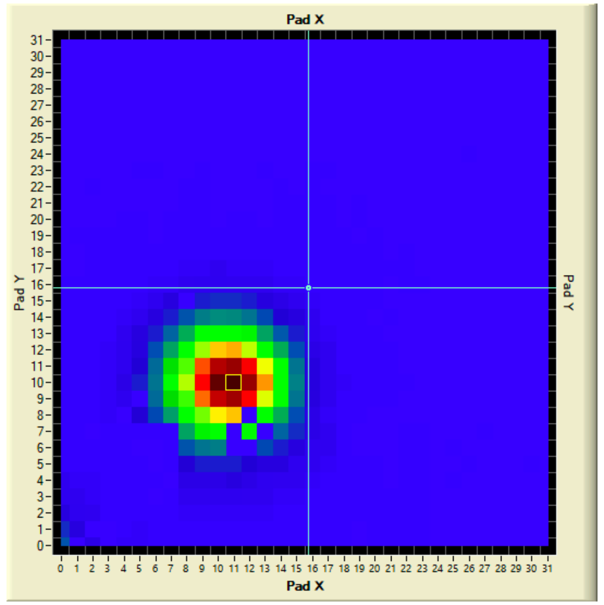
SiW-ECAL in beam test @ DESY

Detector Setup



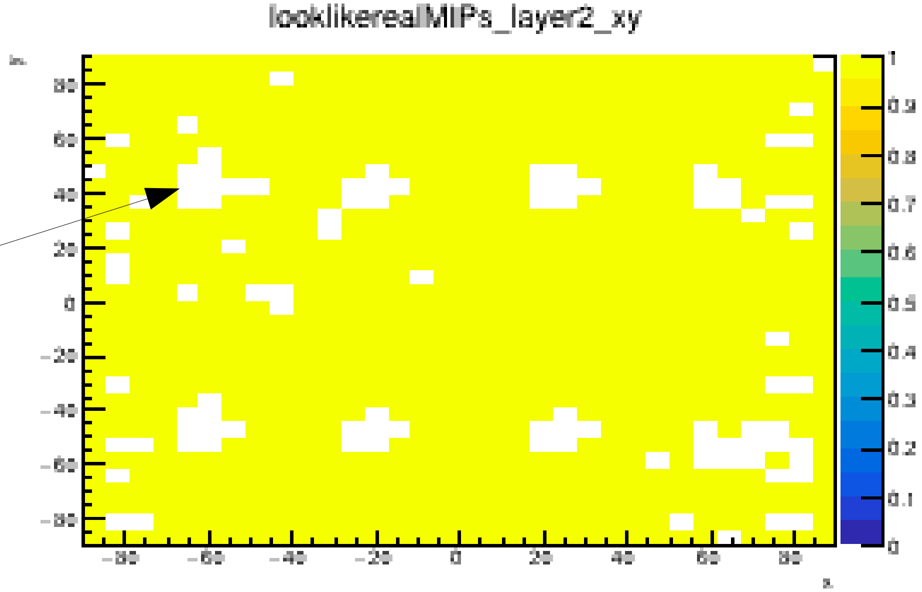
Detector in beam position

- Testbeam with 15 layers equivalent to 15360 cells
- Two COB layers were part of the setup



Clear beam spot in COB based layers

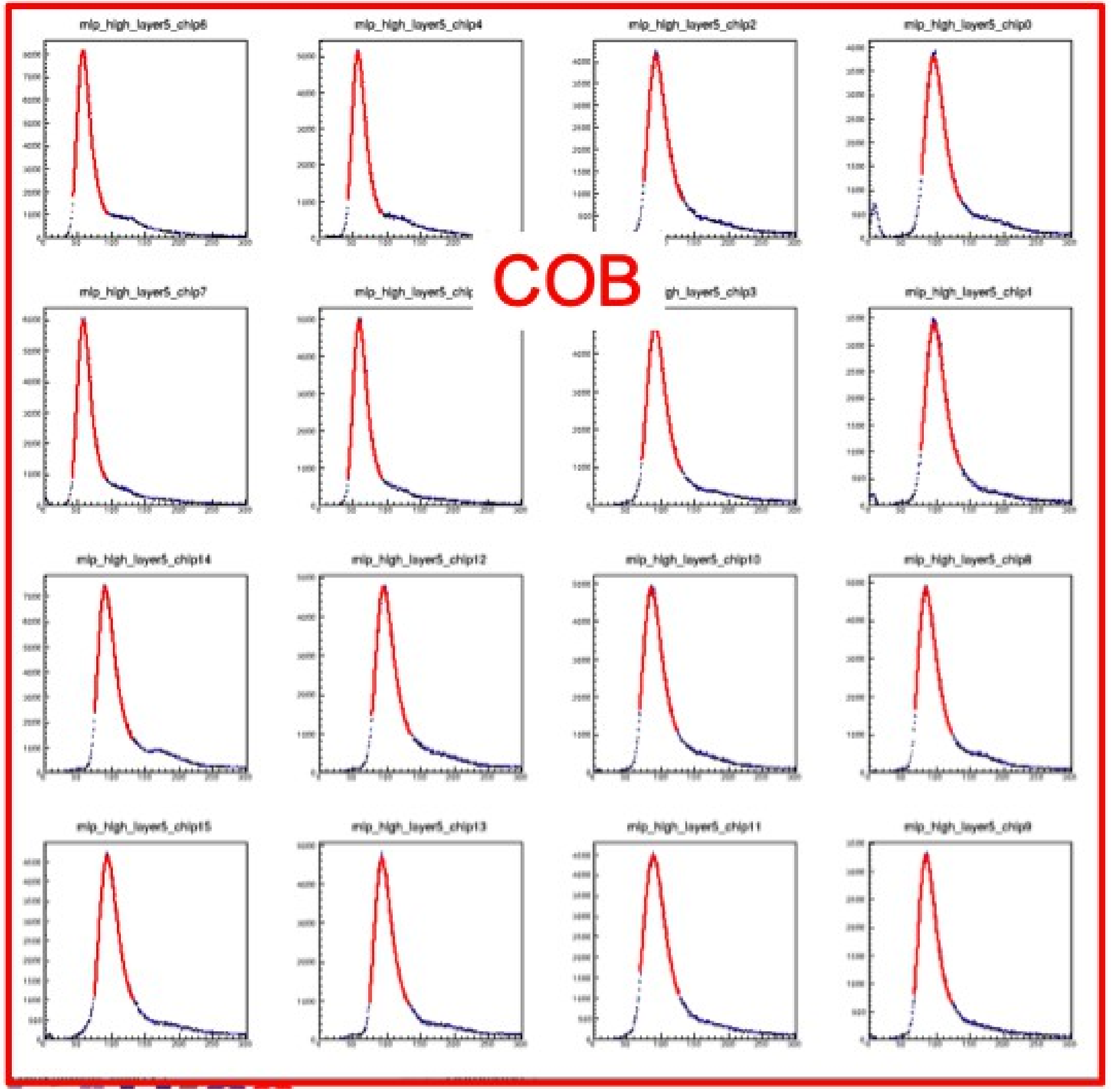
"MIP Map" of one COB

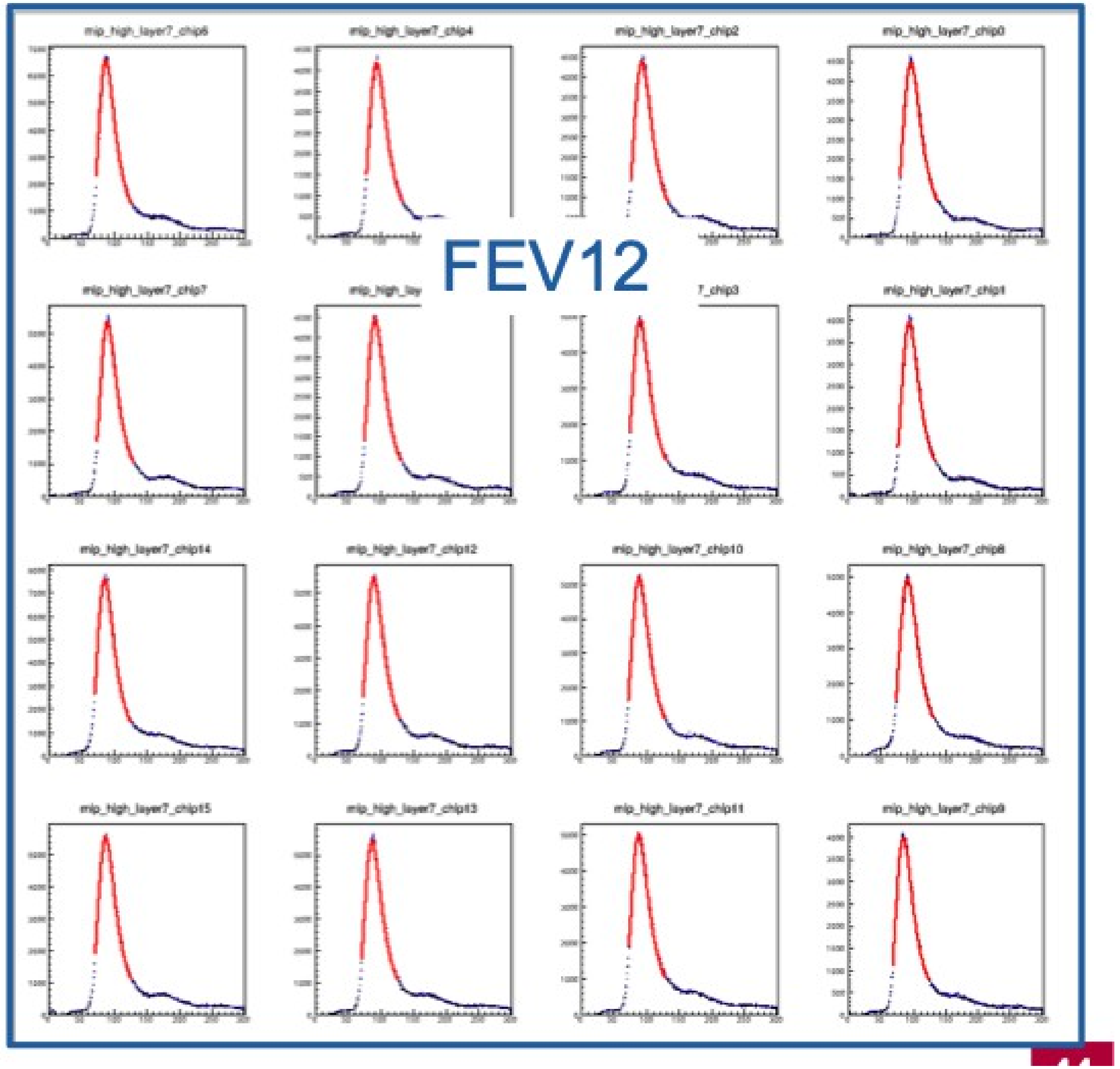


- Homogeneous response of board(s) to MIPs
- ~10% noisy cells had to be masked
  - Nearly all on digital line, curable with decoupling capacitances

Plots by A. Irles, IFIC

MIP Signals - COB vs. BGA

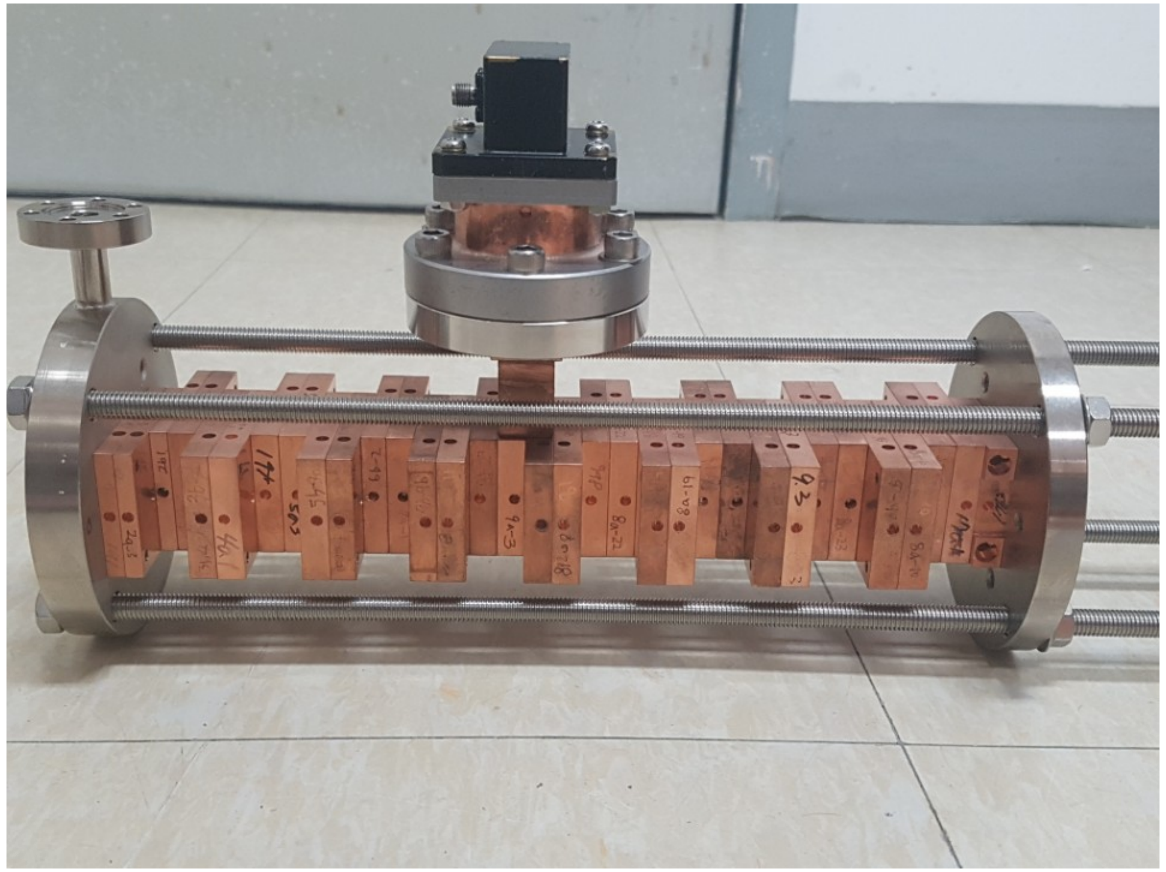




- Quality of MIP signals comparable between COB and BGA variants of PCB

Collaboration ITAEC/SKKU – IJCLab,OMEGA – A new idea

Small S-Band Accelerator for medical purposes
constructed ITAEC/SKKU
5-10 MeV Electrons



~20cm

- Well, this idea is pending since 2018
- Have only since 2019 a first working version of the COB
  - With one Si sensor only
  - ... and 2020 came the pandeic

- Would like to study whether the accelerator can be be used for detector development

- Electrons would act as MIPs in detector material (5-10 MeV is close to typical critical energy of detector materials)

Advantages:

- Higher rates than cosmics
- (Might) be better controllable than sources

Issues to be addressed:

- Control of accelerator rate
- Mechanical installation to hold/move detector elements
- For sure a lot of other points including safety aspects

Premises

- Accelerator exists
- FEV11_COB as first “guinea pigs”
- In passing, equipped FEV11_COB can serve ”immediately” for the radiation protection system
  -> Detectors, readout system and analysis tools are at hand

Summary and outlook

- Two fully equipped COB Boards (finally) produced in 2021/22
  - Collaboration IN2P3-SKKU and EOS Company in South-Korea

- First systematic study of Chip-on-Board PCB in beam
  - Flatness good enough for wafers gluing (critical item of R&D)
  - Encouraging results
  - No serious issues discovered
  - Results comparable with those obtained for BGA based PCBs

- The successful beam test in March 2022 concludes the first R&D cycle on the COBs
  - Proof of principle that these PCBs can be built and operated
  - Real R&D success and it was clearly the continuous support by FKPPL that made this success possible!
  - Thank you very much

- Towards new design
  - Integration of decoupling capacitances
  - Adaptation for power pulsing
  - Need to resume discussions with EOS (Korea)
    - Complete interruption due to pandemic
  - New ideas exists but require restart of regular exchange