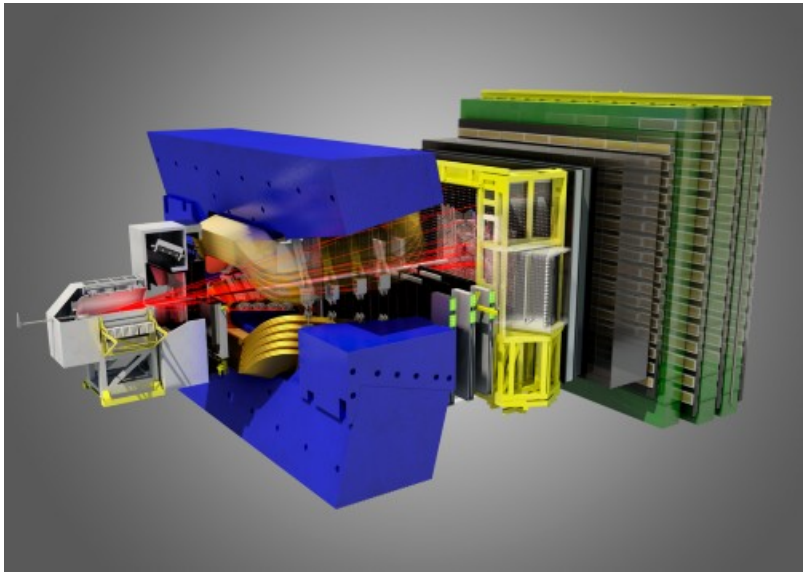
PCIe400 : Project progress

P. Bibron, CPPM

Contents



Current development

Studies done or ongoing :

- Agilex Power supplies
  - Core Power estimations
  - Other Rails Power estimations
  - Power Tree Design
- Clock Tree
- Agilex configuration study

Firmware :

- Slow Control prototype

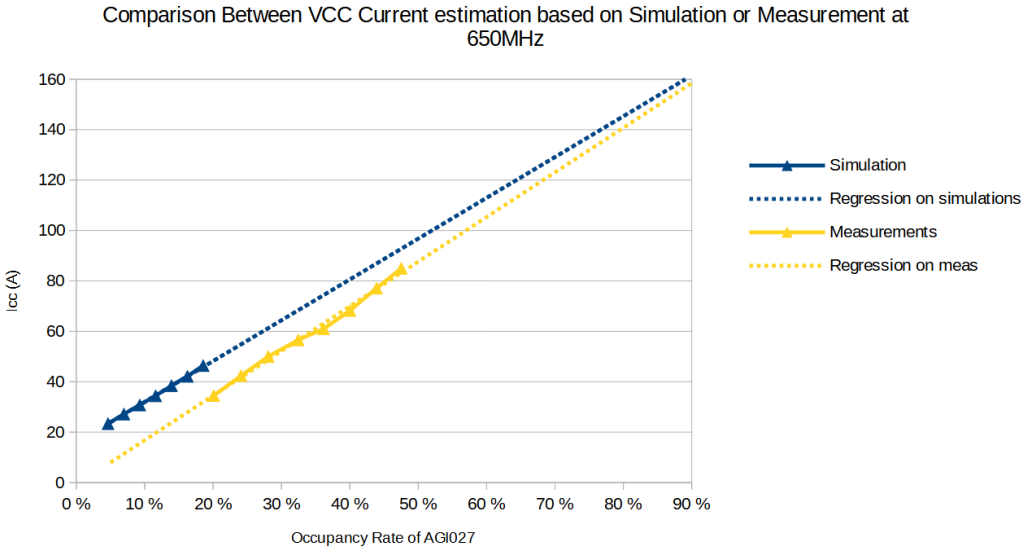
Component procurement

- Most critical components are ordered

Power Supplies estimations

Agilex Core Power Estimations

- Core Power Simulations
  - FPGA Design based on random pattern generators
  - Simulation Post Fit
  - Quartus Power Analyzer (with Thermal Parameters)
  - Realistic estimation of core power
  - Linear, so results can be extrapolated
- Agilex F-Series Development kit measurements confirm simulations
- Applied on Agilex F-Series, but methodology is mastered
  - Can be applied on M-Series (estimation is 240A max for Agilex M-Series 3.9MLEs)
  - Different cooling solutions can be compared



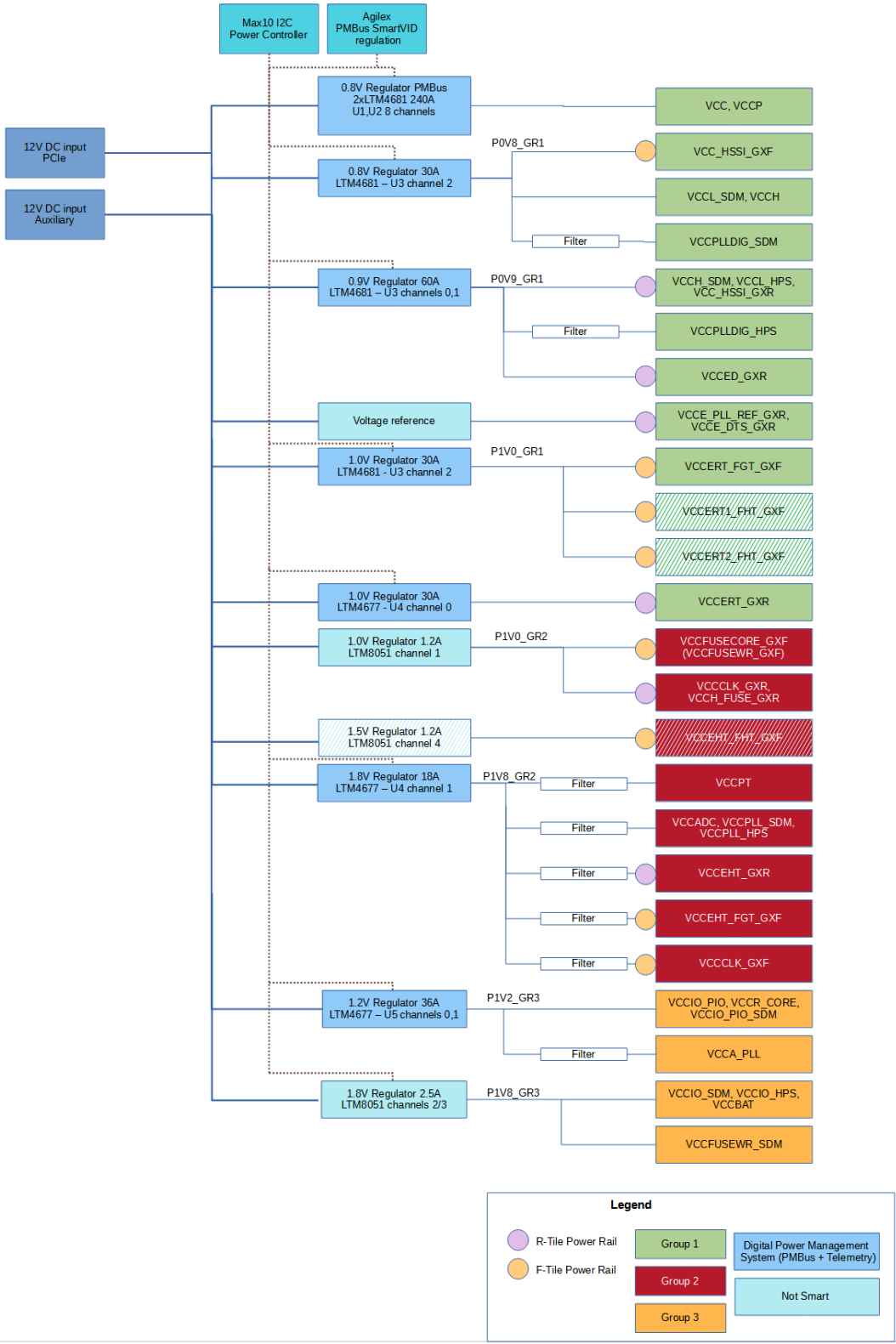
Agilex Power Tree

Agilex FPGA requires :

- 11 Regulators / 24 rails
- Power On Sequencer (3 groups)
- Low ripple voltage / High accuracy (0,5%)

High Power regulators characteristics :

- Digital Power Management (PMBus, Voltage/ Current/Temperature Telemetry)
- Analog Devices (ex Linear) µmodules chosen
  - Low Surface
  - Easy to simulate & implement
  - Expensive but easy to find
- One supplier, easier for firmware development
- Only 3 references for the whole Agilex Power Tree
- Similar approach for the peripheral power supplies



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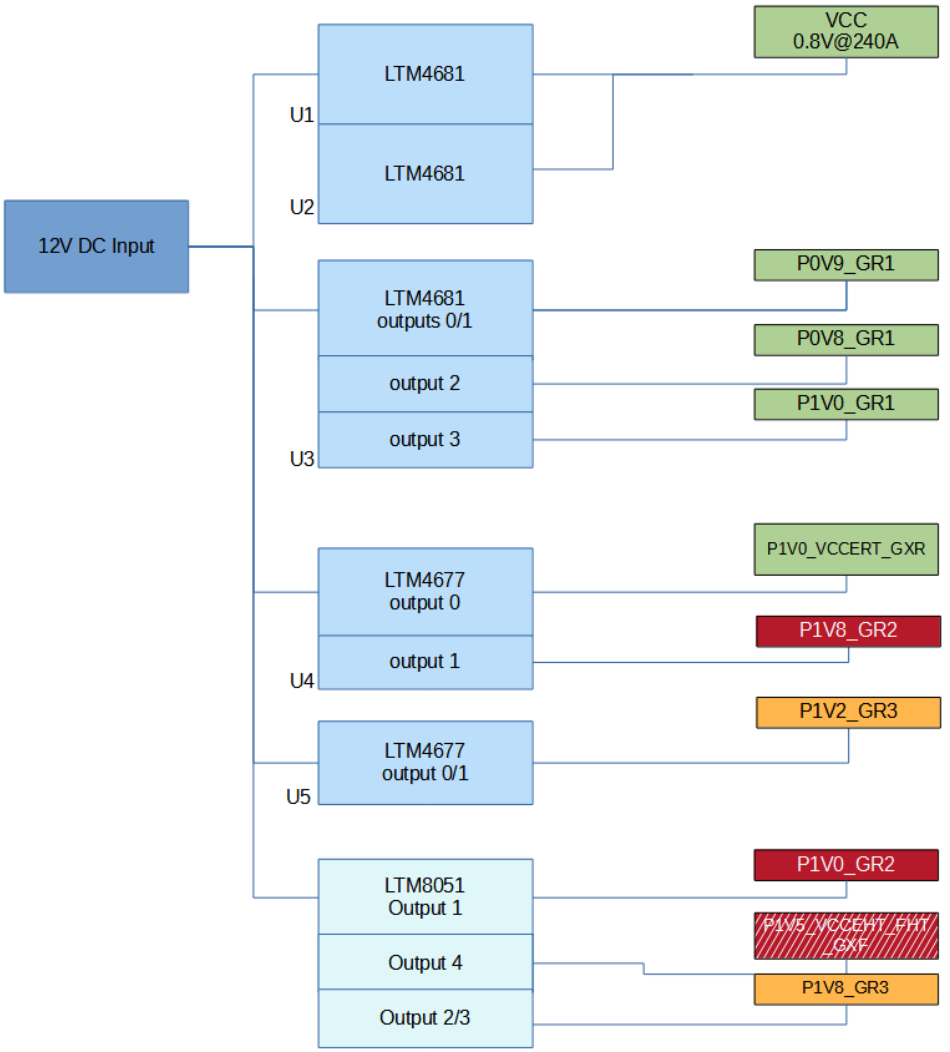


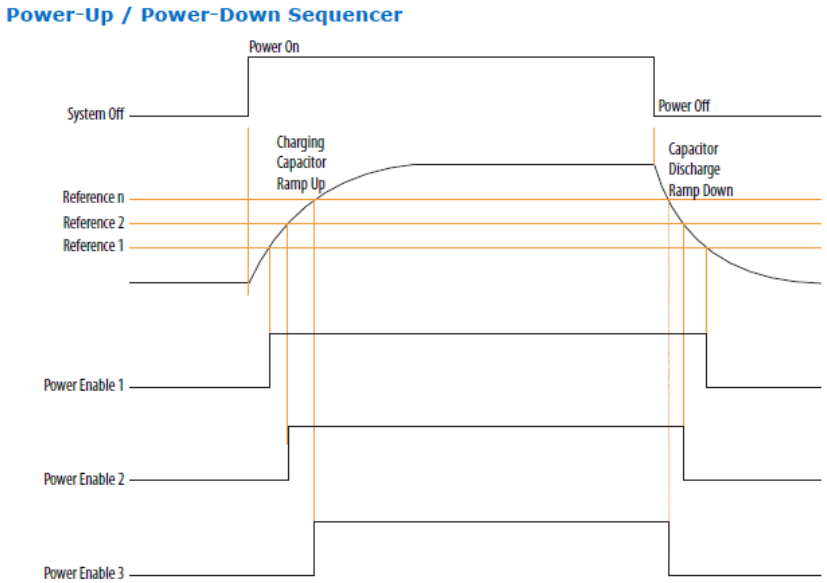
Hardware schematics progress

Hardware Tools and environment

- Started on Concept HDL
- Migration on System Capture is planned
- Part creation on IN2P3 database

Schematics done :

- Agilex Power Supplies
- Voltage rail sequencer (Max10 FPGA)
- USB Blaster (Max10 FPGA)



Foreseen development

Short term development at CPPM

- Power supplies
  - Peripheral Power Supplies
  - Power delivery network
  - Power integrity simulations
    - Stackup dimensioning (Thickness, number of layers)
  - Power Sequencer

- Serial links
  - 28/56 Gbits/s transmissions
    - Simulations
    - Implementation on Intel devkit I-Series
  - PCIe on R-Tile
    - Implementation on Intel devkit I-Series

Conclusion

Recap

- Architecture almost final
- Schematics ongoing
- Critical studies done or ongoing

Challenges expected

- Long delay for FPGA Pinout (June 2022)
- Component procurement
- White Rabbit implementation
- Stackup
- Cooling