Toward Ultra-Light Vertexing Devices Suited to all FCCee Regimes

(le projet ITS-3 d'ALICE vu depuis les usines à Higgs-top)

M.Winter / 22 Avril 2022

CONTENTS:

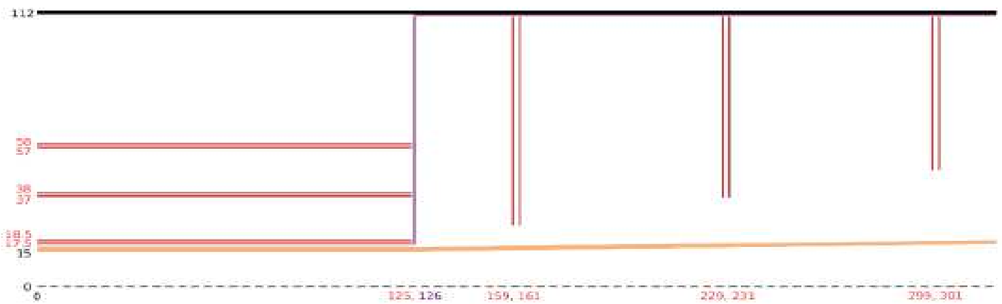
- **How to approach the requirements of a vertex detector suited to FCCee**
  - Hierarchy among the requirements
  - From the Higgs-top energy regime to the Tera-Z regime
- **Practical approach:**
  - Environments supporting R&D serving FCCee vertex detector goals
  - ALICE-ITS3: attractive aspects of its R&D programme
  - CMOS pixel sensors in TJsc 65 nm technology
  - large surface, thin and bent CMOS pixel sensors
- **Summary & Outlook**

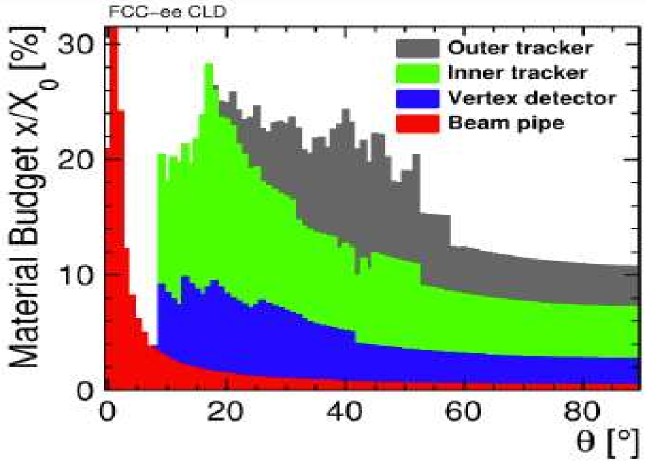
CLD - Vertexing and tracking

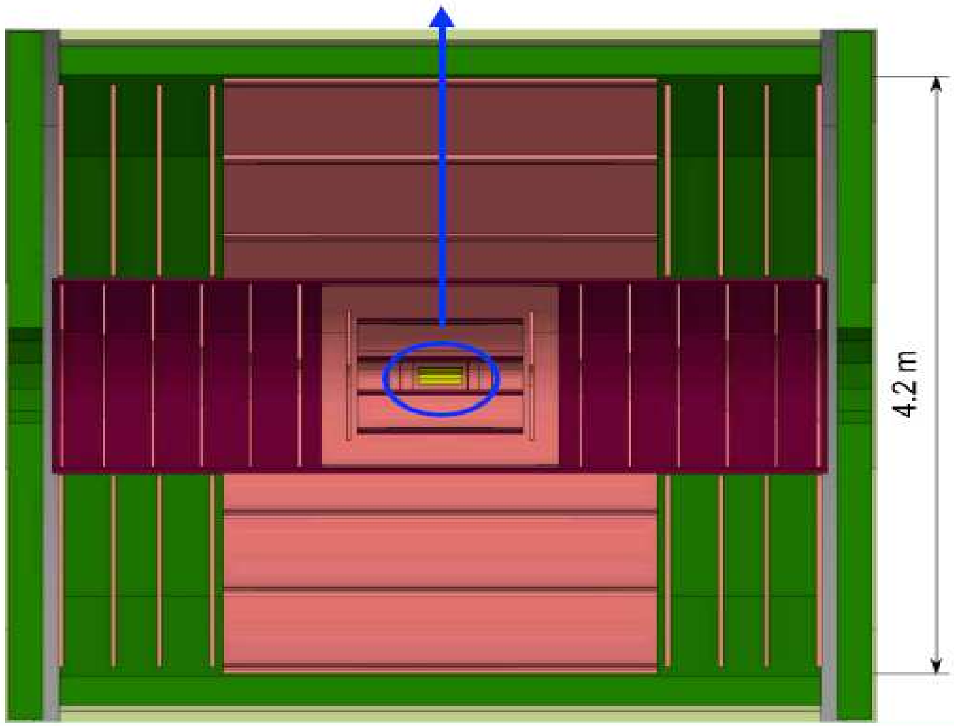
UNIVERSITY OF SUSSEX

VTX:
- Pixel size 25x25 μm² - 50 μm sensor thickness - aiming at 3 μm resolution
- Material and cooling benchmarked on ALICE ITS LS2 upgrade design (MAPS)
- Occupancy dominated by IPC - higher at the Z pole and below 1% (Safety factor 5 - 10 μs readout window)
- Power dissipation: 40 mW/cm² - water cooled

ID:
- Single point resolution 7x90 μm² - 5x5 μm² in 1st layer.
- Inner tracker: Barrel 3 layers, end-cap 7 discs.
- Outer tracker: Barrel 3 layers, end-cap 4 discs.







Vertex Detector Requirements: Time Resolution

- **Expected occupancy vs time stamping:**
  - ⋇ Beam crossing at IP: from every 20 ns (91.2 GeV) to every 3.4 μs (365 GeV)
  - ⋇ N. Bacchetta et al. (CLD - arXiv:1911.12230v3 - 12.12.2019):
    - consider approach of ALICE-ITS2 (ALPIDE sensor): $\approx$ 40 mW/cm^2 (watch hit rate !)
    - assume $\Delta_t \approx$ 10 μs for vertex detector (case of ALICE-ITS2)
    - occupancy (simul x 5, cluster size = 3): from 0.43 % (91.2 GeV) to 0.13 % (365 GeV) $\Rightarrow$ OK
  - ⋇ P. Azzi & E. Perez (Eur. Phys. J. Plus - 30.11.2021 - 136:1195):

    "$\Delta_t <$ 1 μs makes integrated background negligible"

- **ILD vertex detector requirement:**
  - ⋇ $\Delta_t \lesssim$ 1 μs based on CMOS sensors (providing simultaneously required spatial resolution)
  - ⋇ expected occupancy at FCCee (scaled from above):

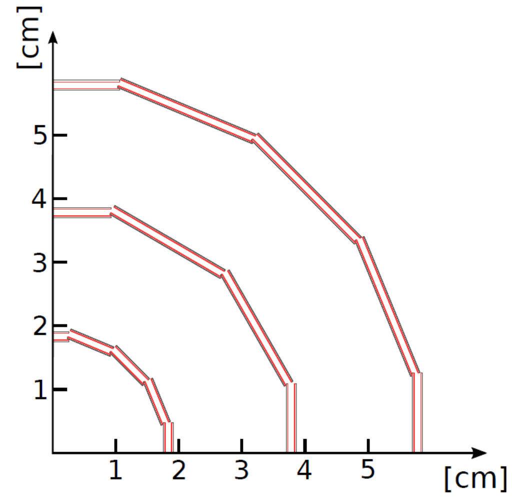
    $\lesssim$ 0.043 % (91.2 GeV) $\longrightarrow$ $\lesssim$ 0.013 % (365 GeV)

$\Rrightarrow$ **no need to push time resolution below $\sim$ 500 ns**

$\hookrightarrow$ **power saving is the priority !**

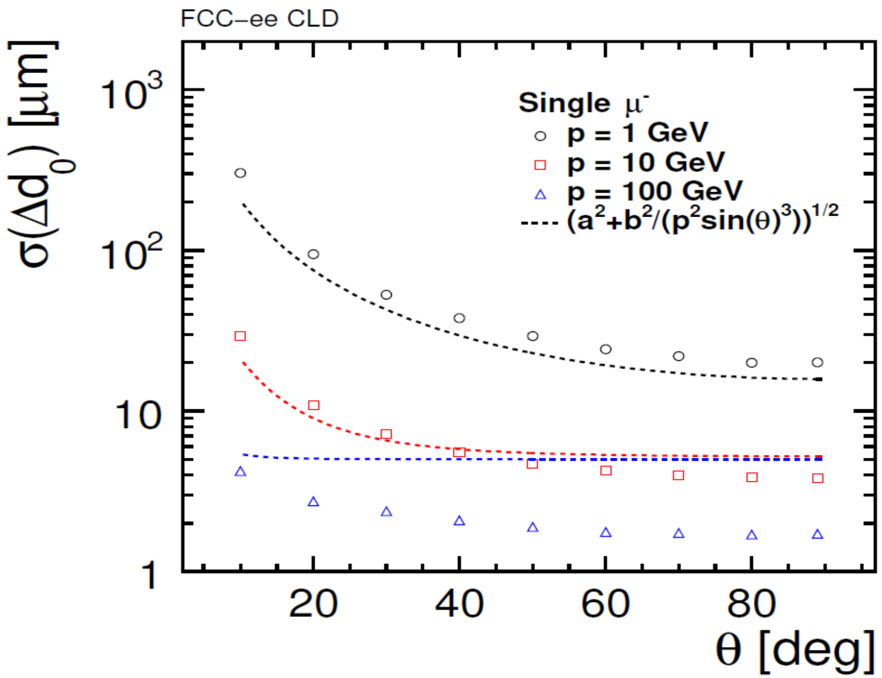
Vertex Detector Requirements: Spatial Resolution (1/2)

- **Vertexing goal:**
  - ⋇ $\sigma(\Delta d_0) \leq a \oplus b/p \cdot sin^{3/2}\theta \;\; \mu m$
    with $a \approx 5$ and $b \approx 10 - 15 GeV \cdot \mu m$
  - ⋇ assume 3 double layers (R ranging from 17.5 to 60 mm) ⟶
  - ⋇ $\sigma^{sp}_{R\phi,Z}$ = 3 μm
  - ⋇ 3 dble-layers with water cooling (≡ ALICE-ITS2)
    ⇛ 0.6 - 0.7 % X_0/dble-layer



- **Beam pipe:**
  - ⋇ dble-shell of Be with water cooling ≡ 0.34 % X_0
  - ⋇ gold coting (5 μm) ≡ 0.15 % X_0

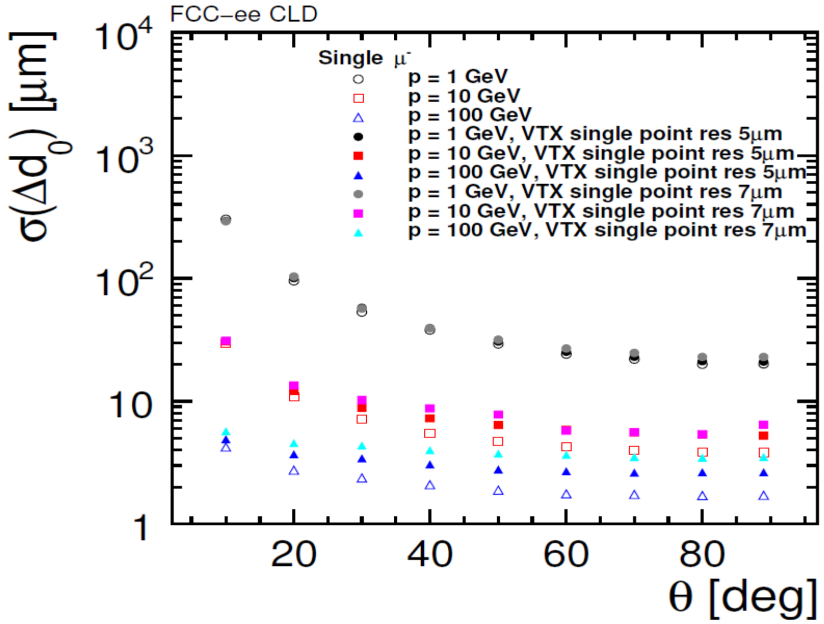
- **ILD VXD & beam pipe material budget:**
  - ⋇ VXD: 0.3 % X_0/dble-layer with air cooling
    (possibility of power pulsing)
  - ⋇ BP: sgle-shell of Be with no cooling ≡ 0.14 % X_0
  - ⇛ b ≃ 10 GeV·μm instead of 15 GeV·μm



(a) d_0 resolution

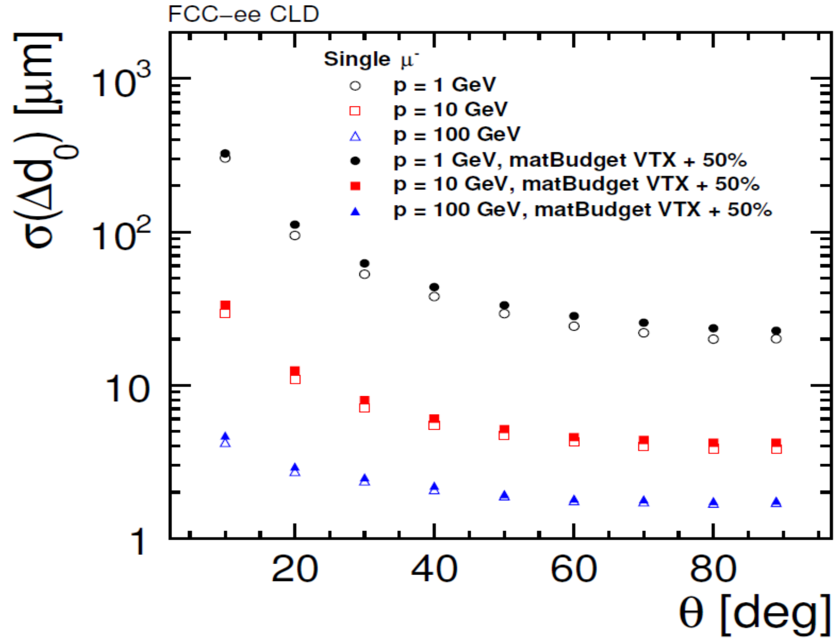
Vertex Detector Requirements: Single Point Resolution (2/2)

- **Impact of relaxed constraint on single point resolution:**
  - ⋇ $\sigma^{sp}_{R\phi,Z}$ = 3 μm $\longrightarrow$ 5 and 7 μm
  - ⋇ dilutes $\sigma(\Delta d_0)$ by up to factor 2



- **Impact of increased dble-layer material budget:**
  - ⋇ add 50 % to dble-layer material budget
  - ⋇ impact is nearly marginal $\Rrightarrow$ impact $<$ 1 GeV/c ?

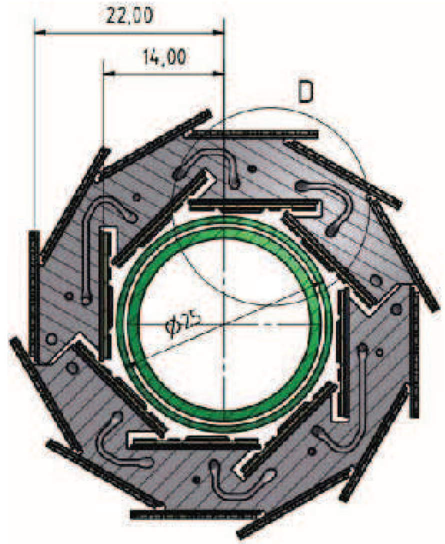
    What if mat. budget would be twice less ?

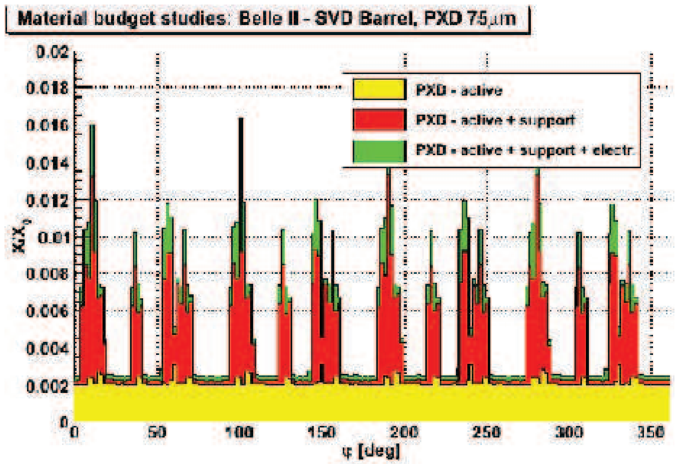


(a) d_0 resolution

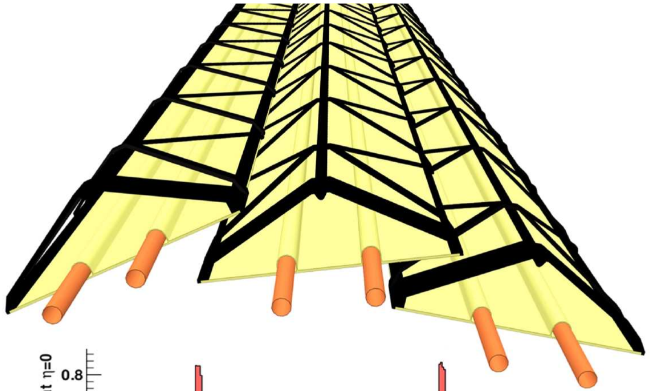
Major R&D Goal in Coming Years: Material Budget Reduction

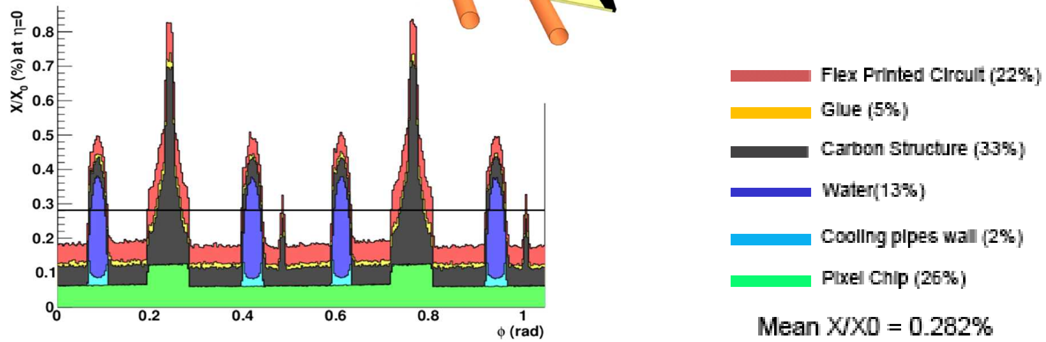
- Physics perfo. limited by material budget of services & overlaps of neighbouring modules/ladders





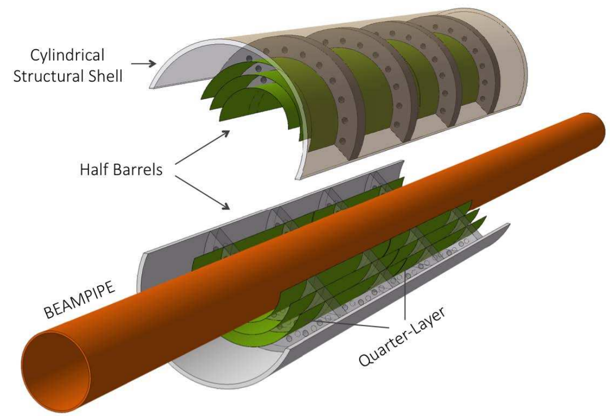
BELLE-II PXD





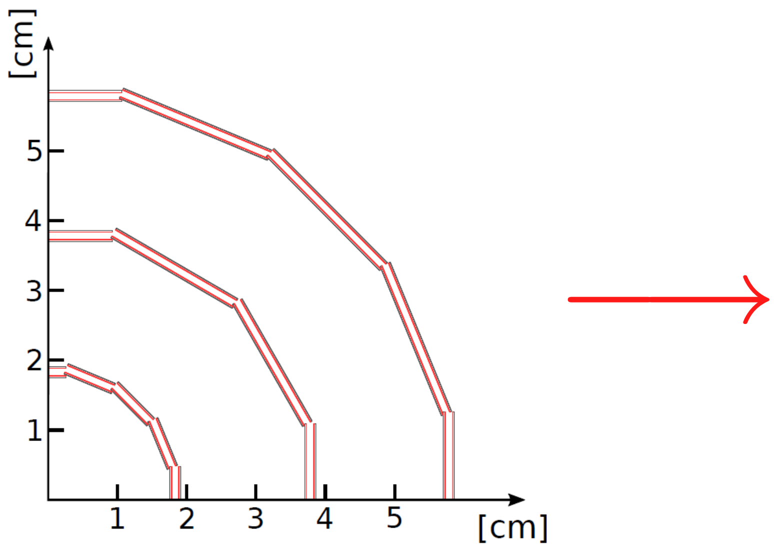
ALICE-ITS

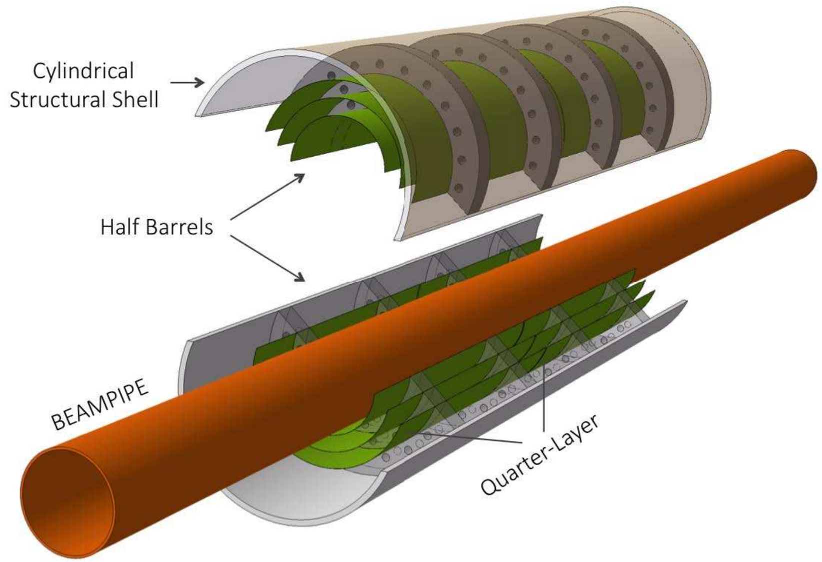
- Contribution of sensors to total material budget of vertex detector layer is modest: 15 - 30%
- **R&D objective beyond "classical" concepts:**
  - Innermost layer: try stitched & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process
  - Concept with minimised mechanical support (e.g. using beam pipe) See Talk of M. Mager at Vertex-19, Lopud Island, Oct.'19



Aiming at Improved Physics Performances w.r.t. State-of-the-Art

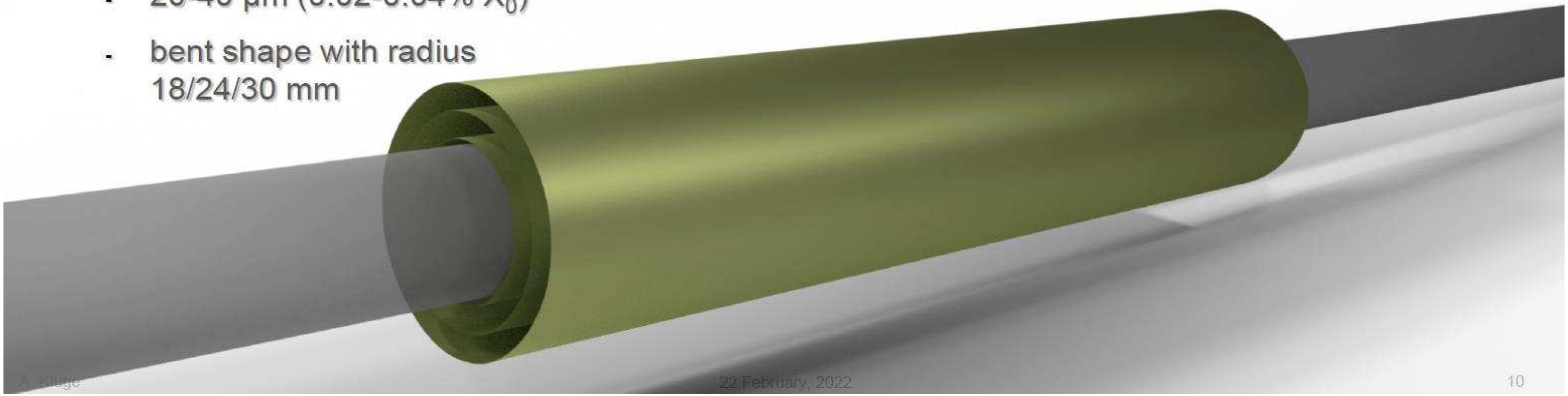
- Revisit globally usual vertex detector concepts in ordre to suppress its material budget and improve the spatial resolution toward the ambitionned 3 μm
- **Join R&D effort of ALICE-ITS3 project**, associated to W.P.-1.2 of CERN-EP R&D programme (despite some modest ambitioned performances: 5 μm and 10 μs)
- Unique occasion to develop stitched (curved) pixel sensors in a 65 nm technology (cost !) and a novel integration concept optimised for material budget suppression





ITS3 specifications & layout

- **Concept**
  - **replace inner 3 layers of ITS2 with ITS3**
  - 280 mm long sensor ASICs
  - out of 300 mm long stitched wafers
  - 20-40 µm (0.02-0.04% X_0)
  - bent shape with radius 18/24/30 mm
  - carbon foam rib to hold ASICs in place
  - air cooling
  - homogenous material distribution
- **6 sensor ASICs**
  - **2 halves * 3 layers**



from A. Kluge - VCI 2022

Which questions need to be answered?

- **Idea**
  - **remove all but the silicon sensor ASIC and**
  - **bend it around beam pipe**

    for increased performance and mechanical stability
- **Questions**
  - **Can thin silicon be bent without breaking?**
  - **Are bent silicon sensor ASICs functional?**
  - **Can long, thinned silicon sensors be integrated without a heavy CF structure?**
  - **Can the sensor be cooled with air only efficiently?**
  - **Can a 280 mm long silicon sensor ASIC be produced?**
  - **Can the sensors be connected without additional HDI?**

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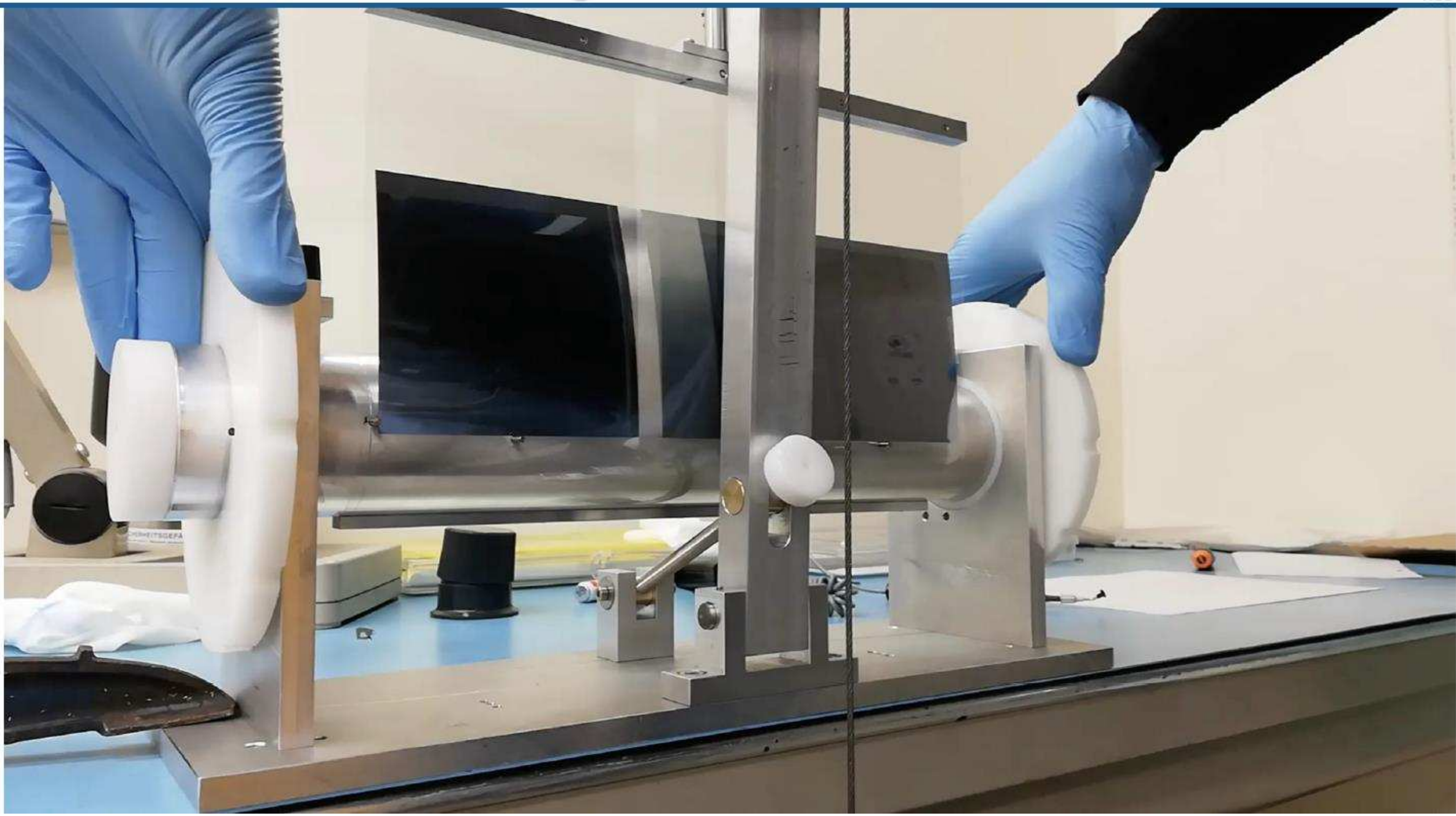
Bending wafer scale silicon



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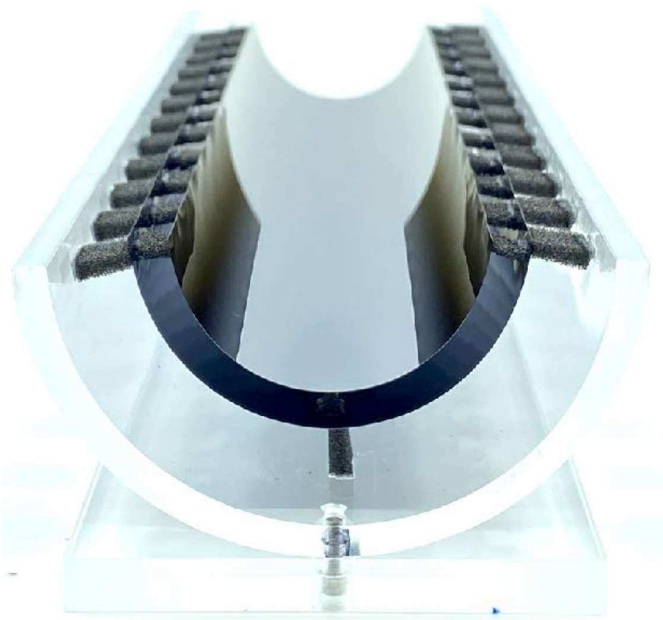
Layer assembly

CERN ALICE

Layer 2

Layers 2+1

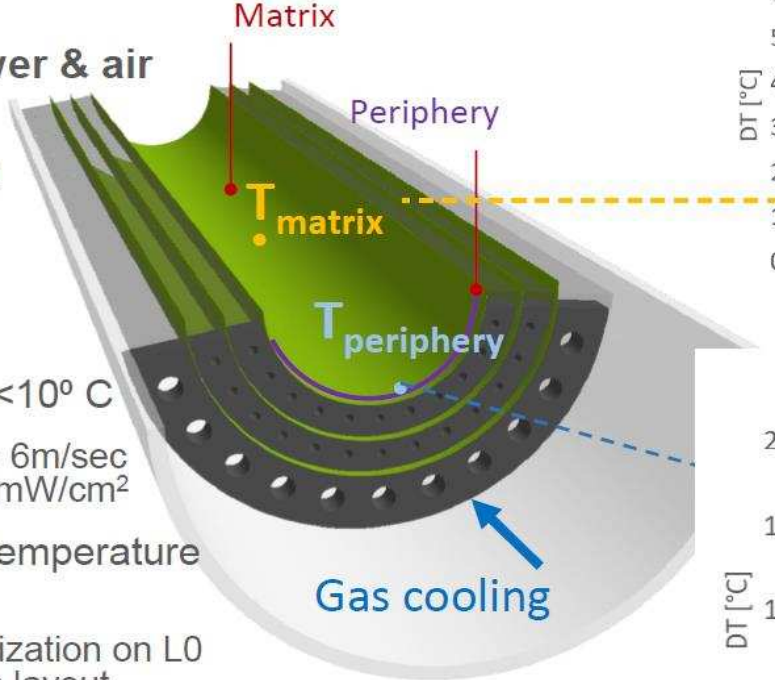


Layers 2+1+0

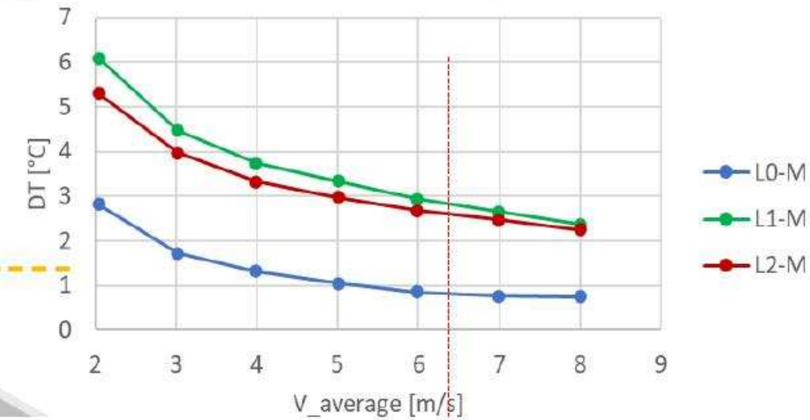
3-layer integration successful!

Wind tunnel cooling studies

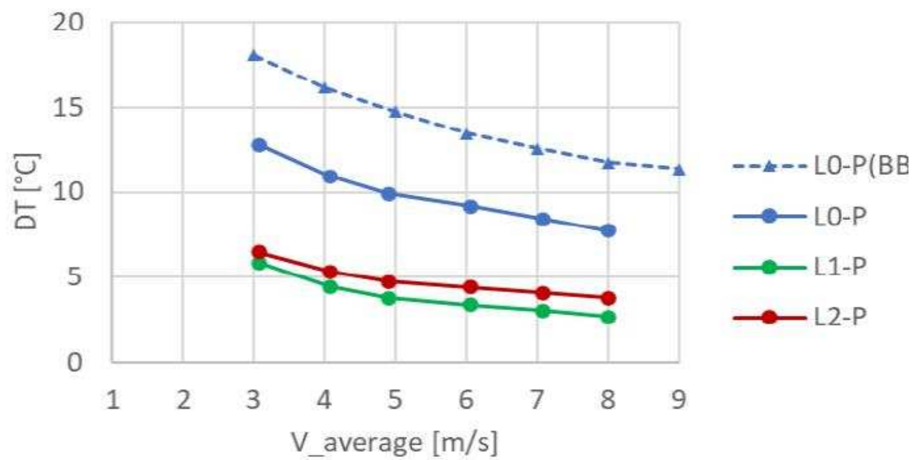
- **Tests with model and heaters**
  - **Different power & air speed**
  - **Carbon foam radiator are key for heat removal at periphery**
  - L1 and L2 DT <10º C
    for gas flow> 6m/sec and PW 900mW/cm²
  - L0 has larger temperature DT to air
    further optimization on L0 Carbon foam layout
  - Power density concentrated on 2.5 mm periphery



DT = $T_{periphery}$ − T_{air_in} Vs Airspeed Matrix 20mW/cm²



Periphery 900mW/cm²



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CURVED SENSOR DEVELOPMENT BASED ON ASSEMBLY OF ALPIDE SENSORS

A Large Ion Collider Experiment

ALICE

Super-ALPIDE mockup assembly - V2

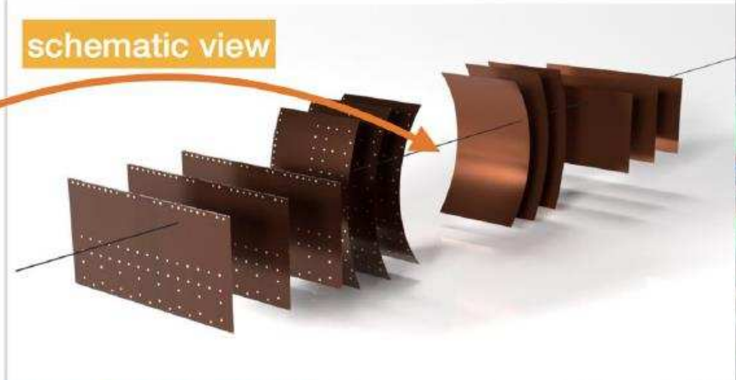
Wire-bonding through exoskeleton

from ALICE-ITS3 - internal $\Rrightarrow$ **NOT TO COPY**

ALICE | WP4 meeting | 14 April 2022 | Domenico Colella 16

▷ **Extendable to MIMOSIS+ : $\lesssim$ 5 μm – O(1 μs) – 2 Gbits/s**

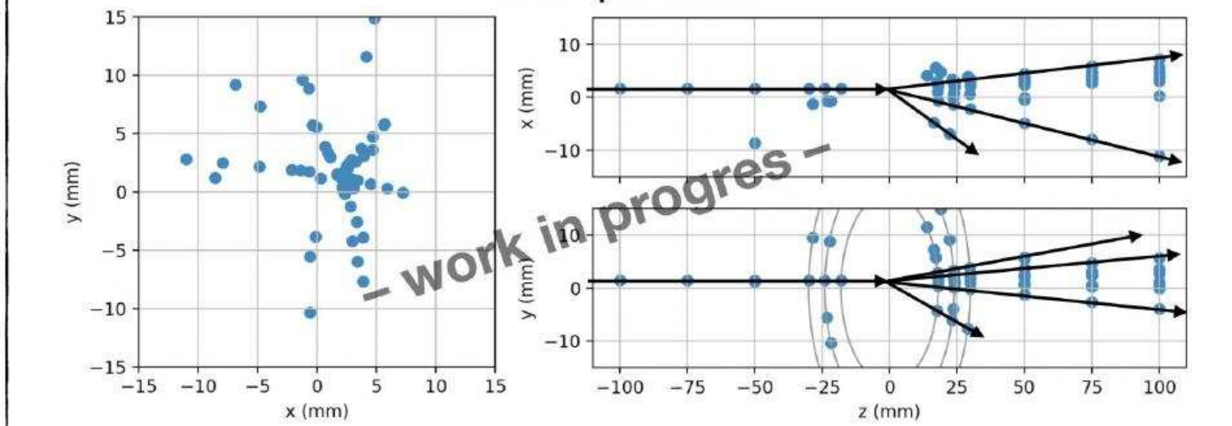
µITS3



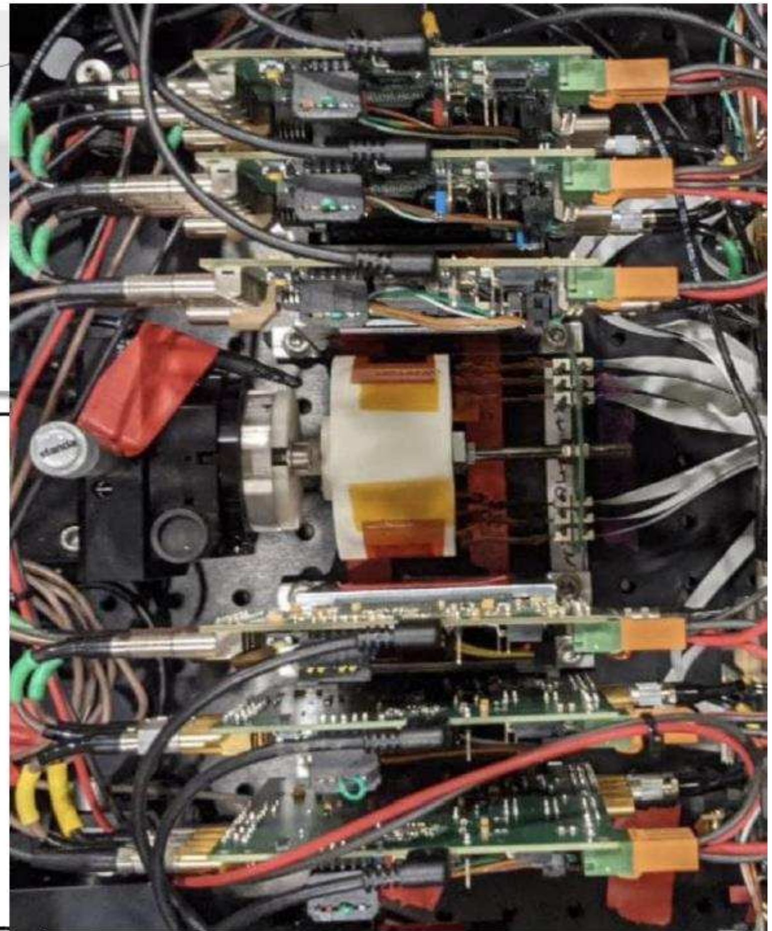
Cu target in the center

expect to see 120 GeV proton/pion–Cu collisions

Example event



[few hand-drawn track lines to guide the eye]



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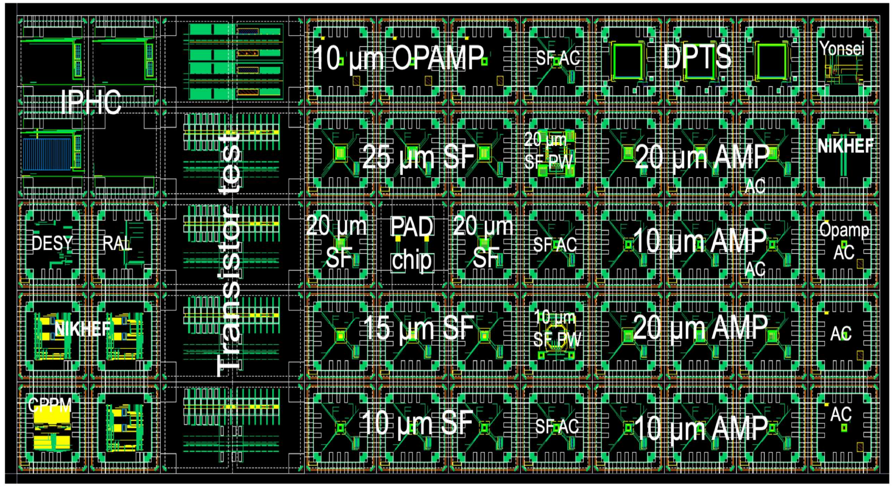
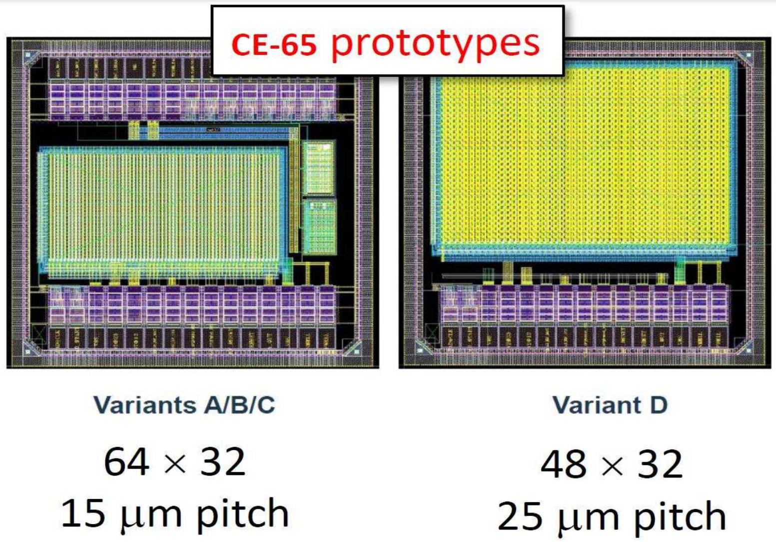
Exploration of a 65 nm Imaging Technology

- **Motivations of the R&D:**
  - ⋇ Smaller feature size than 180 nm technology used for MIMOSIS
    $\Rrightarrow$ smaller pixels, more in-pixel functionnalities,
    less power consumption, faster readout, ...
  - ⋇ Imaging technology available since $\sim$ Spring 2020:
    includes stiching $\Rrightarrow$ multireticle sensors
  - ⋇ R&D coordinated at CERN (ALICE-ITS3 & EP-div)
  - ⋇ ITS3 goals: small pixels and very low material budget
    exploiting stitching for "supportless" detector layer



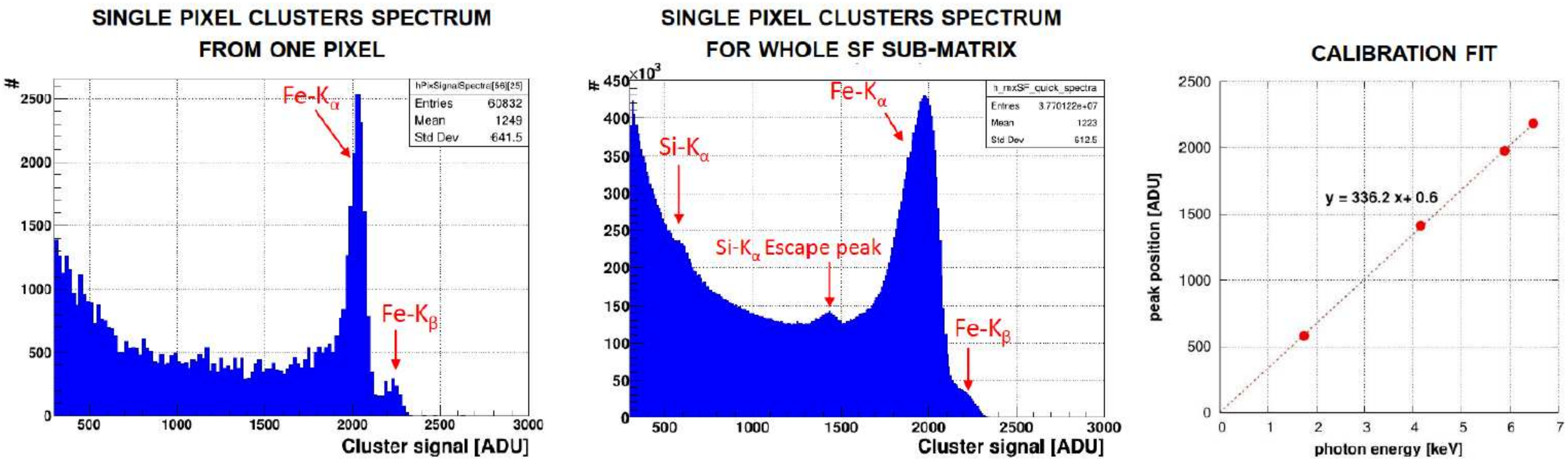
- **Prototyping at IPHC for MLR1 (2020):**
  - ◦ Design of "elementary" test structures with CERN
  - ◦ Design of 2 chips featuring arrays of 15x15 & 25x25μm^2 pixels
    with rolling shutter readout & analog output
  - ◦ Grouped submission (MLR1) submitted to TowerJazz
    for fabrication during Winter-Spring 2020-21
  - ◦ Tests under way: detection performances are promising



MLR1: CE-65 Proto. Testing Charge Collection with 15 μm Pitch

CE65 (IPHC): Exemplary ^{55}Fe spectra

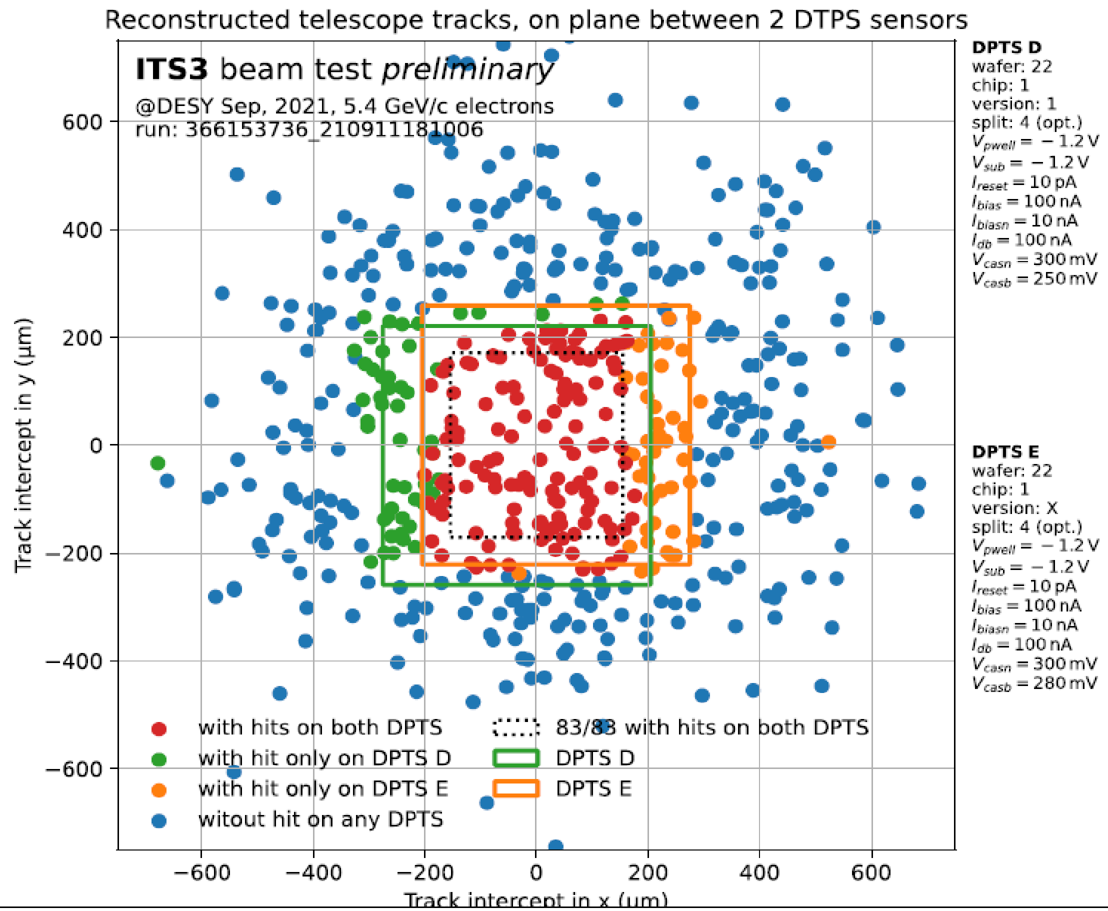
Source follower sub matrix, optimised diode



See S. Bugiel, A. Dorokhov et al, VCI

from VCI-2022 - S. Bugiel et al.

Beam test with Telescope with DPTS



- **Tracks without hit in the DPTS**
  - **have 100% shadow over DPTS**
- **166/166 tracks in DPTS1**
- **162/162 tracks in DPTS2**
- **and even for both in coincidence 83/83 tracks**
- **100% efficiency**
- **Excellent sensor/front-end performance already from first 65 nm prototype**

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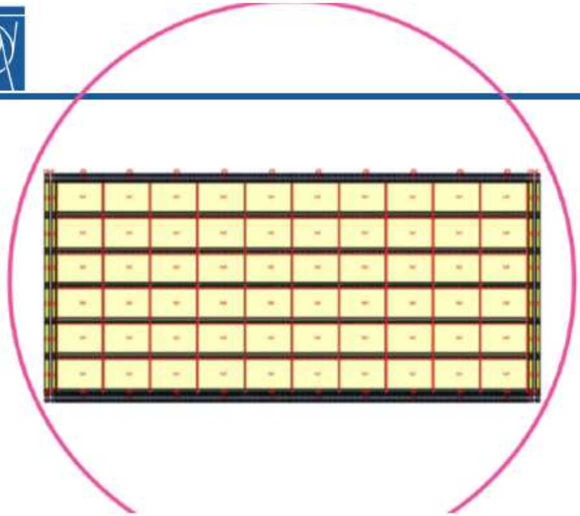
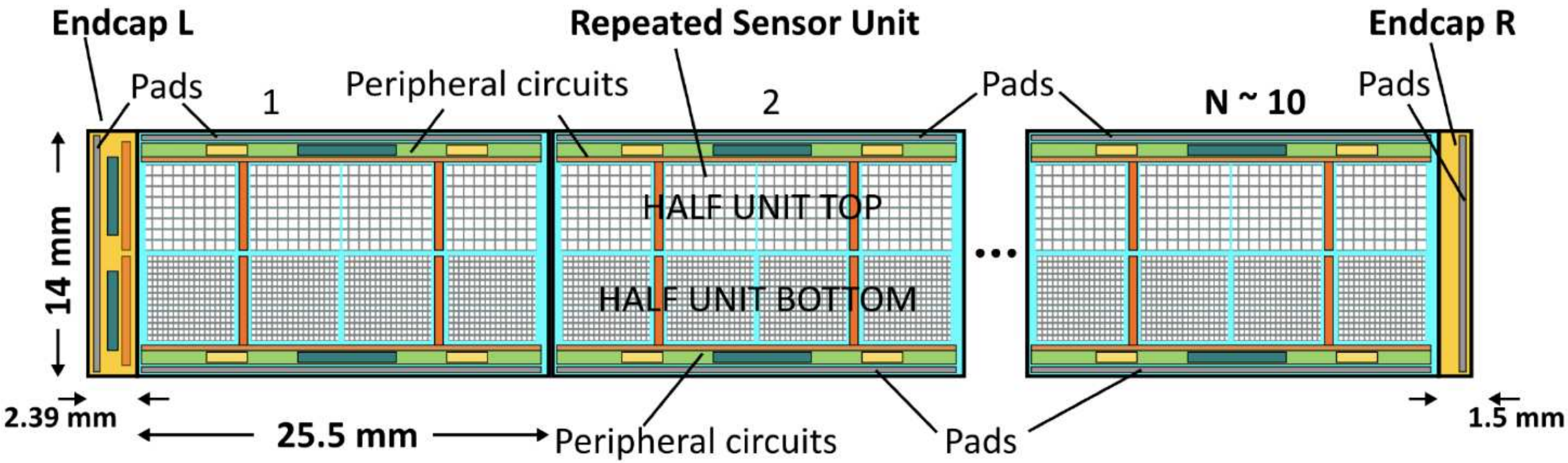
Stitched sensor ASICs



- **Next big milestone in sensor design: stitching**
- **Design activity in full swing**
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**



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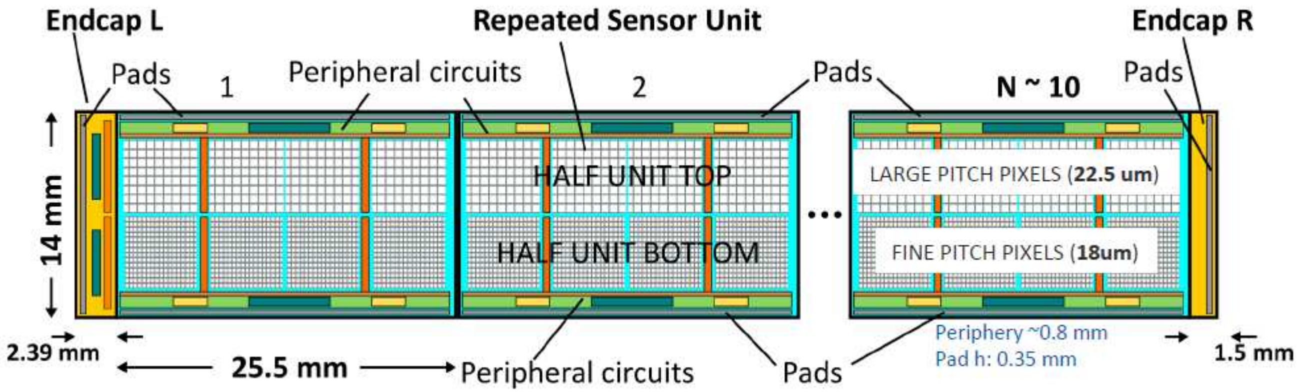
Next Step: ER1 including 25 x 1.5 cm large sensor in 65 nm Technology

MOSS Monolithic Stitched Sensor Prototype



Primary Goals
Learn Stitching to make a particle detector
Interconnect power and signals on wafer scale design
Learn about yield and DFM
Study power, leakage, spread, noise, speed

- Large sensor abutting identical but functionally independent sub-units
  - Repeated Sensor Unit, Endcap Left, Endcap Right
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

On behalf of MOSS team

VXD Upgrade -Requirements

Radius range: R	14 – 135 mm (**)
Tracking & Vertexing performance at least as good as current VXD	
Single point resolution(*)	< 15 um
Total material budget	< (2x 0.2% + 4x 0.7%) X_0
Robustness against radiation environment	
Hit rate(*)	~ 120 MHz/cm^2
Total Ionizing Dose(*)	~ 10 Mrad/year
NIEL fluence(*)	~ 5.0 × 10^{13} n_{eq}/cm^2/year

(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

- Be prepared for a major interaction region redesign
  - Allow large safety factors against backgrounds
- Take advantage of technology development
- Possible performance improvements
  - Impact parameter and vertexing resolution
  - Tracking performance for low pT tracks
  - Lower trigger latency
  - L1 trigger capabilities

INFN Feb 23, 2022 F.Forti - Belle II Upgrades Belle II++ 12

- Little overlap in sensor requirements: $<$ (15 μm, 100 ns, 200 mW/cm^2)
- **But:** cooling system possibly relevant for FCCee vertex detector

CONCLUSIONS

- SCIENTIFIC PRIORITIES FOR THE R&D TARGETTING A VERTEX DETECTOR AT FCCEE (ALL E_{CM}):

1) **Material budget !!!** ⇛ multi-reticle, very low power pixel sensor integrated in an ultra-light and stable system **(challenging)**

2) Spatial resolution: $\sigma^{sp}_{R\phi,Z} \approx 3\ \mu m$ (less challenging)

- PRIVILEGED ENVIRONMENT FOR THIS R&D:

⋇ ALICE-ITS3 W.P.-3 & W.P.-4 (together with CERN-EP R&D W.P.-1.2)

⋇ Devt of stitched (i.e. multi-reticle) CMOS pixel sensors ⇛ mat. budget

⋇ Exploration of 65 nm TJsc process

⇛ low power, thin (bending), small pixels

Will end up with a real detector taking data in $\gtrsim 5 yrs$

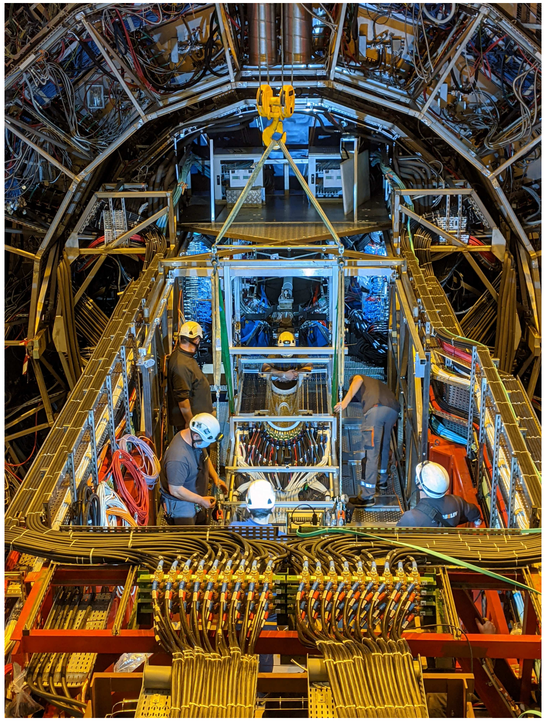
- COMMENT ON FAST SENSORS:

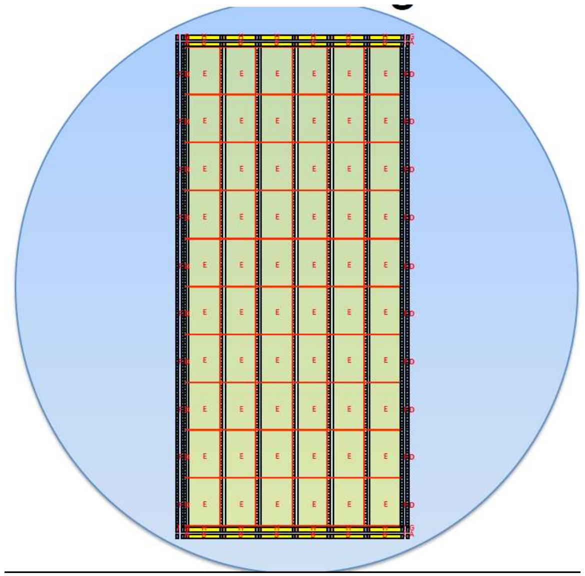
⋇ **not a must for a vertex detector** addressing Higgs, top, Z, WW physics

⋇ added value for BG rejection, TOF, B decays, long-lived new particles, ...

⋇ generates substantial extra power consumption ⇛ extra material !

⇛ avoid vertex detector and minimise fast detector surfaces





ALPIDE: Single point resolution and Cluster multiplicity

ALPIDE Position resolution and cluster size