Status CE65v2_xx chip

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CE65v2_xx (1.5mm x 1.5mm) PADs

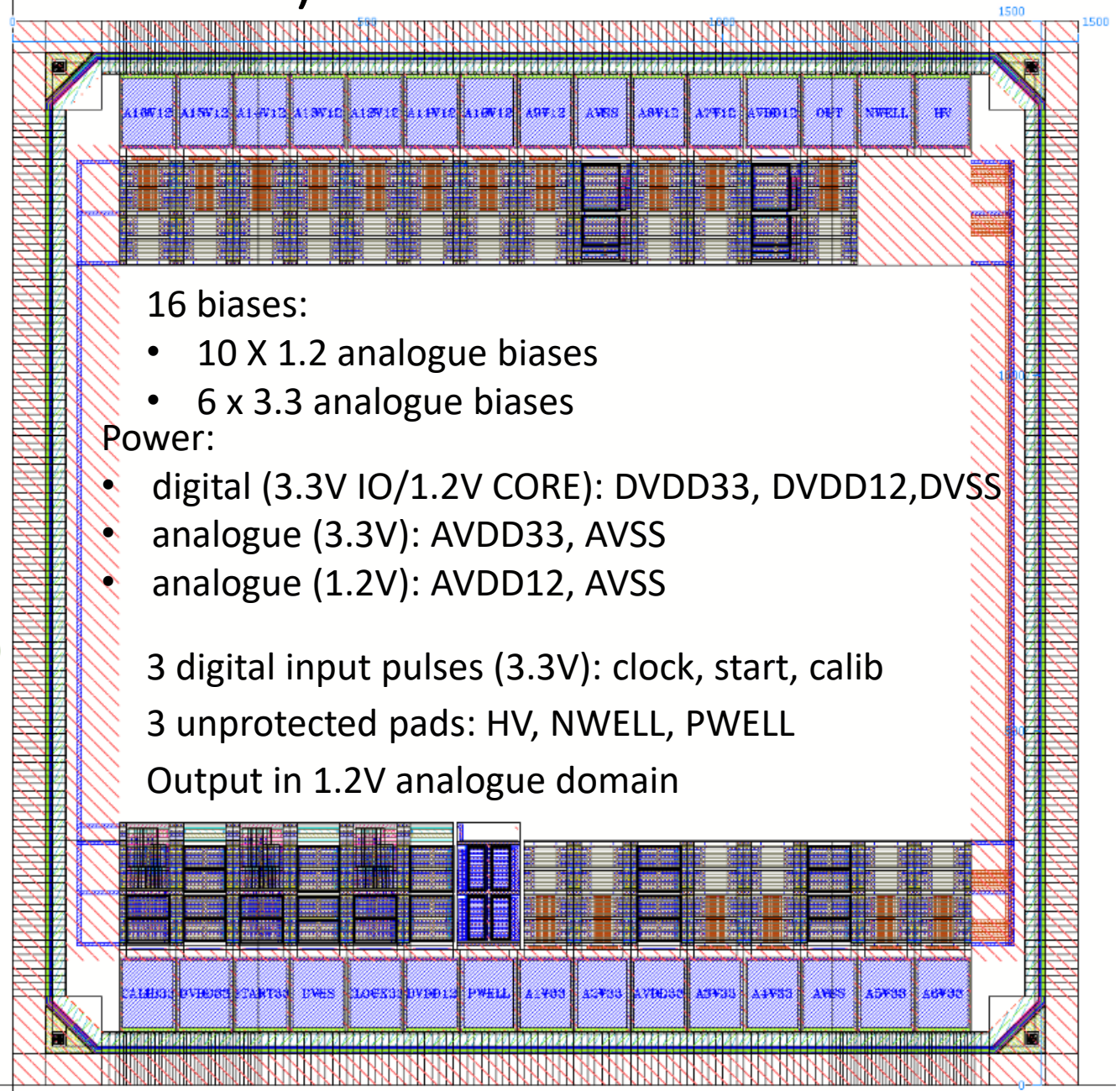
Versatile (test vehicle) chip using matrix of pixels (32 x 32) output is multiplexed to one analogue (digital pulse readout in analogue mode) channel (rolling shutter mode):

- ✓ Share common padring structure, carrier and proxy boards
- ✓ 4 power domains: 3.3V analogue, 1.2 analogue, 3.3 digital, 1.2 digital
- ✓ 3.3 analog and 1.2 analog share same ground AVSS
- ✓ 3.3 digital and 1.2 digital share same ground DVSS

The pads are from standard library, including power domain separator cells, not modified: "IO_TPS65ISC_W60_NP_4M_33V" (LVS/DRC ok) With new metal stack, will they remain 1-to-1 compatible?

Changes from CE65 version (MLR1):

1. Added calibration charge pulse
2. No DACs (but we can resubmit existing CE65 for that if needed)
3. Number of biases (10 in 1.2V domain and 6 in 3.3V domain)
4. Only one pixel design for charge collection chip version (taken at basis of measurements)
5. Digital and analogue domain reworked (3 powers-> 6 powers):
   - VSS is separated for analog/digital domain
   - VDD12 is separated for digital core and analogue domain
   - VDD33 is separated for digital IO and analogue domain



16 biases:

- 10 X 1.2 analogue biases
- 6 x 3.3 analogue biases

Power:

- digital (3.3V IO/1.2V CORE): DVDD33, DVDD12,DVSS
- analogue (3.3V): AVDD33, AVSS
- analogue (1.2V): AVDD12, AVSS

3 digital input pulses (3.3V): clock, start, calib

3 unprotected pads: HV, NWELL, PWELL

Output in 1.2V analogue domain

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CE65v2_xx signals specification

Signal	Purpose	Specs	Comment
AVDD33, AVDD12, 2 x AVSS, DVDD33,DVDD12, DVSS, PWELL,NWELL, SUB(not a pad), HV	power	3.3v/1.2v/0v/ 3.3v/1.2v/0v/ -var/+var/-var 0 - 20V	With current monitor on proxy or HV supply
START, CLOCK	single pixel selection/rolling shutter scan	digital IO 3.3v, ~40 MHz	
PULSE	Injection	digital IO 3.3v, ~40 MHz	
Bias(V or I) 3.3 domain [1:6]	FE, 3T pix,… biases	Low current ~mA, from 0 to 3.3v	For CE65(A,B,C,D) VRESET..
Bias(V or I) 1.2 domain [7:16]	FE, 3T pix,… biases	Low current ~mA, from 0 to 1.2 v	for MOSS FE and variations
Out	1.2 domain output		

Total 30 PADs, this fits to existing chip size (1.5 mm X 1.5mm) of CE65

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Different modifications/chips of CE65v2_xx

Modif.	Purpose	Pitch, um	Comment	N
CE65v2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (one best pixel from CE65 will be selected, preliminary test shown better S/N with in pixel amplifier)	15, 18, 22.5, 18_{hexsq},22.5_{hexs}, $22.5_{hex(*)}$	For lab and beam test, charge collection node, techno, optimization	5
CE65v2_A_xx	Precise measurements of multiplexed analogue or digital output of pixel FE ("_A_"): pulse duration, gain, FPN, noise, RTS..	18	For lab only, possibility to measure with oscilloscope FE optimization/tuning, one pixel measured at time	1+.
CE65v2_D_xx	Digital FE ("_D_"), matrix of pixels with digital storage -> digital clusters	15(*), 18, 22.5, 22.5_{hexsq}	For lab and beam tests, Optimization of variants of digital FE + charge collection study	4

Goals:

1. CE65v2_C_xx: 15um- compatibility with previous chip + testing better resolution, other combinations to match to MOSS/MOST, a combination true "hex" for academic study
2. CE65v2_A_xx: one pitch 18um – exact geometry has less importance for FE tuning , 1 FE from MOSS/MOST or + variants for optimization + if new ideas come which are not in MOSS/MOST
3. CE65v2_D_xx: pitch combinations to match to MOSS/MOST, a version of FE which could be in MOSS but not implemented there

Total ~10 chips: do be discussed (blue(*) in less priority), Estimated time schedule:

1. end of December – at least one completed chip version for test submission(new metal stack ?..)
2. + ~0.5 - 1 month for each modification(of 3).. – February - March

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