Propositions for evolution of CE65 in next 65nm run-versatile CE65v2_xx chip

Andrei DOROKHOV,
on behalf of C4Pi and PICSEL,
IPHC, Strasbourg
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CE65v2_xx

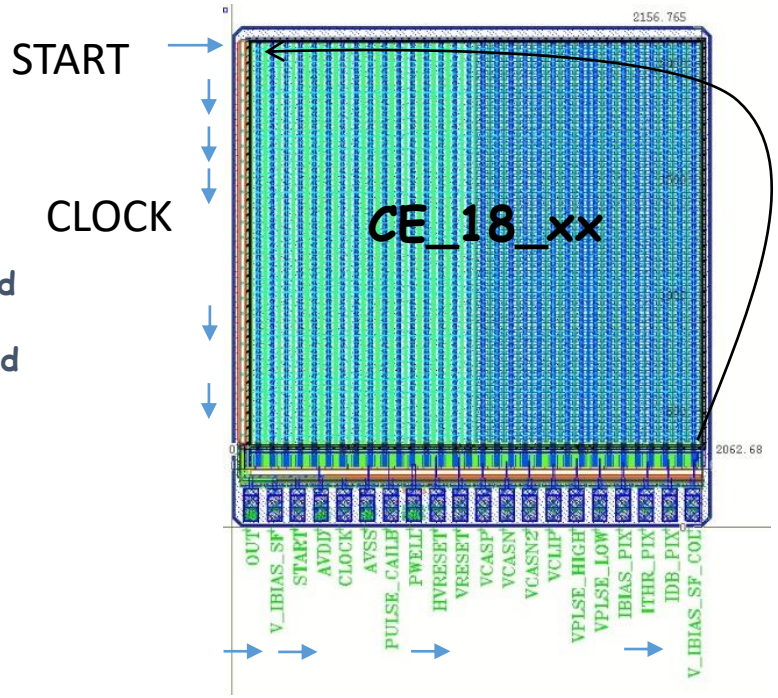
Versatile chip using matrix of pixels (~3T, analogue, digital) in a rolling shutter readout way to one analogue (digital pulse readout in analogue mode) channel:

- ✓ Share common padring structure, carrier and proxy boards
- ✓ Should have sufficient number of biases for FE circuits (~10)
- ✓ 3 power domains: 3.3V analogue, 1.2 analogue, 1.2 digital
- ✓ Possibility to inject calibration pulse, set one high voltage and one substrate bias
- ✓ Possibility to continuously scan pixels in matrix with clock and start signal, or using the same digital signals to select single pixel
- ✓ Size of matrix > ~1000 pixels, other options discussed later

All that already exists in CE18_xx chips+carrier+DAQ, but not in CE65(ABCD), so new chip would be close to functionalities of CE18_xx

CE_18_xx: 64x64 pixels, pixel output is multiplexed to common output by CLOCK and START:

1. **START high - upper left pixel [first] selected**
2. **CLOCK high and START low - go to next address: pixel from top to bottom in the column, and then from left column to right column**



andrei.dorokhov@iphc.cnrs.fr , IPHC, Strasbourg

CE65v2_xx signals specification

Signal	Purpose	Specs	Comment
AVDD33, AVDD, AVSS, DVSS, PWELL, SUB, HV	power	3.3v/1.2v/0v/0v/-var/-var/~20V	With current monitor on proxy or HV supply
START, CLOCK	single pixel selection/rolling shutter scan	digital 1.2v, ~40 MHz	
PULSE	injection	digital 1.2v, ~40 MHz	
Voltage_Bias12 [1:5]	FE, 3T,… bias	Low current ~mA, from 0 to 1.2v	for MOSS FE and variations
Voltage_Bias33 [1:2?]	FE, 3T,… bias	Low current ~mA, from 0 to 3.3v	For CE65(A,B,C,D) VRESET
Current_Bias [1:5]	FE, 3T	Low currents < 1u (sink or source?)	Can be scaled on chip, an converted to needed sink or source
Current_Bias [1:2]	Output buffers	50uA ..10 mA (sink or source?)	Can be scaled on chip, an converted to needed sink or source

Total 24 signals, 6 could be redundant (x2?) = total 30 PADs, this fits to existing padring size(15 top 15 bottom pads) of CE65A, however the pads has to be replaced

andrei.dorokhov@iphc.cnrs.fr , IPHC, Strasbourg

Different modifications of CE65v2_xx

Modification	Purpose	Comment
CE65v2_C_xx	Charge collection ("_C_") measurements, rolling shutter clusters with (~3T pixels)	For lab and beam test, charge collection node, techno, optimization
CE65v2_A_xx	Digital FE amplifier, precise measurements of analogue output and/or digital of FE ("_A_") pulse duration, amplitude, FPN, noise, RTS..	For lab only, possibility to measure with oscilloscope, For exploring FE optimization
CE65v2_D_xx	Digital FE amplifier("_D_"), readout matrix of pixels with digital storage, digital clusters	For lab and beam tests, variants of FE + charge collection optimization

andrei.dorokhov@iphc.cnrs.fr , IPHC, Strasbourg

CE65v2_C_xx

Motivations for the test chips to explore charge collection properties ("CE65v2_C"harge) :

- ✓ Square layout: x=y=15um, x=y=18um(==MOSS chip, should we do also 23um?) ,x=y=25um (sq)
- ✓ Staggered layouts with pixel surface = 15x15 um^2, 18x18 um^2, 25x25 um^2 :
  - x=y=15um(hexsq), x=13.95um & y=16.1um(hex)
  - x=y=18um(hexsq), x=16.75um & y=19.3um(hex)
  - x=y=25um(hexsq), x=23.26um & y=26.86um(hex)

- ✓ Several technology options (tech flavor: X times, splits) – minor changes to on top of chip layout

Total: 9 matrix versions (X tech options), do we need to have another sizes? Or reduce not interesting cases? ->

➢ need confirmation (agreement) before starting the design of matrixes,
existing CE65 PADring/Carrier board will be reused, shift registers may require small modifications

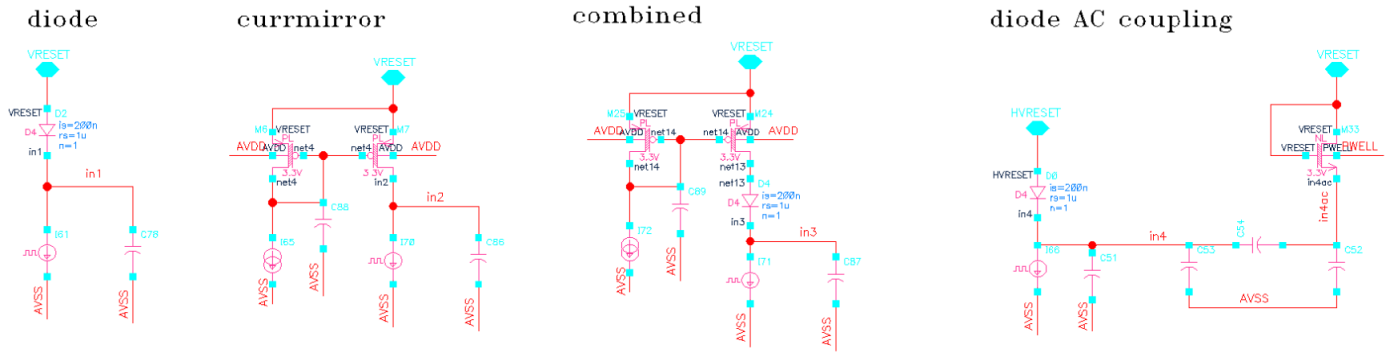
Note:
Proposed structures naming conventions: "chipname_purpose_pitch[+layout modifier: sq, hex, hexsq]_FE option[AC,DC coulped]_technooption"
Example, CE65v2_C_18sq_AC_1 : exploratory chip in 65nm v2, charge measurements, 18 um pitch square configuration, AC coupled, technology option 1 (standard process or else, t.b.d.)

andrei.dorokhov@iphc.cnrs.fr , IPHC, Strasbourg

CE65v2_C_xx

The leakage current for rolling shutter architecture is main concern: it deteriorates response, which should be linear to study charge collection properties.

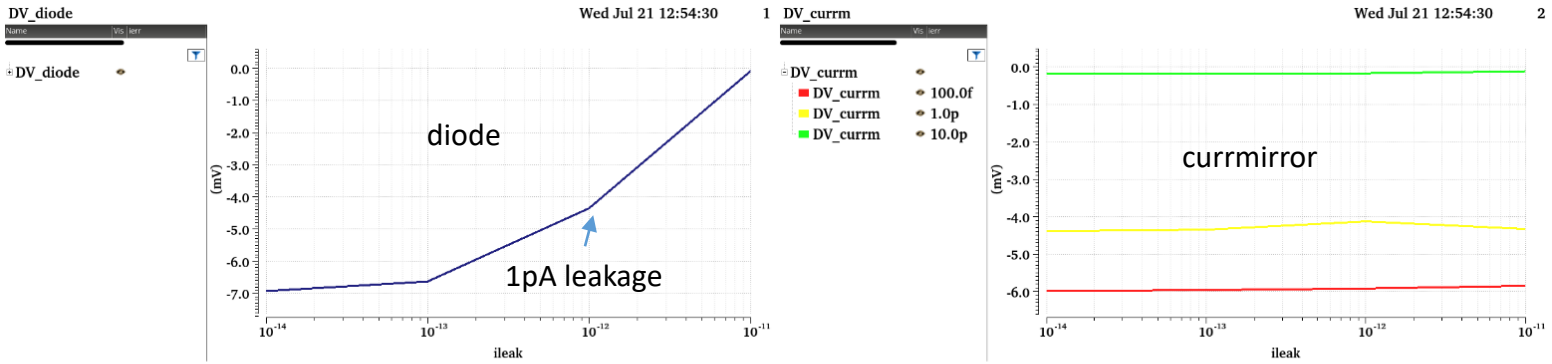
If we keep one readout channel at 40MHz, frame readout time is ~25 us for 1024 pixels.



Four biasing schemes are studied, in current CE65 diode biasing used for DC and AC.

Signal (negative) as a function of leakage current: value at 25 us after injection of 100e

1) For diode versions, for 1pA leakage signal loss already significant
2) for current mirror is OK, but need fine adjustment of current(~100fA) to compensate the leakage current – so it is may dangerous
3) For combined version, if fine current adjustment is failed, at least it works as diode version and has less parasitic capacitance



➢ need to estimate upper limit of leakage current from measurements of CE65: if >> 1 pA /pixel – even reduced to 32x32 pixels matrix can not be measured with this simple readout architecture-> other options to cope with high leakage: smaller matrix, parallel readout, analogue memory…

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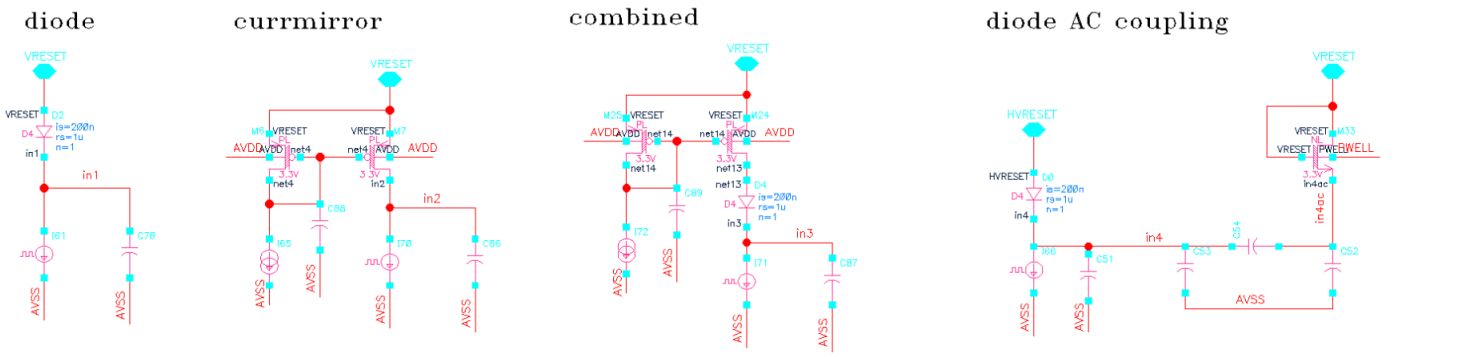
For reference, results of simulation: value after 1us from injection of 100e



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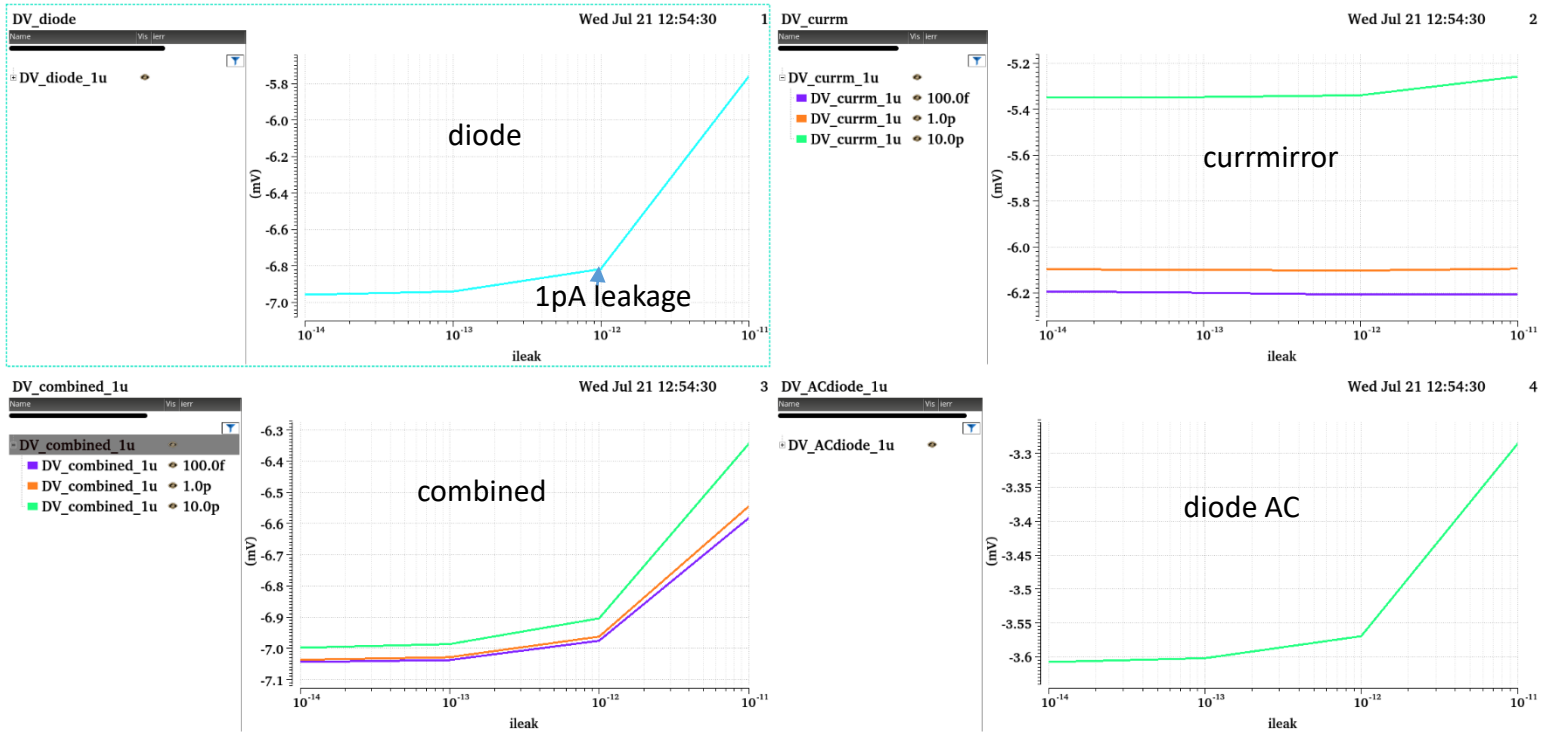

Signal (negative) as a function of leakage current: value at 1 us after injection of 100e

andrei.dorokhov@iphc.cnrs.fr , IPHC, Strasbourg

CE65v2_C_xx

In exiting CE65 there are 3 version of FE are used: AC and DC voltage level amplifiers and SF: one perhaps should choose either amplifier or SF version – in new chip we also can reuse those existing blocks, but first -

- need to measure (spectrum from Fe55) CE65 in order to understand what can be used, is S/N sufficient for given FE variant
- most likely amplifier version is OK, but need to be confirmed by test

1) For CE65v2_C_xx we may completely reuse CE65 padring, but with loosing the idea of generalization of the test chips with rolling shutter architecture, so may be not a good idea - in any case the matrixes has to be redone
2) We may also re-submit same existing CE65[A,B,C,D] for monitoring of foundry process change? Depends on availability of place for chips

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CE65v2_A_xx and CE65v2_D_xx

First variant of chip is intended to be used for FE amplifier tests (“CE65v2_A”mplifier), i.e. matrix of amplifiers (~1000) with selectable output, which can be digitized or monitored by oscilloscope – gain, dispersion, noise, (RTS?)..

FE amplifier (with discriminator) are possible optimization versions of FE from MOSS, both analogue or digital pulses can be monitored by pixel selection.

Second variant the chip is intended to be used for measuring digital clusters (“CE65v2_D”igital): each pixel has FE (with discriminator) and a memory (digital latch..).
The readout is done in rolling shutter mode, similar to CE65V2_A, except only binary hits map is measured.

- FE of MOSS actually has ~10 biases : in existing CE65 there are 7 biases possibly reused (if needed current maybe converted to voltage) –> seems to be hard to reuse CE65 “as it is”…
- May be reusing PADring of DPTS with carrier board, is best solution, does it has sufficient number of biases and pixel selection features? -> Not sure, and not universal approach…

Note:
Proposed structures naming conventions: “chipname_purpose_pitch[+layout modifier: sq, hex, hexsq]_FE version_technooption”
example CE65v2_A_18sq_F1_1 : exploratory chip in 65nm v2, analogue measurements, 18 um pitch square configuration, front end version 1 technology option 1 (standard process or else, t.b.d.)

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Conclusions for CE65v2_[C,A,D]_xx

1) Three variants, depending on purpose of one versatile CE65v2 chip are described, potential problems spotted in relation to measurements of CE65[ABCD]

2) Total possible number of chips:
{3pitch X 3 layout opts x 2 AC/DC x [techno options] } + 2? X Analog FE + 2? X Digital FE == 22.
That is multiplied by techno options, do we need techno option splits for A/D FE? Do we need to resubmit existing CE65[ABCD] in addition?.. -> if too much we should reduce combinations and prioritized them..

3) Most likely not possible to reuse/adapt existing padrings of CE65, for CE65v2_xx one need to create new PADring design and carrier board – but 3T structures and charge sensing diodes can be reused (need to be confirmed by measurements of CE65)

4) Appropriate new proxy board needed –> to be confirmed (by FW/HW and DAQ developers..)

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