WP12 NA1 - QCD Physics at GSI/FAIR (FAIRnet)

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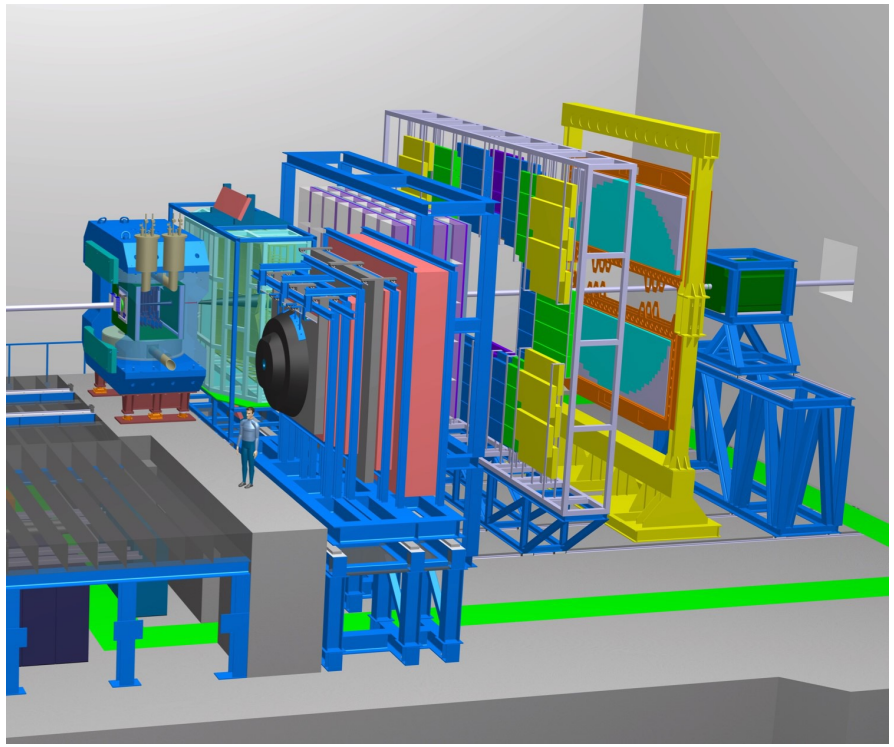
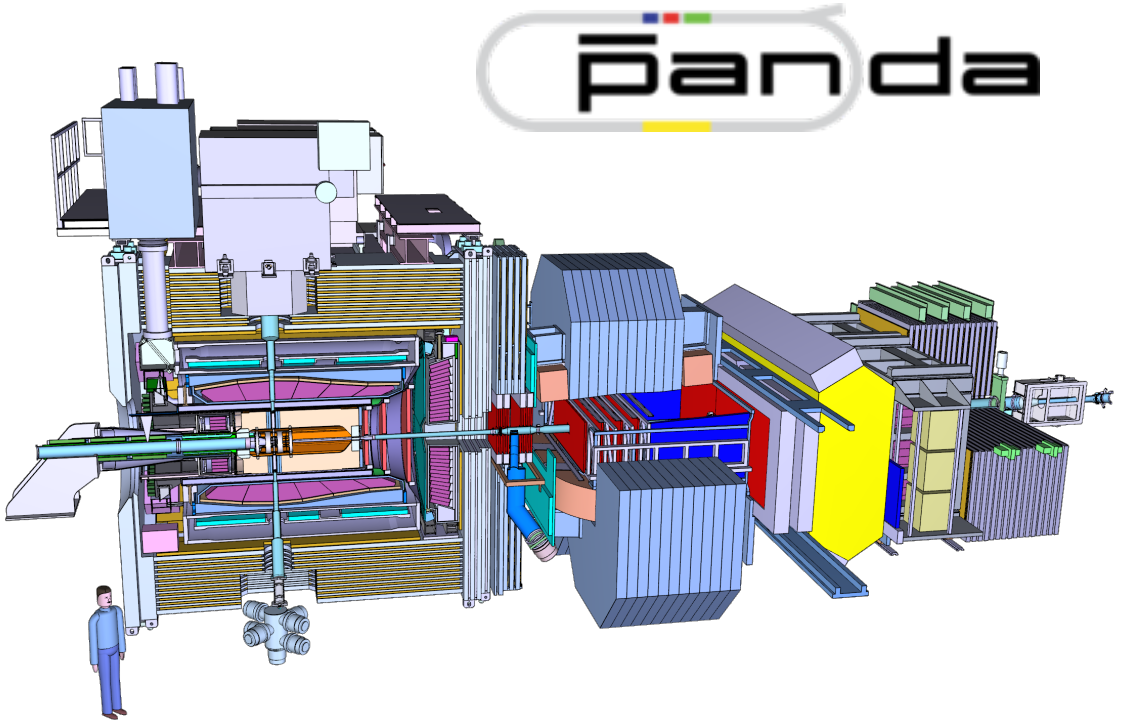
NA1 – QCD Physics at FAIR/GSI

9/2021
CBM Hall

NA1 – QCD Physics at FAIR/GSI



Explore properties of strongly interacting matter under extreme conditions



Investigate the nature of the strong force at the quark level

NA1 – QCD Physics at FAIR/GSI

1. Progress made during the year towards the objectives

Task 1: Front-end electronics, DAQ and Online

Task 2: Demonstrator

Task 3: Data analysis challenge

Task 4: Outreach and education

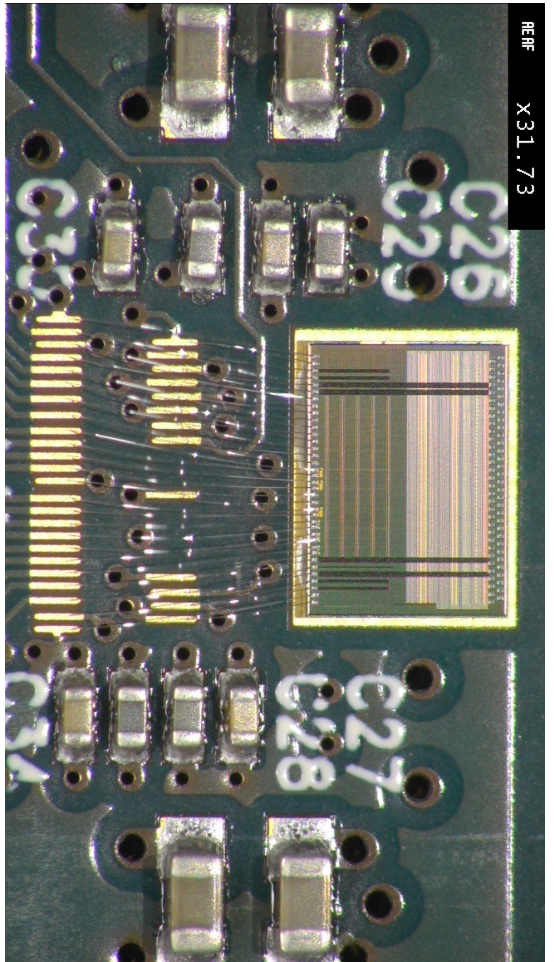
Selected highlights

Progress in Task 1 – Front-end electronics, DAQ and Online

ToASt : a 64 channels readout ASIC for silicon strip detectors in 0.11 µm CMOS technology

[G. Mazza et al. IEEE NSS MIC October 2021]

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy



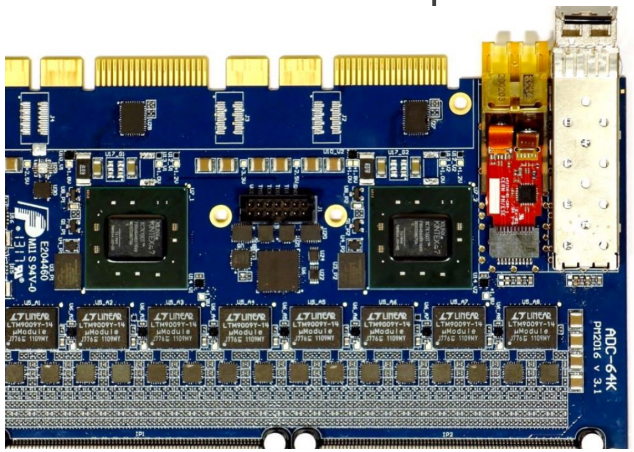
Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.5 × 3.5		mm^2
Pads position	On two sides only		

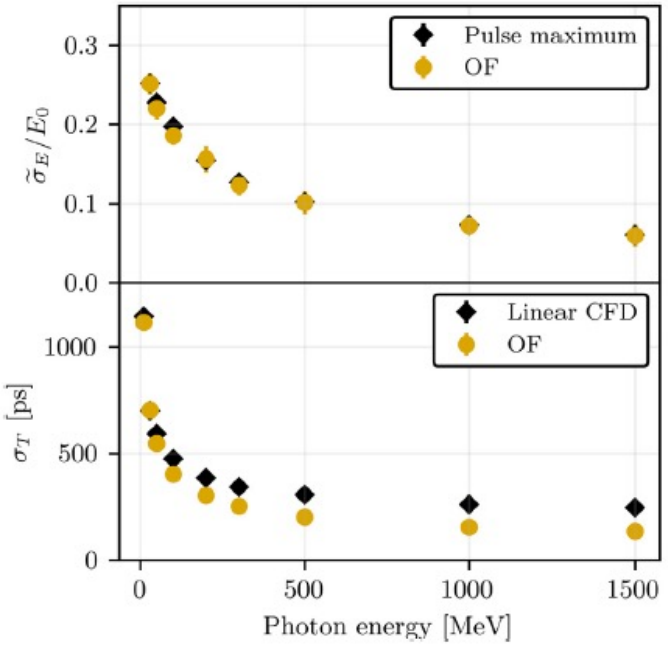
Progress in Task 1 – Front-end electronics, DAQ and Online

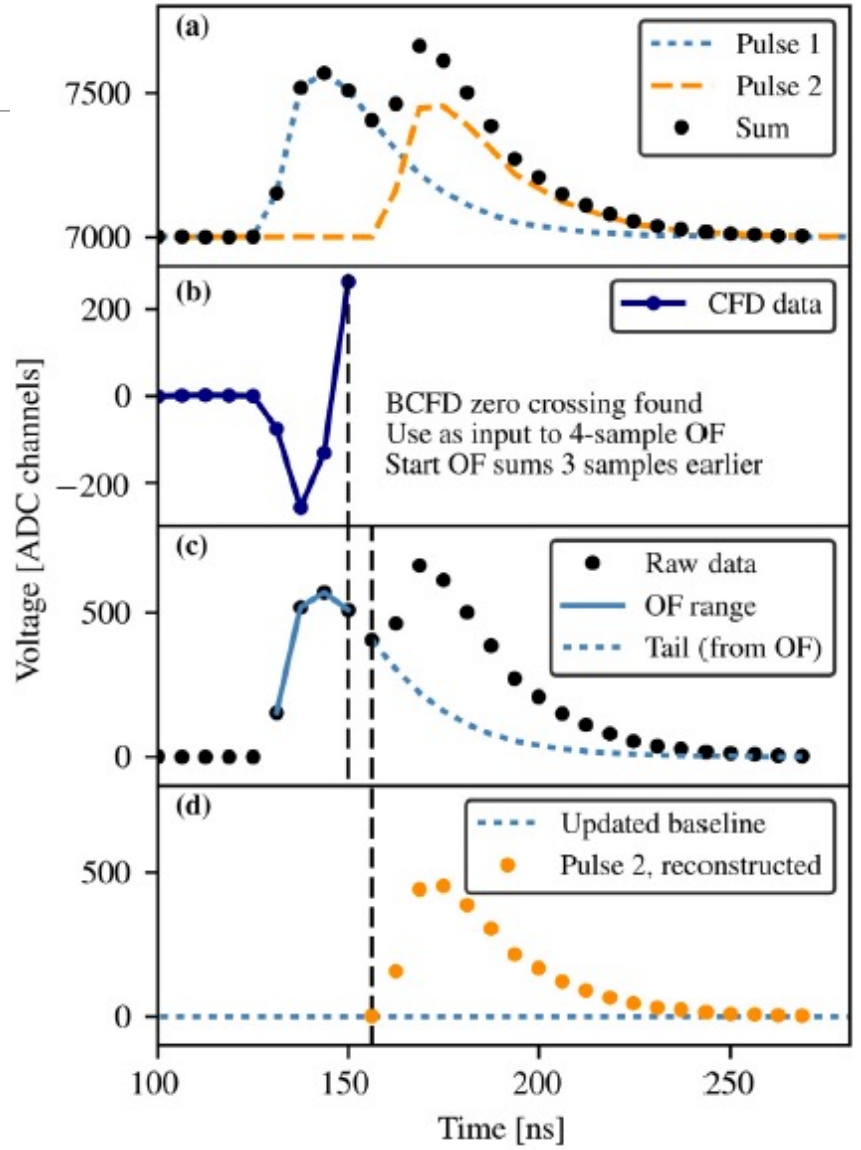
A feature-extraction and pile-up reconstruction algorithm for the forward-spectrometer EMC of the PANDA experiment

[M. Preston et al. NIM A (2021) 165601]

Combination of optimal filter (OF) with constant fraction discriminator implemented in VHDL for the SADC



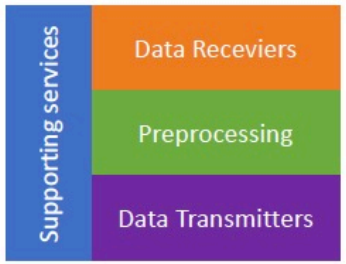




Progress in Task 1 – Front-end electronics, DAQ and Online

Front-end Electronics and DAQ Workshop October 2021

DC Firmware



Data receivers region:
- Logic common to all DCs (configurable num. of links)
- Common link type and protocol
- Unified interface to Preprocessing region

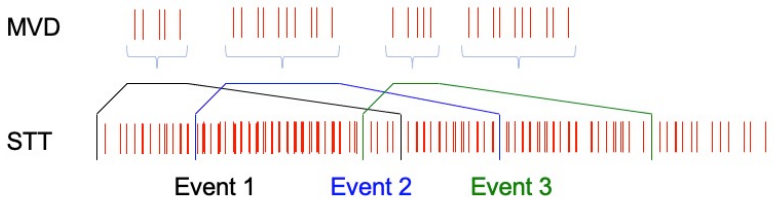
Preprocessing region:
- Fixed, unified data in and out interfaces
- Region available to Subsystem devs.

Data transmitters region:
- Logic common to all DCs (configurable num. of links)
- Unified interface to Preprocessing region
- Commercial network interface

Supporting services:
- Control and monitoring
- SODANet
- ATCA management
- ...

Event Building

Method 1: Add by time window



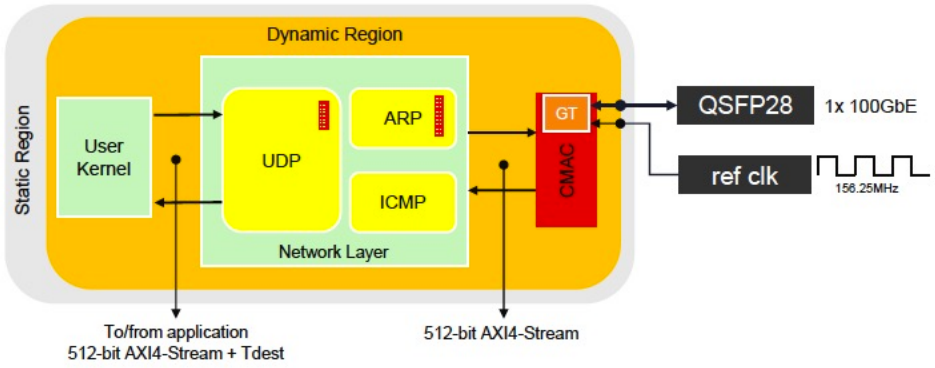
- Event start and stop time from fast detectors (in this example MVD)
- Data from slow detectors added with time window (e.g. -10 ns / +250 ns for STT)
- Overlapping events → remove hits from previously reconstructed events
- Alternative continuous processing

Progress in Task 1 – Front-end electronics, DAQ and Online

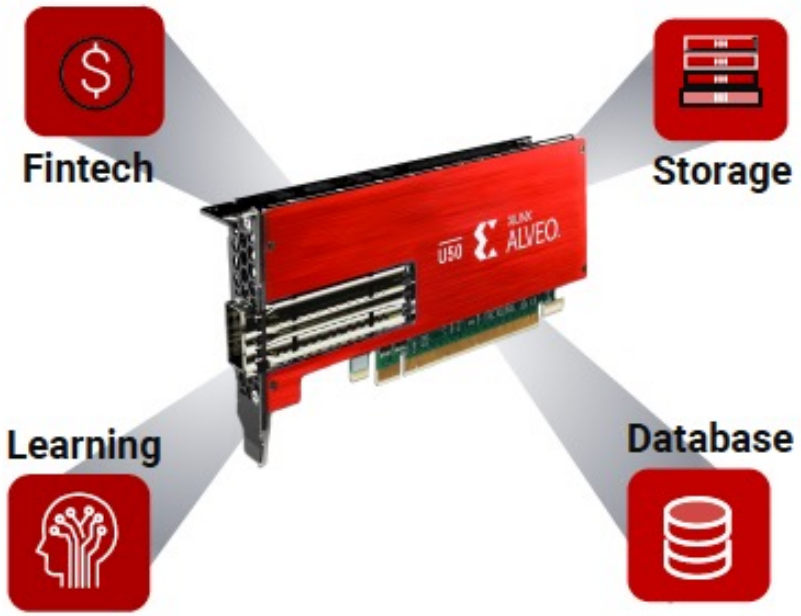
Front-end Electronics and DAQ Workshop October 2021

Invited speaker: Mario Ruiz (Xilinx)

100 Gbit Ethernet



Alveo U50 / U50LV – Low Profile Acceleration Card



Feature	Alveo U50 / U50LV
Primary Application	Fintech + Storage + Database + ML
FPGA	XCU50
CCIX	Yes
Core Voltage	0.85V / 0.72V
Width	Single slot
Form Factor (Passive)	HHHL
Memory Target	8 GB HBM
Memory Config	Dual Stack, 32 pseudo-ports
PCIe	2x Gen4x8, 1x Gen4x8, Gen3x16, CCIX
Network I/F	1X QSFP28
Thermal	Passive
Power (Max TDP)	75W
KLuts	872K

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XILINX

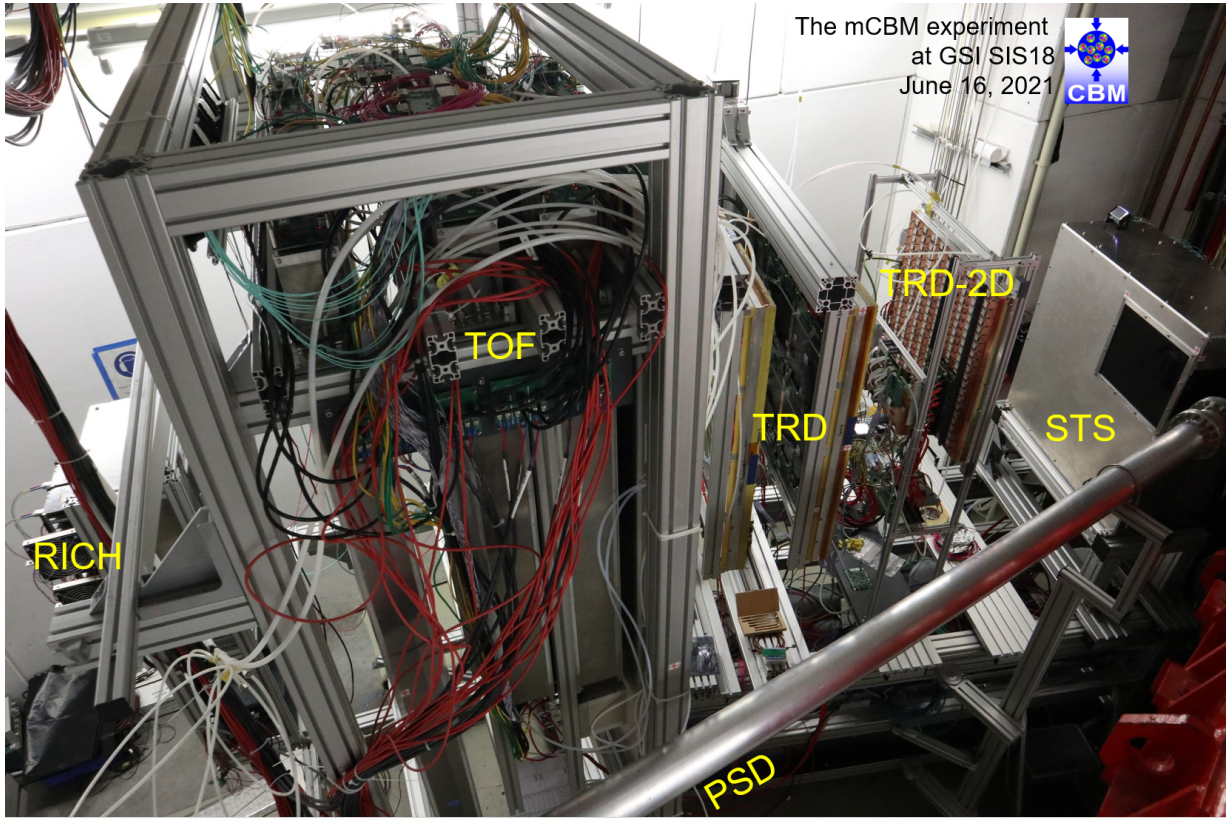
Progress in Task 2 – Demonstrator

June 2021 mCBM@SIS18

- mCBM experiment at SIS18

  CBM full-system test, involving pre-series and prototype detector modules of all CBM subsystems

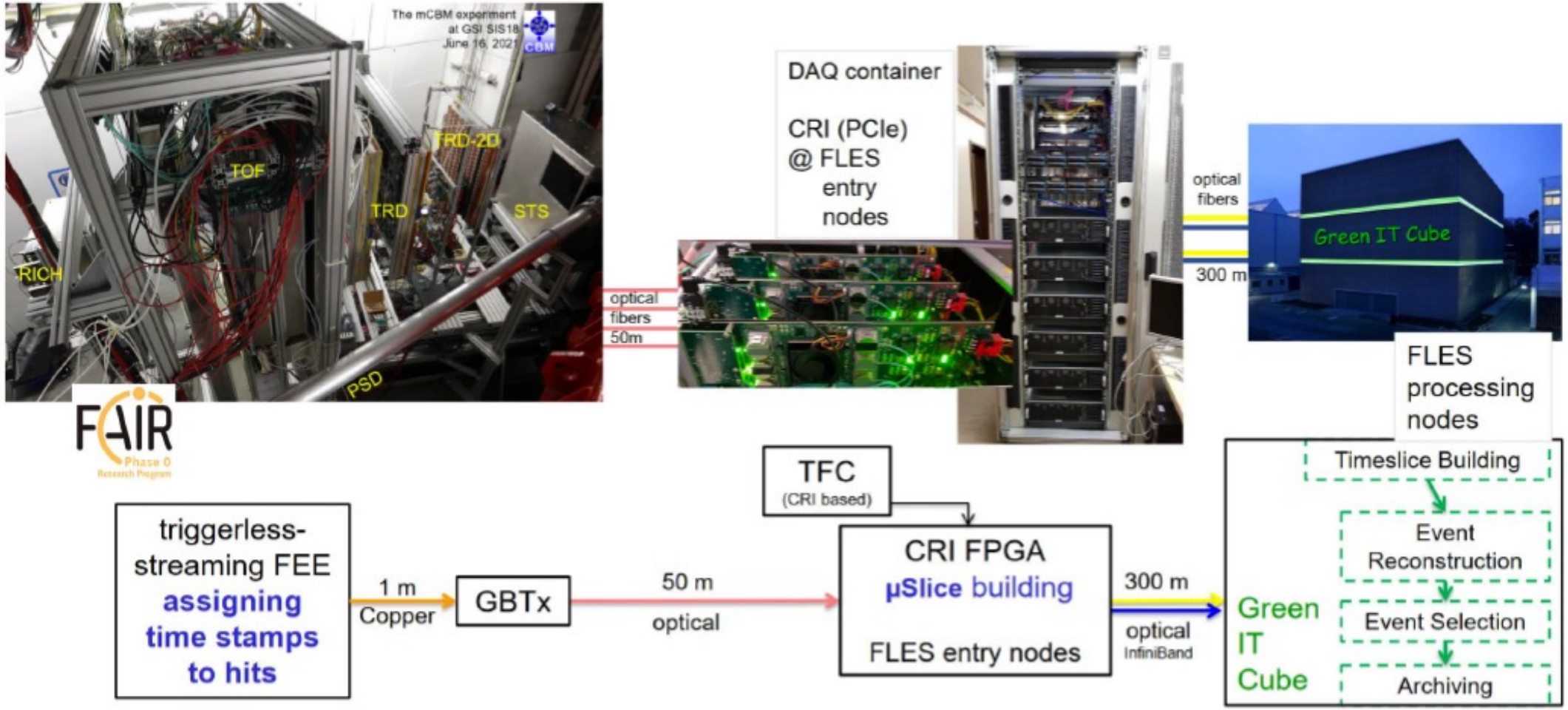
  - High-rate detector tests performed in February - May ‘21
  - Final configuration of the DAQ / data transport system successfully tested with beam in June/July ‘21



Month in 2021	beam ion	Energy, AGeV	target	rate per spill	duration, sec
March	^{208}Pb (67+)	1.06	Ni	2 x 10^9	10
May	^{124}Xe (46+)	1.3	Ni	3 x 10^9	10
June	^{16}O (8+)	2	Ni	10^{11}	10

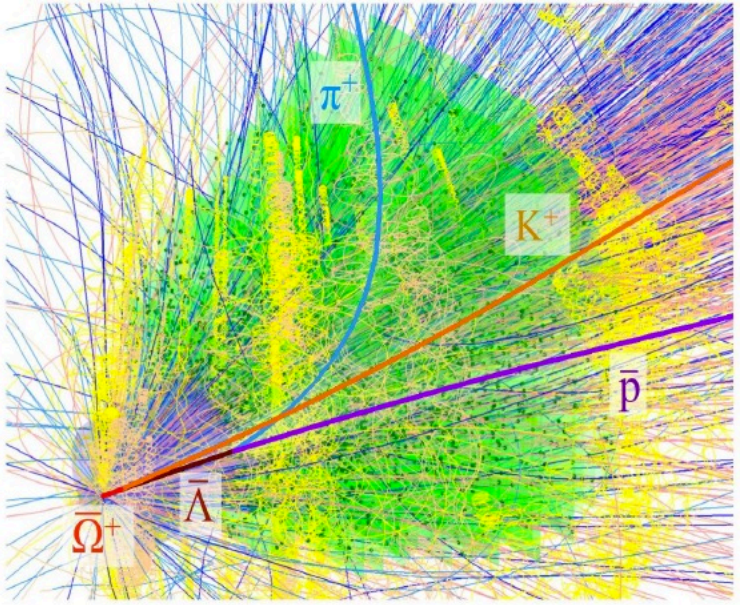
Progress in Task 2 – Demonstrator

The mCBM experiment at SIS18



Progress in Task 3 – Data analysis challenge

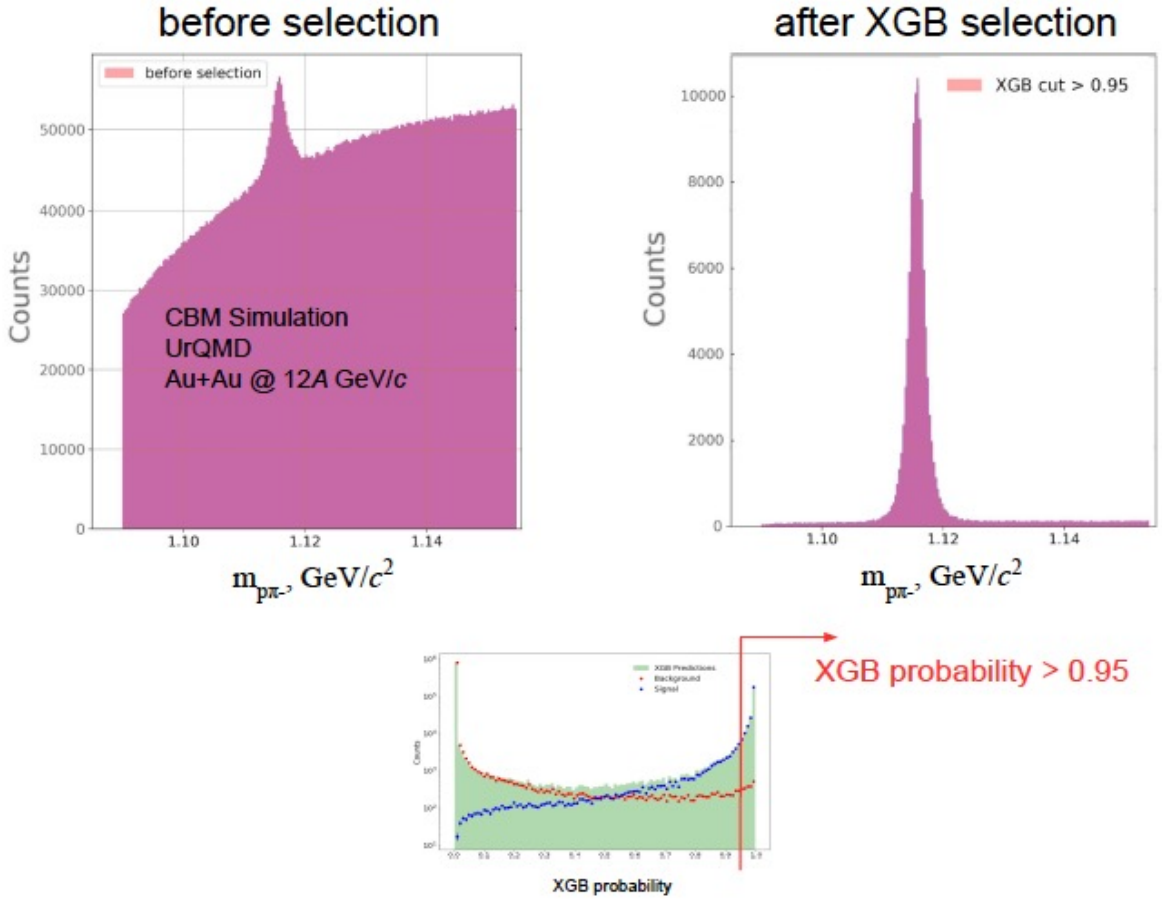
(Multi)-strange hyperons reconstruction at CBM



CBM simulation, Au+Au collisions @ 12*A* GeV/*c*

I. Selyushenkov, Mini-symposium "Hyperons@FAIR, Oct. 2021

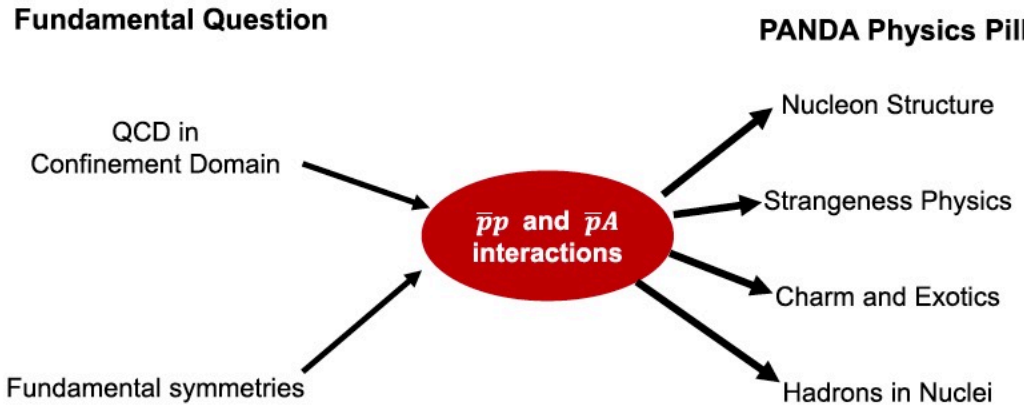
Example of Λ reconstruction via $\Lambda \rightarrow p\pi^-$

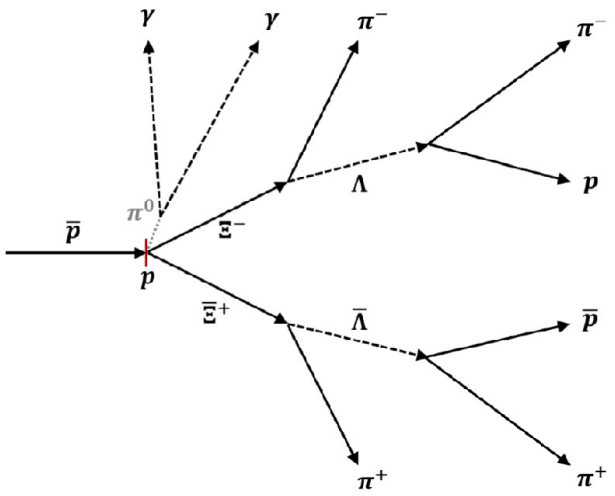


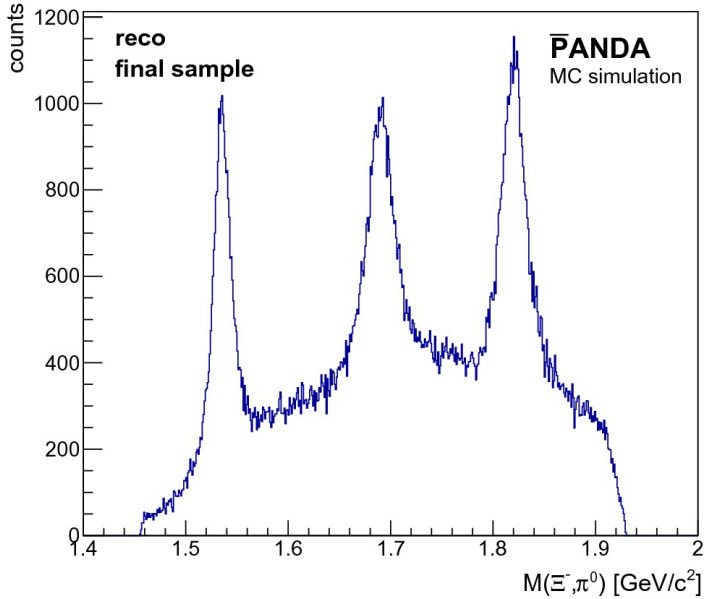
Lambda selection criteria are optimzed multi-dimensionally and non-linearly using Machine Learnig algorithms (XGBoost)

Progress in Task 3 – Data analysis challenge

- PANDA Phase One paper, *Eur. Phys. J. A* **57,** 184 (2021)
  - Outline of physics programme for the detector setup at the time of the delivery of the first antiproton beams at HESR
- The potential of Λ and Ξ^- studies with PANDA at FAIR, *Eur. Phys. J. A* **57,** 154 (2021)
- Study of excited Ξ baryons with the PANDA detector, *Eur. Phys. J. A* **57,** 149 (2021)







Progress in Task 4 – Outreach and education

Limited due to Covid-19 restrictions

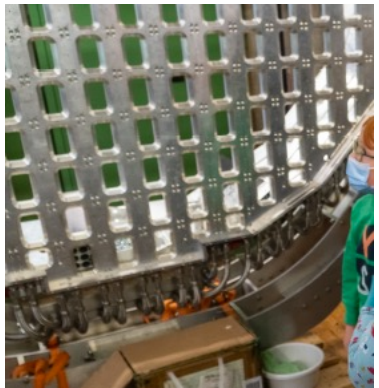
"Maus-Tag" October 3rd

Real-world stories instead of television

34 kids split into 10 groups

- Presentation of PANDA and strong interaction
- Explanation of the electromagnetic calorimeter
- Lab visits
- Model of a linear particle accelerator
- FAIR drone videos: https://www.youtube.com/watch?v=Y82ZeLH1vZs
- Hands on: Turning lemons into batteries

Model of linear accelerator as a game



2. Deviations from planned objectives and tasks, and their impact on the progress of the Work Package

Task 1: Front-end electronics, DAQ and Online

- delays in production and test of electronics
  - ToAST ASIC: Expected in July, delayed to October due to fab overload
  - Data Concentrator delayed due limited resources at the company, delay in PCB
  - Shortage of electronic components: price increase and delivery times of up to 1 year for FPGAs, controllers and even simple buffers
- plan to catch up in order to reach the objectives

Task 2: Demonstrator

- mCBM@SIS18 experiment
  - Travel restrictions, thus local personnel increased (funding adjustments)
  - Objectives will be reached
- Demonstrator at COSY/Jülich
  - Delays in preparation due to restricted lab access
  - Try to reach goals in 2023

Task 3: Data analysis challenge

- Work independent of location, no major delays

Task 4: Outreach and education

- Limited possibilities for on-site events, increase efforts once pandemic restrictions are gone

3. Deliverables and milestones

Deliverables (May 2023):

- Technical reports and user manuals
- Repository of software components

Milestones (November 2020):

- Repository – software released (done)