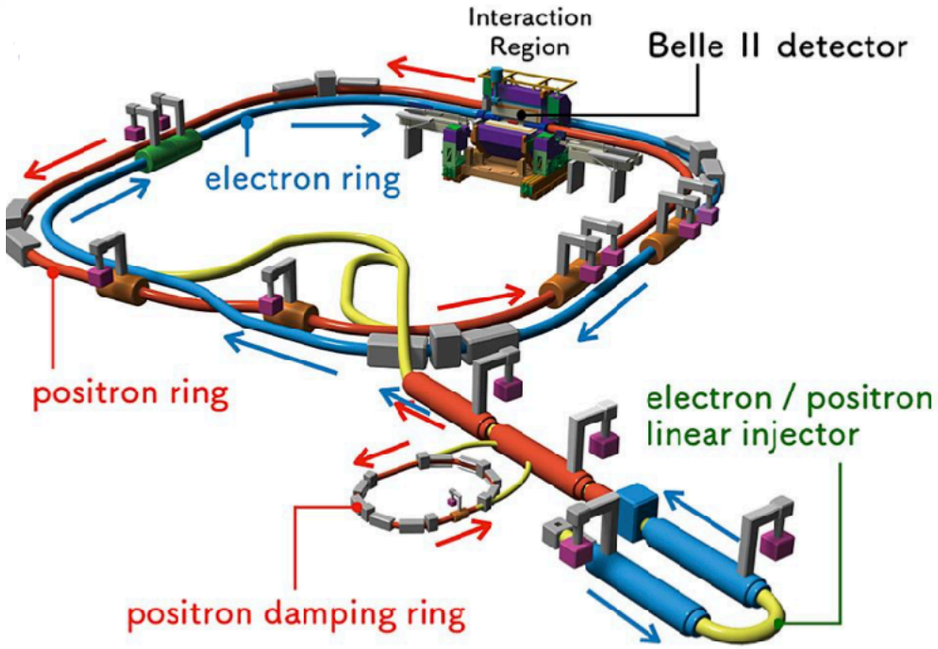
# Belle II upgrade

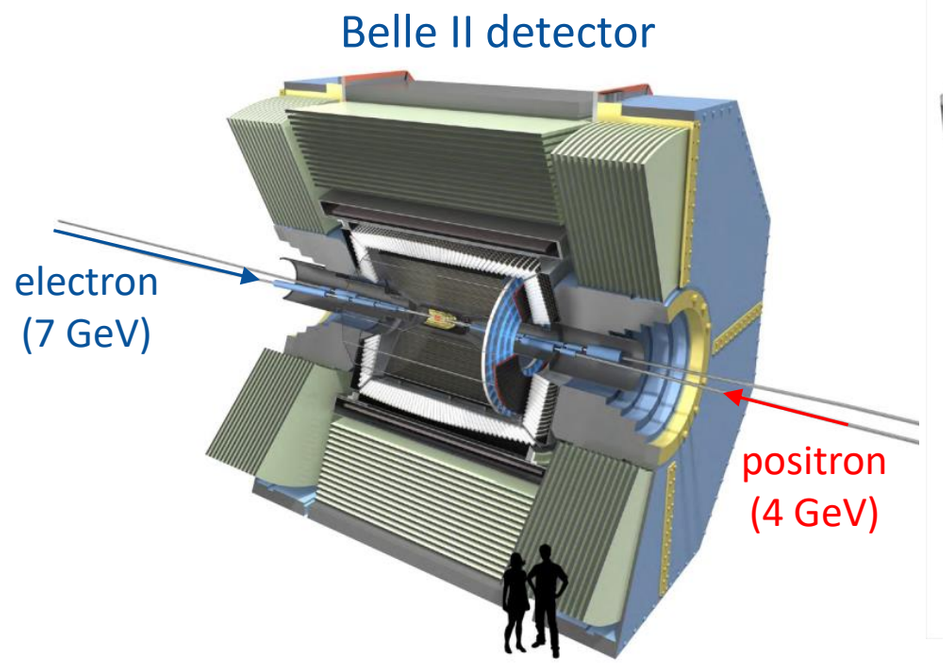
## (vertex detector)

Christian Finck
on behalf of IPHC team

GDR-InF annual meeting

# SuperKEKB collider

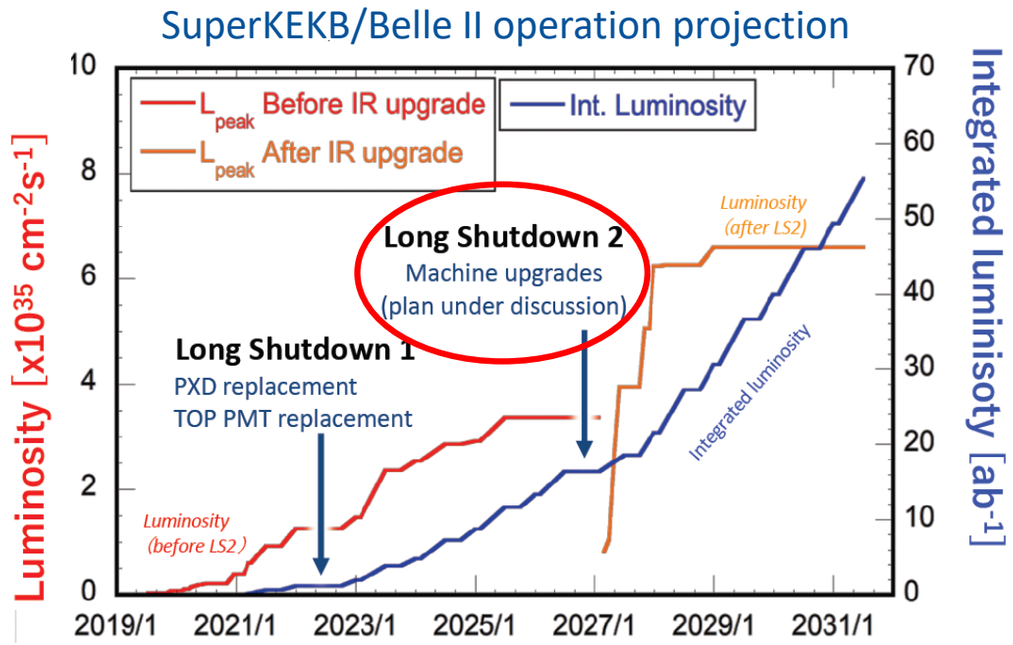



- Luminosity-frontier experiment exploring physics beyond the standard model
  - Today peak luminosity: $2.4 \cdot 10^{34}\, cm^{-2}s^{-1}$ $(219\, fb^{-1})$
  - Goal peak luminosity: $\sim 6 \cdot 10^{35}\, cm^{-2}s^{-1}$ $(\sim 50\, ab^{-1})$
- Nano-beam scheme, high current

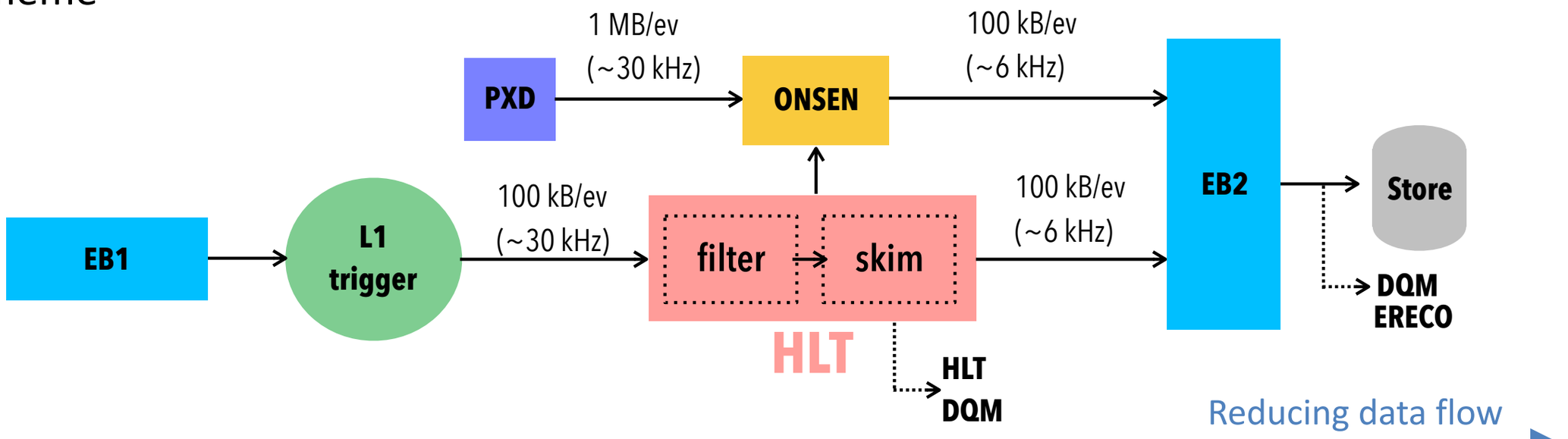
➡ High collision rate, high induced background

➡ Opportunity for detector's upgrade in 2026



# Challenges
## (Hardware side)

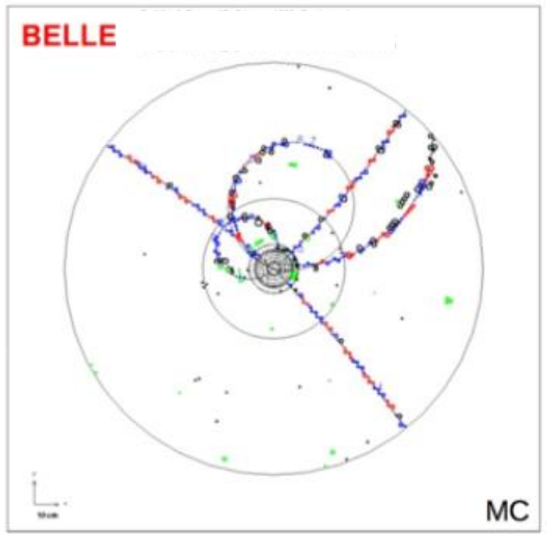
HLT scheme

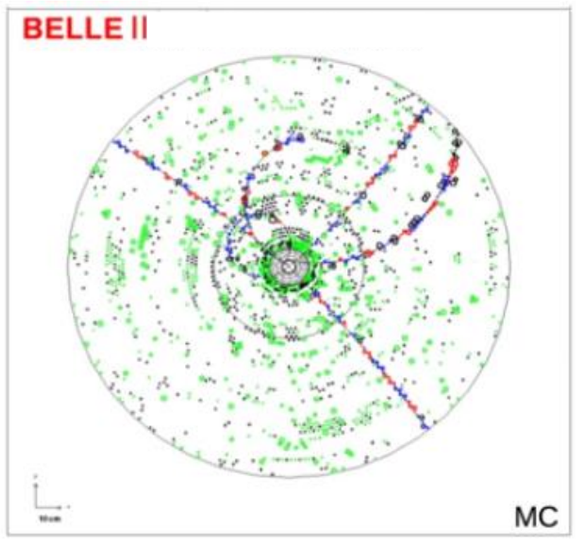


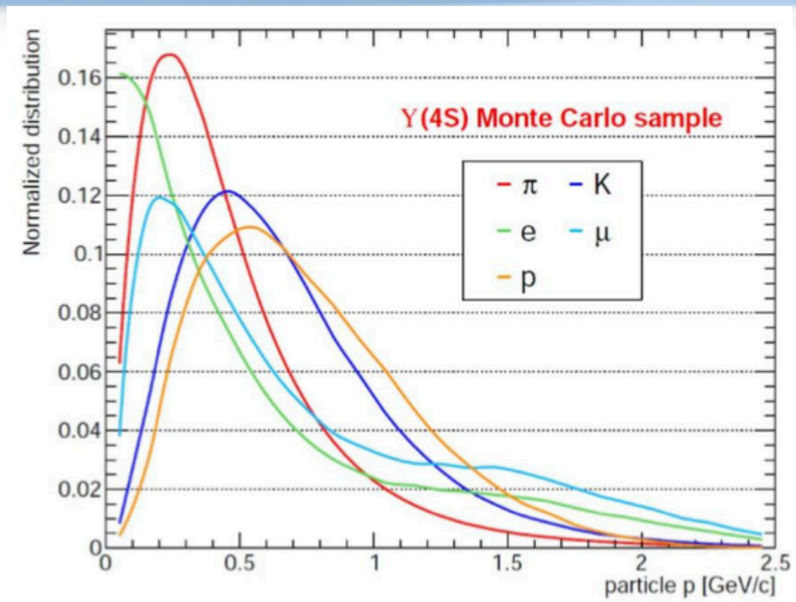

- Not all vertex detectors  are in the HLT scheme
  - dedicated HLT algorithm for PXD
  - All other detectors have another HLT
  - ➡ include all detector in on HLT scheme

➡ Reducing the bandwidth of data flow

# Challenges
## (Software side)



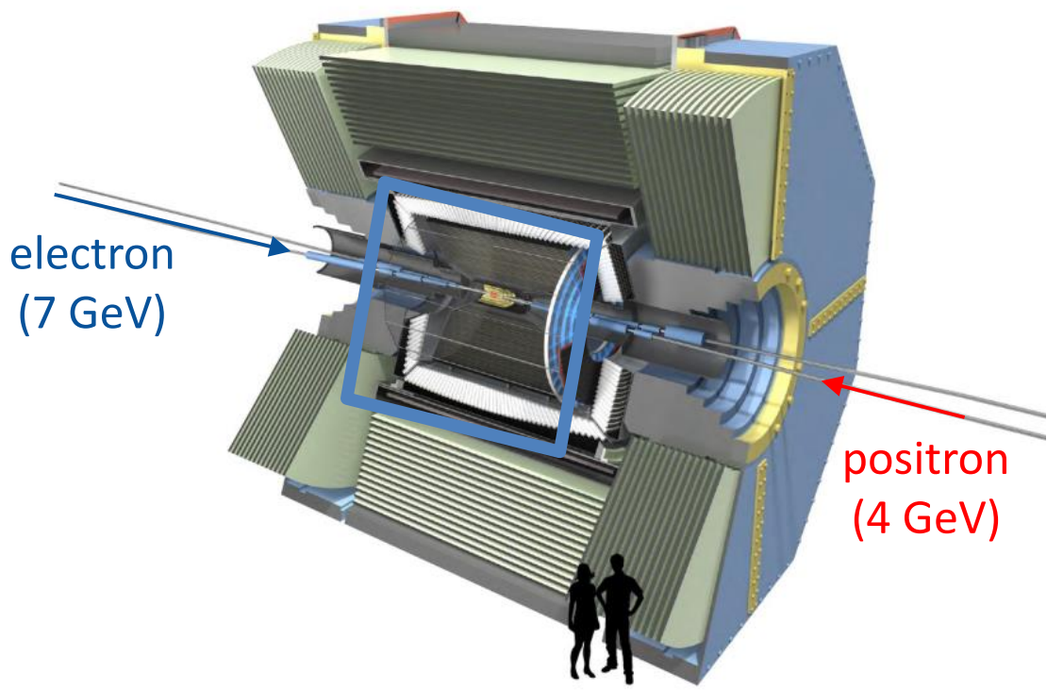



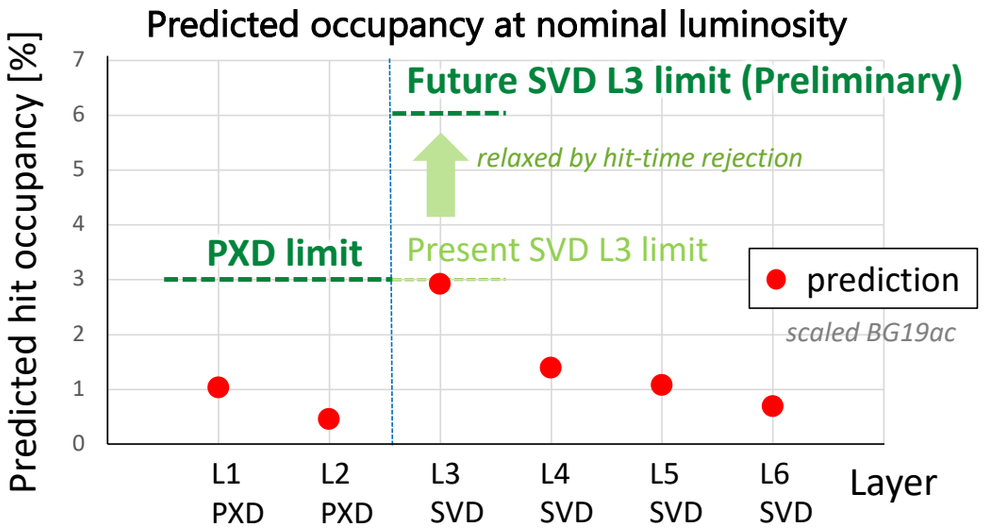

- Average track multiplicity: ~10
  - including low momentum particles (curling tracks, multiple-scattering)
  - embedded in a high beam-induced background
  - ➡ occupancy dominated with background hits

- Challenging with increasing Bkg for:
  - Central drift chamber: CDC
  - Vertex detector: VXD (PXD+SVD)

Belle II detector

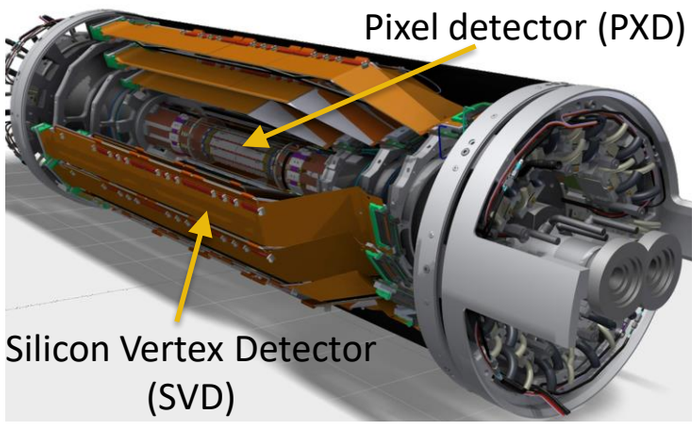


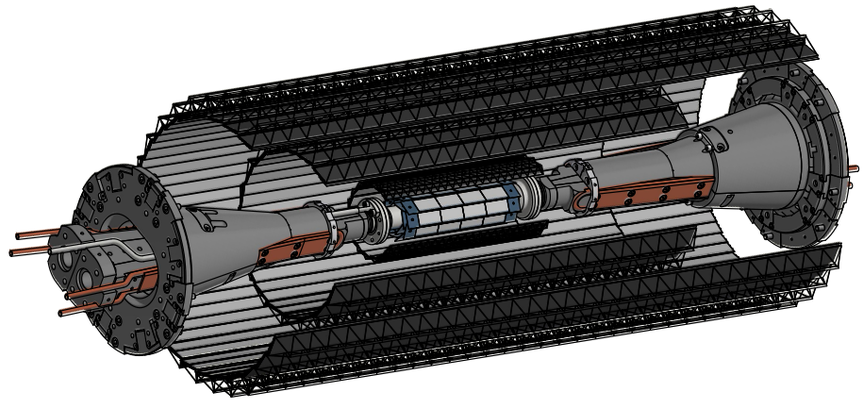
# Vertex Upgrade




- With a VTX project, occupancy should decrease to $10^{-4}$ level, better safety margin against Bkg level uncertainties:
- $$occupancy \propto \frac{t_{integration}}{granularity}$$

- Decreasing time integration, increasing granularity
  - ➡ Fully pixelized and fast detector



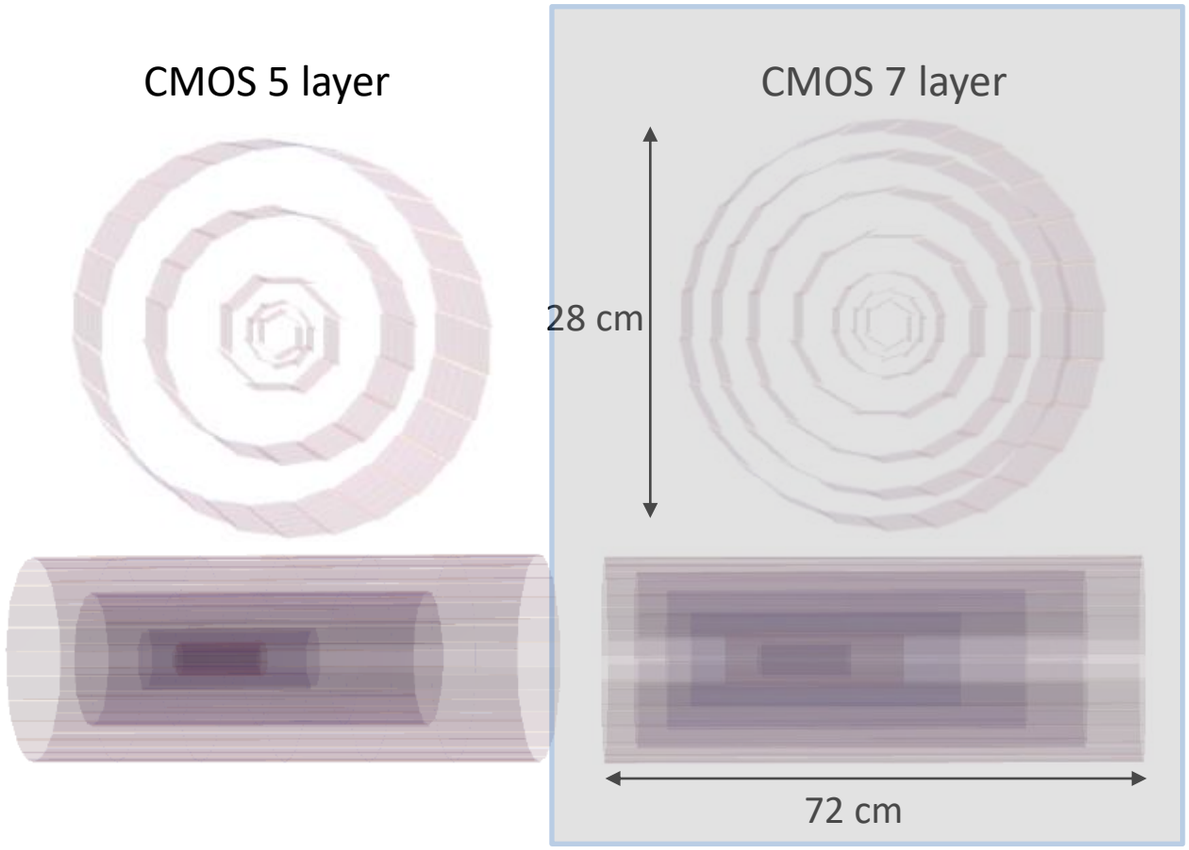
- Proposed technology:
  - Thin DSSD (140 µm)
  - Upgraded DepFet pixel
  - Dual Time CMOS pixel (DuTip)
  - CMOS pixel: VTX

# VTX Project

VTX: replaces VXD (PXD+SVD)

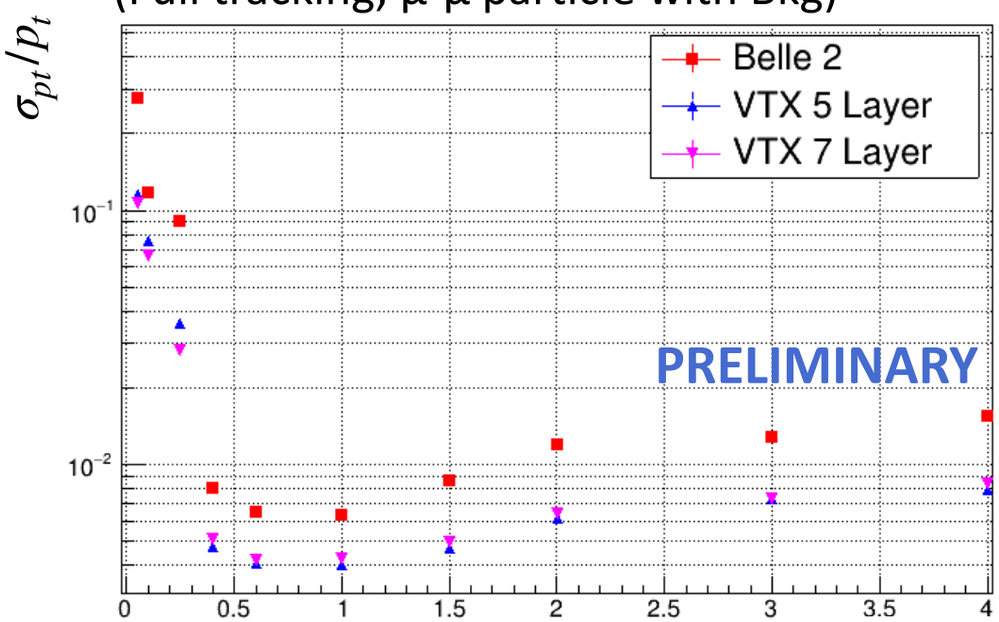
- Low material budget (50 µm thick sensor)
  - Total: < 1.5% of $X_0$
- Depleted monolithic active CMOS pixel sensor
  - size: ~2x3 $cm^2$
  - pitch: 30-40 $\mu m^2$
  - fast integration time: 25-100 ns
- Hit rate
  - ~120MHz.$cm^{-2}$
- Power dispersion
  - 100 mW.$cm^{-2}$
- Integration in the HLT level decision
  - lower data flow bandwidth
- Mitigating service bulkiness
  - less cabling and cooling pipes

- Layout
  - CMOS 5 layers
  - CMOS 7 layers

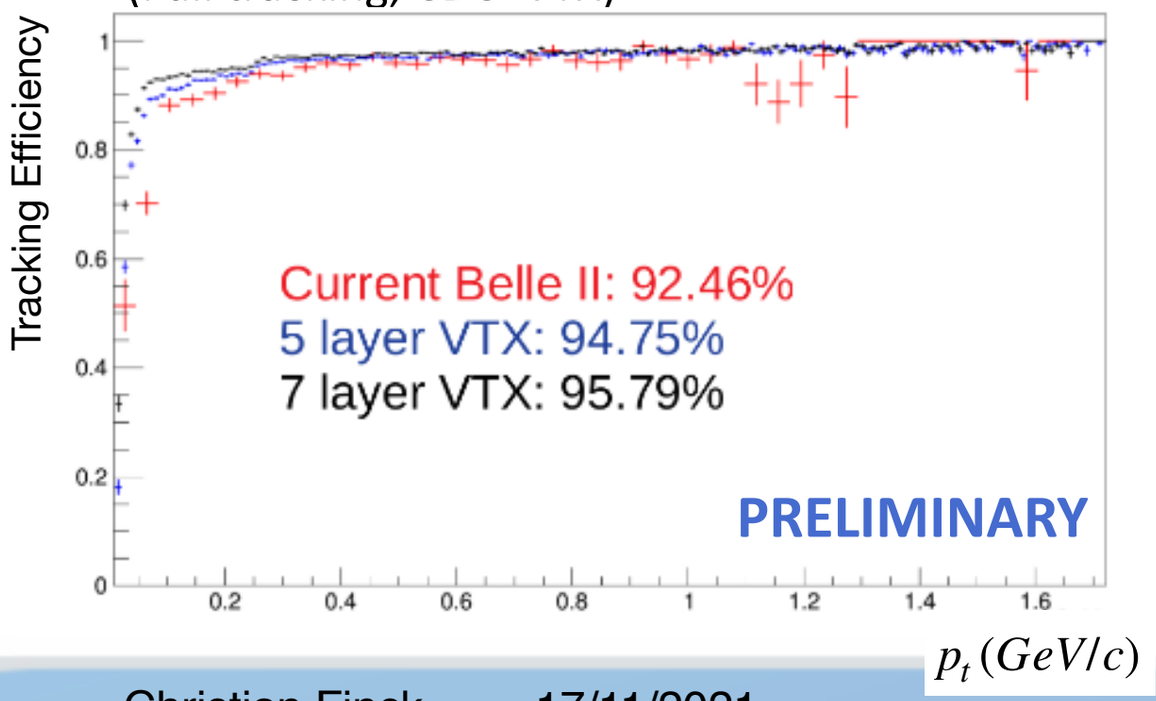


# VTX Performances

- Transverse momentum resolution vs $p_t$
  (Full tracking, μ-μ particle with Bkg)




- Tracking efficiency vs $p_t$
  (Full tracking, CDC+VTX)




- Total tracking efficiency

| | Bkg x 1 | Bkg x 5 |
|---|---|---|
| SVD | 0.961 | 0.907 |
| VTX (5 layers) | 0.984 | 0.979 |
| VTX (7 layers) | 0.987 | 0.978 |

- Occupancy
  - VTX layer 1: 0.002%
    (3 order of magnitude lower than for VXD)

- Fake rate
  - Comparable to SVD

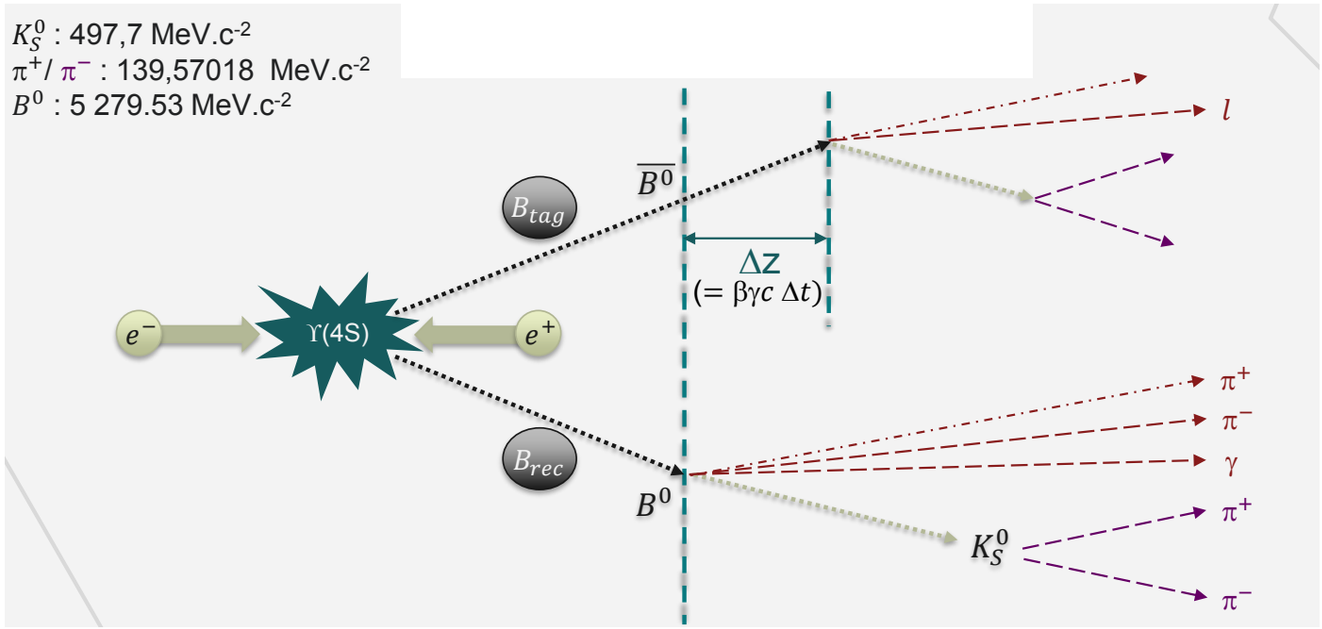
➡ Better performance at low $p_t$

➡ More robust against increasing Bkg

➡ Lower occupancy

# Impact on physics
## (as an example)

- Time dependent CP violation (TDCPV): $B^0 \to K^0_S \pi^+ \pi^- \gamma$




- $K^0_S$ vertex resolution @ Bkg x 1

| | ResX (µm) | ResY (µm) | ResZ (µm) |
|---|---|---|---|
| SVD | 64 ± 3 | 67 ± 3 | 61 ± 2 |
| VTX (5 layers) | 58 ± 2 | 52 ± 3 | 58 ± 2 |
| VTX (7 layers) | 44 ± 2 | 46 ± 2 | 39 ± 1 |

- $\Delta t$ time resolution btw $B_{rec}$ and $B_{tag}$ @ Bkg x 1

| | Δt (ps) |
|---|---|
| SVD | 4.0 ± 0.2 |
| VTX (5 layers) | 3.7 ± 0.2 |
| VTX (7 layers) | 3.6 ± 0.2 |

➡ Better spatial resolution (gain ~20-30%)

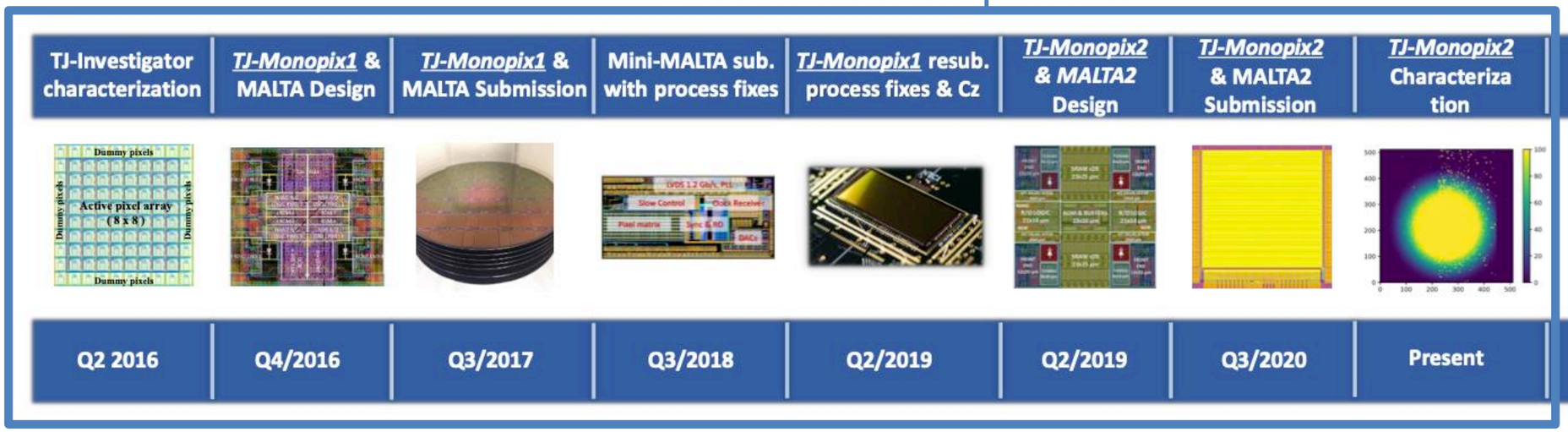
➡ Better time resolution (gain ~10%)

➡ Better reconstruction

# Sensor ongoing activities

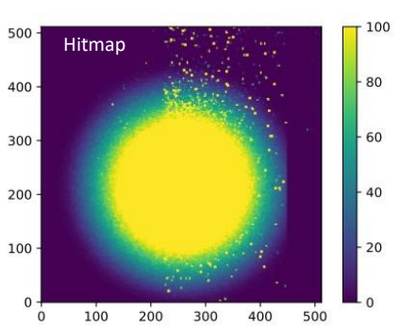
- TJ-MONOPIX family

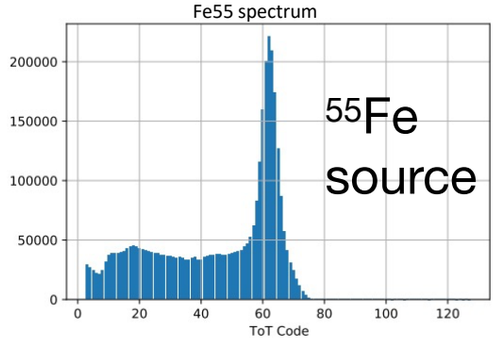
External developments

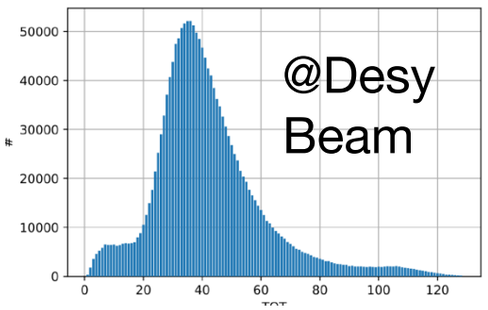



Optimized **BEL**LE2 p**IX**el

➡ Benefits from past year of R&D and from large expertise on TJ-180nm




- TJ-Monopix2 produced, received and tests started

➡ First complete prototype OBELIX-1 targeted in 2022

- Digital design starting
- Analogue design still under organisation

➡ Other ongoing activities

- Mechanics studies
- Thermomechanics studies
- Transmission lines studies

# Conclusions

➡ Opportunity for a more powerful VTX detector in 2026

- First performance studies show:
  - Better performance at low $p_t$
  - More robust against increasing Bkg
  - Lower occupancy

- Better space resolution in physics channel

- Baseline technology from TJ-Monopix2

# Perspectives

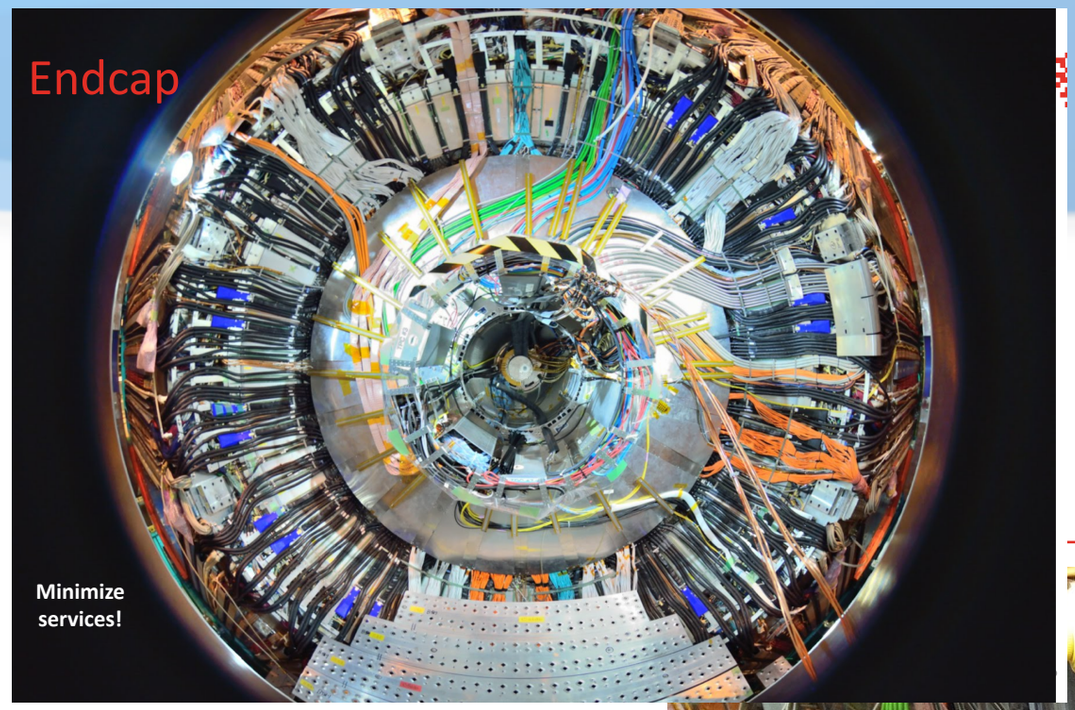
- Writing the Conceptual Design Report for end of 2022
- Performance studies, prototyping of sensor, detection elements (modules & ladders)
- French contribution:
  - Design of OBELIX-1 + performance tests (CPPM and IPHC)
    - ➡ Submission prototype 2022, test until 2023
  - Tests and thermic studies, impact on HLT (IJCLAB)

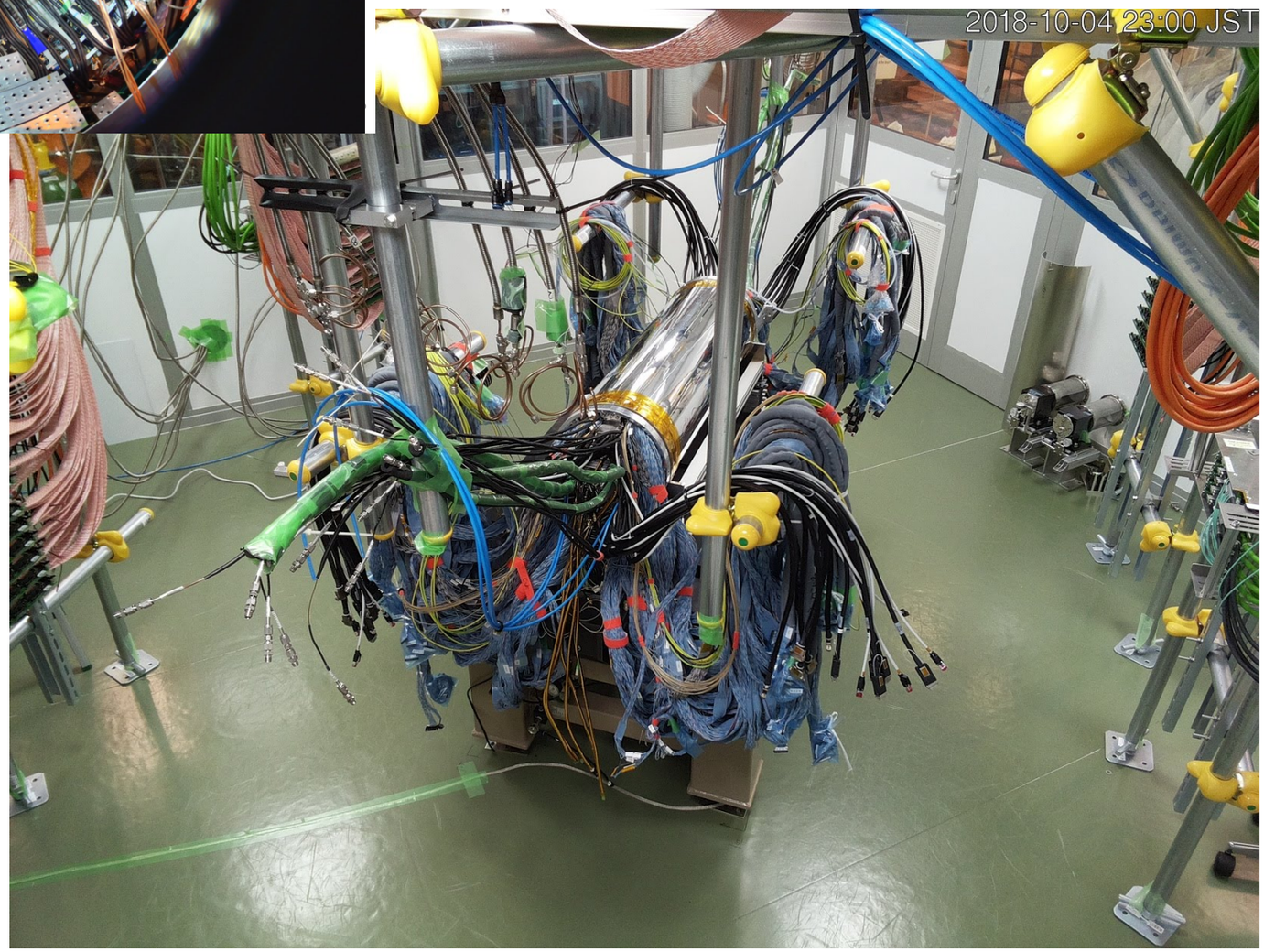
**Proposal of an all-layer monolithic pixel vertex detector for the Belle II upgrade**

O. Alonso, F. Arteche, M. Barbero, J. Baudot*, F. Bernlochner, S. Bettarini*, J. Ceballos, J. Dingfelder*, F. Forti, A. Frey, S. Grinstein, C. Marinas*, G. Pellegrini, I. Peric, V. Re, C. Schwanda, B. Schwenker*, K. Trabelsi*, I. Vila, on behalf of:

HEPHY, Vienna (Austria)
CPPM, Marseille (France)
IJCLab, Orsay (France)
IPHC, Strasbourg (France)
University of Bonn, Bonn (Germany)
University of Goettingen, Goettingen (Germany)
KIT, Karlsruhe (Germany)
University of Bergamo, Bergamo (Italy)
INFN, Pavia (Italy)
INFN & University of Pisa, Pisa (Italy)
IFAE, Barcelona (Spain)
IMB-CNM-CSIC, Barcelona (Spain)
University of Barcelona, Barcelona (Spain)
IFCA (CSIC-UC), Santander (Spain)
IMSE-CNM-CSIC, Seville (Spain)
IFIC (CSIC-UV), Valencia (Spain)
ITAINNOVA, Zaragoza (Spain)

# Backup




Note: Only less than 50% of PXD installed here

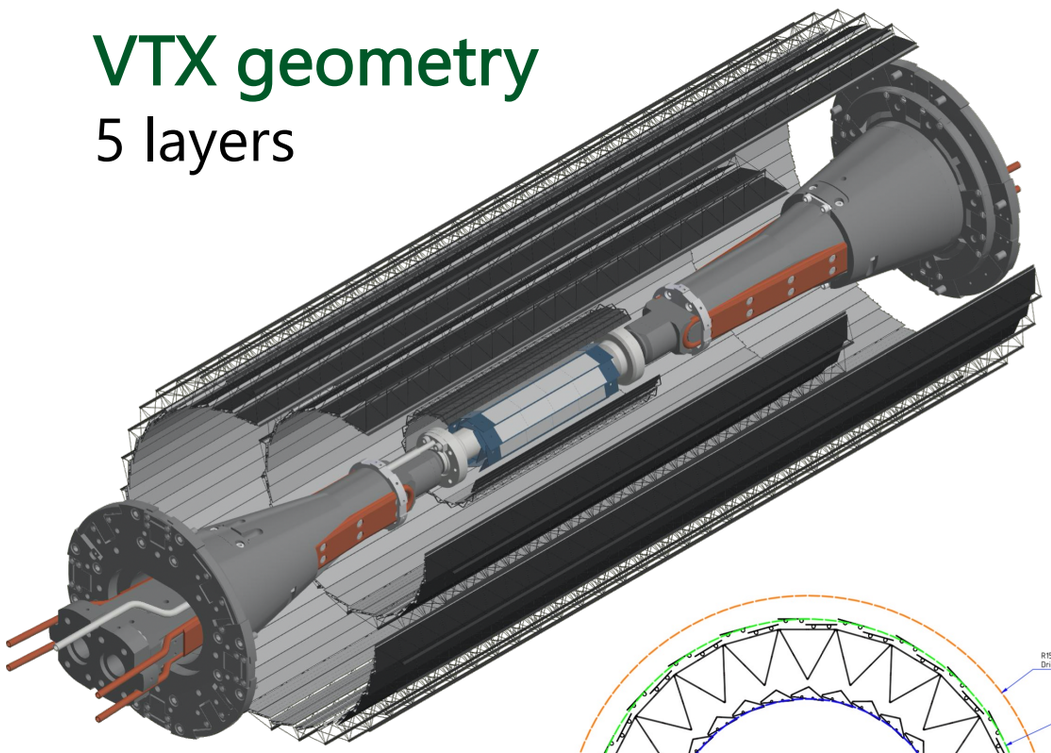
cmarinas@ific.uv.es

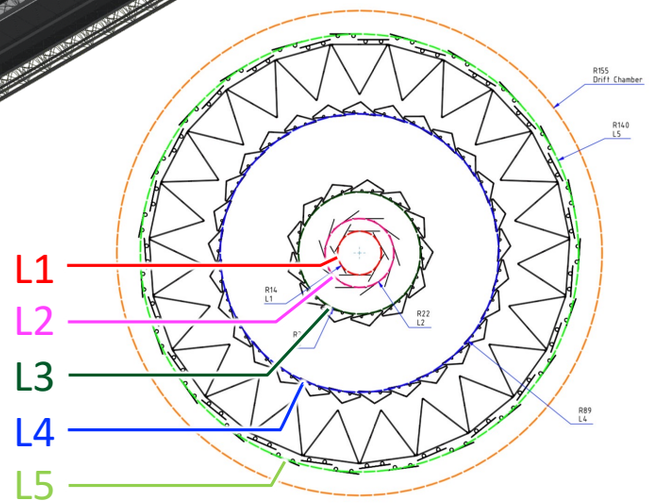
| | MONOPIX-2 | OBELIX-2 (Belle II final) |
|---|---|---|
| Taille du capteur | 2×2 $cm^2$ | $2 \times 3\ cm^2$ |
| Taille du pixel | 33×33 $\mu m^2$ | < 40×40 $\mu m^2$ |
| Temps d'intégration | 25 ns | 100 ns |
| Dissipation | 170 mW $cm^{-2}$ | 100 mW $cm^{-2}$ |
| Trigger | - | 30 kHz |
| Débit de données | xx | 320 Mbits $s^{-1}$ |
| Digitisation | 7 bits | 7 bits |
| Tenue aux radiations | $1\times10^{15}$ n $cm^{-2}$ | 100 MRad<br>$1\times10^{14}$ n $cm^{-2}$ |
| Budget de matière couches L1-L2 | 0.1 % $X_0$ | 0.1-0.2 % $X_0$ |
| Budget de matière couches L3 to L5 | | 0.3 to 0.5 % $X_0$ |

# VTX: An integrated design for fully pixelated option

## VTX geometry

5 layers

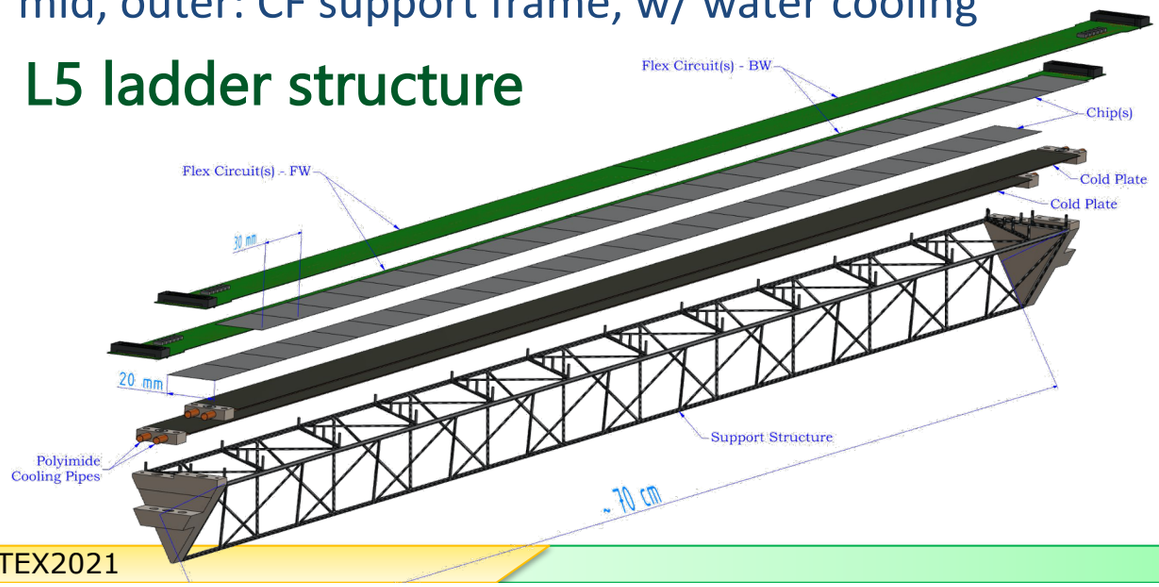





## General concept of VTX

- **Fully pixelated detector with CMOS sensors**
  - Chip size: 2x3 $cm^2$ (same chip in all layers)
- **Low material budget:**
  - sensor thickness ~50 µm
  - 0.1%$X_0$ (L1-2) / 0.3%$X_0$ (L3-4) / 0.8% $X_0$ (L5) per layer
- **Different integration among inner (L1-2), middle (L3-4), and outer (L5) layers**
  - inner: Self supportive silicon ladders, w/ air cooling
  - mid, outer: CF support frame, w/ water cooling

## L5 ladder structure






Katsuro Nakamura

UNIVERSITÄT BONN

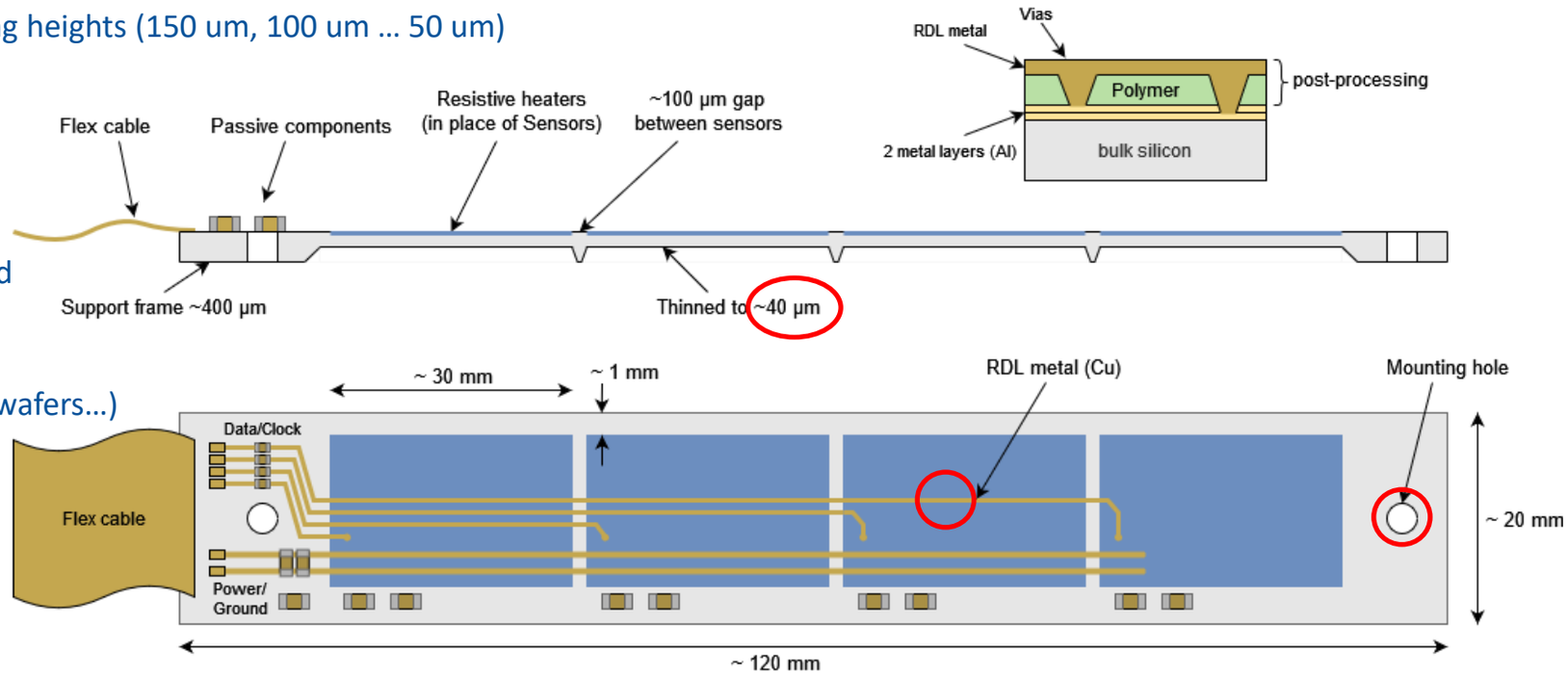
# IVTX DEMONSTRATOR

Plan: 2 runs

1. Proof of concept for the **RDL**, heaters etc.
   - Unthinned wafer
   - **Electrical studies**
2. Evaluation of the **thinning process**
   - Several wafers thinned to different decreasing heights (150 um, 100 um … 50 um)
   - Same mask set as run 1
   - Thermal and mechanical studies

Potential issues raised by IZM

- **Mounting holes** → Gluing/clamping preferred
- **Thinning** the active area to 40 µm
  → ~20 µm process variation, homogeneity
  → Asked to think of alternatives (SOI, gluing wafers…)
- Length of RDL metal lines:
  **Minimum width** of ~20 µm can lead to interruptions along the module
  → wider traces



# Thin and fine-pitch DSSD

@ KEK

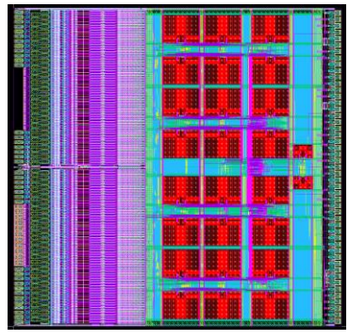
- Main R&D targets
  - Handling higher hit-rate / SVD
    - 10 MHz/cm$^2$ (radii>3 cm)
  - Improved resolution $\sigma_z$ & decrease material budget
  - Longer trigger latency & rate

- R&D paths
  - Shorter strips
  - Finer pitch
  - Thinner sensor

- R&D challenges
  - Heat dissipation (larger #chan.)
  - Noise reduction (lower signal)

- Solutions
  - **Double-Sided Sensors** prototyped by Micron
  - **Front-End ASIC = SNAP128A** under dvpmt
    - Based on SliT chip for g-2 (J-PARC experiment)
    - 180 nm CMOS process

| | **Sensor** dim. | Thickness | Pitch P-side | Pitch N-side |
|---|---|---|---|---|
| Current | 40x125 mm$^2$<br>60x125 mm$^2$ | 300-320 µm | 50-75 µm | 160-240 µm |
| | (with intermediate strip) | | | |
| **Upgrade** | 51.2x57.6 mm$^2$ | 140 µm | 50 µm | 75 µm |




- ENC = 650 e-
- Total power 2.8 mW/chan.
- 127 MHz output
- $\sigma_t$ ~ 8 ns
- 2k-depth memory → latency ~16 µs

⇒ K.Nakamura Development of thin and fine-pitch DSSD poster

⇒ First Sensor+FEE in 2021



➡ thin DSSD, indeed an available techno, it is still to be demontrated that a satisfactory SNR after irradiation for such thin sensors. We should know current 2022.

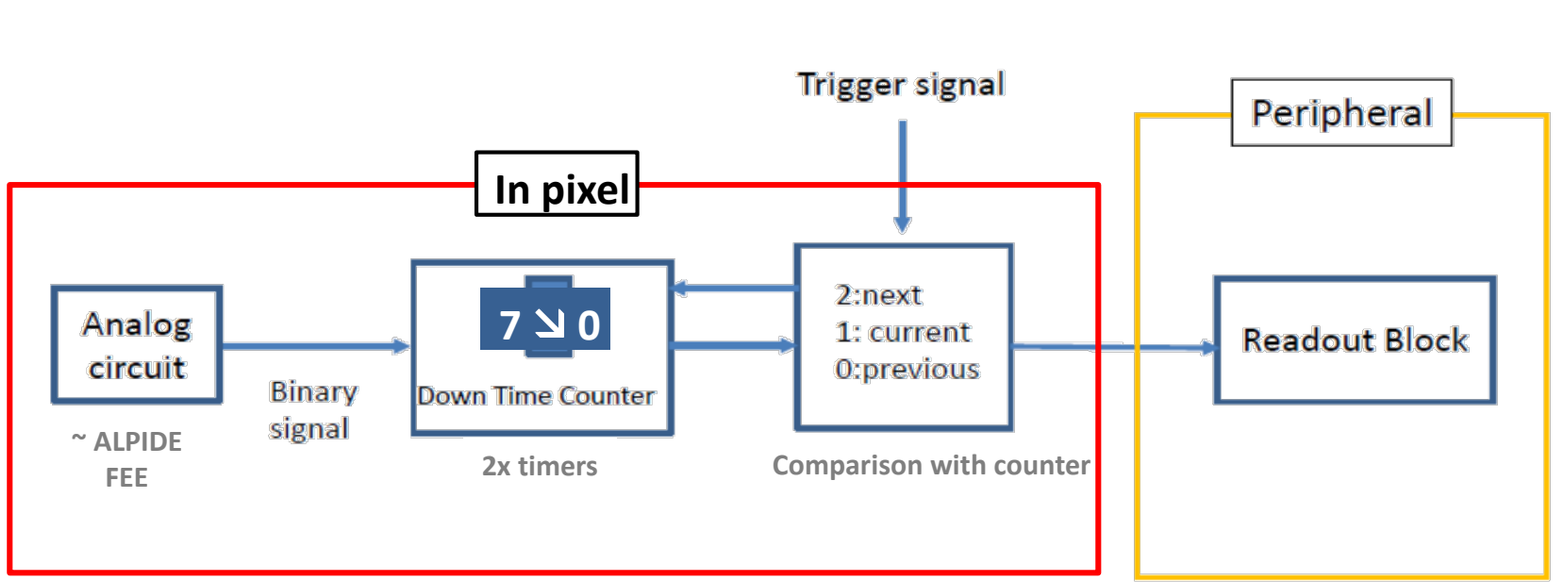
# DuTiP - SOI pixel sensors

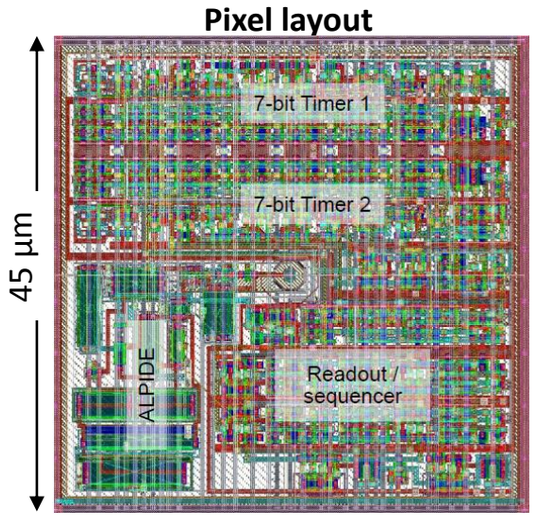
- Main R&D targets
  - Low material budget
    - Monolithic technolgy
  - Handling high-rate
    - Time-stamping < 100 ns
    - Global-shutter style

@ KEK

- Dual Timer Pixel concept
  - 16 MHz clock for TIMER
  - 2x 60 ns "integration" window
  - Trigger latency 8 µs
  - Occupancy << 0.1 %

- SOI Implementation
  - 0.2 µm LAPIS
  - Full depletion
  - Pixel pitch 45x45 µm$^2$
  - Sensitive thickness 50-75 µm




⇒ M.Yamada R&D status of monolithic SOI pixel sensor for vertex detector talk on Wed.

⇒ Initial prototype DuTIP 1 submission in Nov.2020



➡ DUTIP with SOI techno, they R&D is going well on this techno which is only available in Japan. They will demonstrate some performance with initial prototypes next year. Time will be certainly short for them to be ready for 2026.

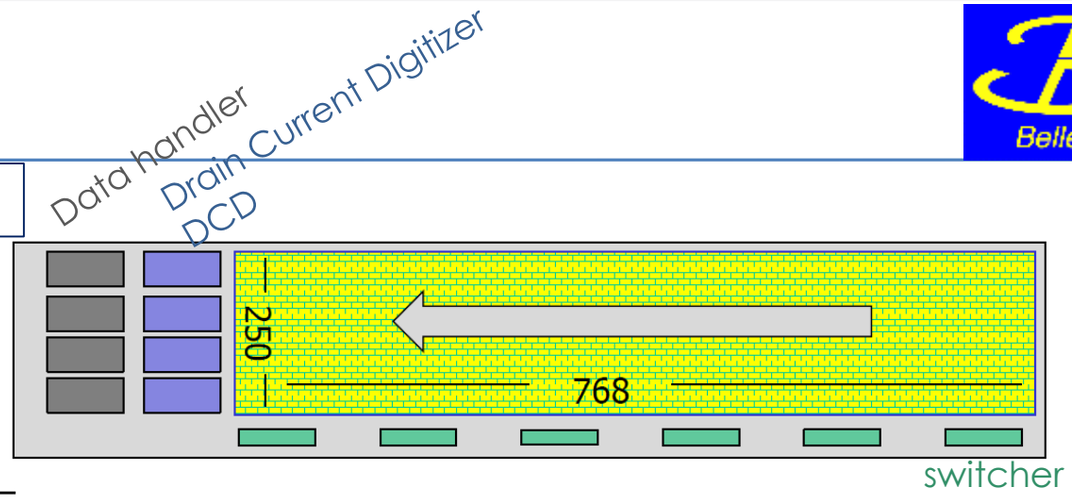
# DEPFET pixel sensors

Belle II DEPFET collaboration

- Current Belle II - PXD
  - First use of the technology in HEP experiment
  - Many lessons learned

- R&D directions
  - Gain increase with shorter FET length L
    → thinner oxide
    → higher signal → improved rad. tolerance

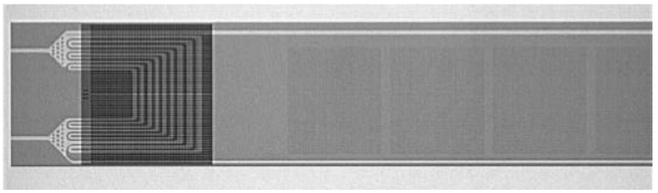
$$g = \frac{\mathrm{d}I_{\mathrm{drain}}}{\mathrm{d}Q} \propto \sqrt{\frac{t_{\mathrm{ox}}}{L^3}}$$

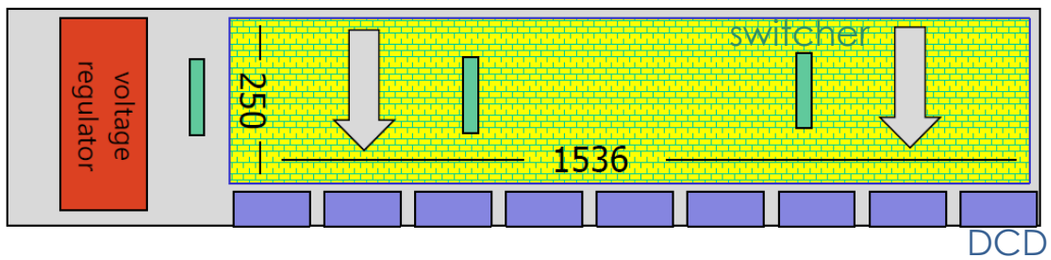



- Rotating read-out direction + switcher intergration
  - Speed x3
  - Pixel size along beam x1/2

- Faster driving & read-out circuits
  - Require advanced processed
  - Speed x2

- **All-silicon module** improvements
  - Microchannel cooling
  - Thinner drivers






- Within reach
  - $T_{int}$: 20 ↘ 3 µs
  - Improved $\sigma_z$
  - Mat. budget 0.21 ↘ 0.15 % $X_0$



➡ Upgraded DEPFET, a significant R&D is needed there… the major pb is that there is so far no manpower

# CMOS pixel sensor optionS

⇒ Various R&D on-going outside Belle II

⇒ Monolithic sessions on Wednesday

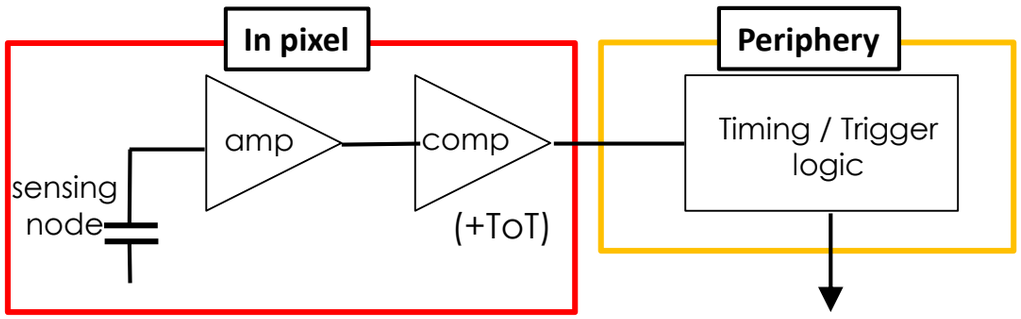
| Sensor available 2020 | MIMOSIS-1 (CBM-MVD) | Belle II requirements "First guess" | MONOPIX-2 (ATLAS-ITK) | ATLASPix3 (ATLAS-ITK) |
|---|---|---|---|---|
| **Time precision (ns)** | 5000 | **50 to 100** | 25 | 25 |
| **Pixel pitch (μm²)** | 30x27 | **30x30 to 40x40** | 33x33 | 150x50 |
| **TID (Mrad)** | 5 | **10** | 100 | |
| **Power (mW/cm²)** | ~50 | **< 100 to 200** | ~150 | ? |
| **Trigger delay (μs)** | No trigger | **5 → 10** | long | |

In test IPHC

Submitted Bonn, CERN, CPPM

Tested Barcelona, CPPM, Geneva, Heidelberg, KIT, Liverpool

180 nm HR-CMOS process → ~full depletion ← 180 nm HV-CMOS process




- Demonstrated
  - Monolithic & low power → low material budget granted
  - Excellent granularity → $\sigma_{s.p.}$ ~ 5-10 μm
  - Short integration → occupancy = $O(10^{-3})$

⇒ 1st dedicated version in 2021 ~ realistic



➡ CMOS: just the best compromise between availability/performance/possibility to be ready by 2026.

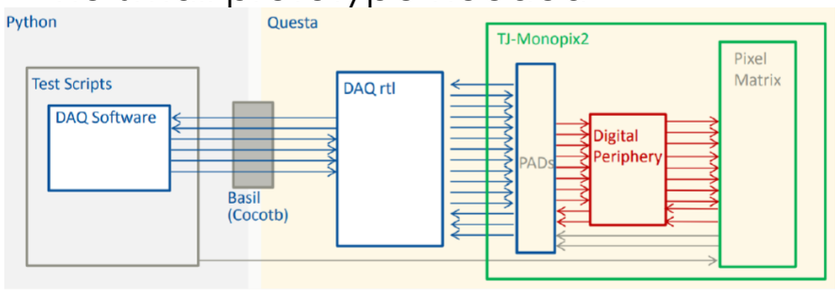
# Details of existing sensors

| Sensor available 2020 | ALPIDE | MIMOSIS-1 | TJMonopix-2 | LFMonopix-2 | ATLASPix-3 | Belle II |
|---|---|---|---|---|---|---|
| **Techno** | TJ-180 nm | TJ-180 nm | TJ-180 nm | LF-150 nm | TSI 180 nm | |
| **Pixel pitch ($\mu m^2$)** | 29x27 | 30x27 | 33x33 | 150x50 | 150x50 | **30 to 40** |
| **#Columns x #Rows** | 1024x512 | 1024x504 | 512x512 | 56x340 | 132x372 | |
| **Sensitive area ($cm^2$)** | 27.5x15.0 | 31.0x13.6 | 16.9x16.9 | 8.4x17 | 19.8x18.6 | **~30x20** |
| **Time Stamp (ns)** | 5000 | 5000 | 25 | 25 | 25 | **O(100)** |
| **Trigger latency (µs)** | Contin./Trig. 2 | Continuous | Global shutter | Continuous | 25 | **5 → 10** |
| **Output charge (bits)** | 1 | 1 | 7 | 6 | 7 | |
| **Bandwidth (Mbits/s)** | 1200 | 3200 | 320 | | 1300 | **O(320)** |
| **Power ($mW/cm^2$)** | 18-35 | ~50 | O(200) | | ~140 | **≤200** |
| **Hit rate ($Mhz/cm^2$)** | <10 | 15-70 | >100 | >100 | >100 | **≤150** |
| **TID kGy** | 27 | 100 | 1000 | | 1000 | **1000** |
| **Fluence (x $10^{13} n_{eq}.cm^{-2}$)** | 1.7 | 7 | 100 | 100 | 100 | **10** |

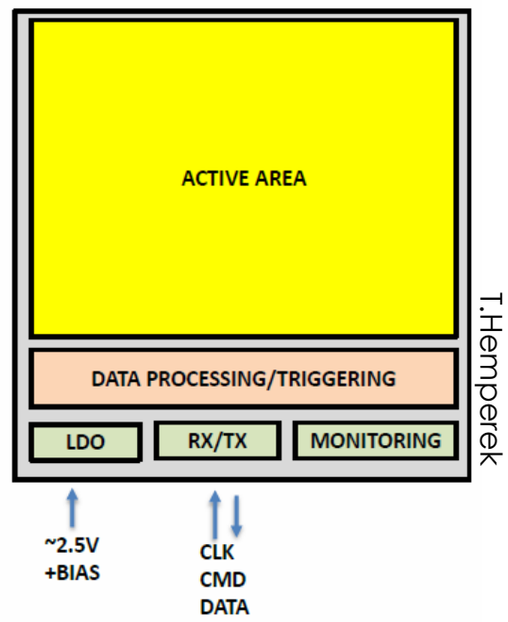
# From Monopix-2 to Optimized BELle II PIXel

- End-of-Column logic
  - Requirements based on
    - **largest hit-rate 150 MHz/cm²**
    - **2 pixels fired per hit**
    - **Longest trigger latency 10 µs**
    - **Wide matrix (896 pixels)**
    - **Long integration time 100 ns**
  - Digital design ⇨ no small prototype needed

- Memory size needed on sensor ~60 Kbytes
- Single output at 320 MHz
- Average bandwidth/sensor 140 Mbits/s



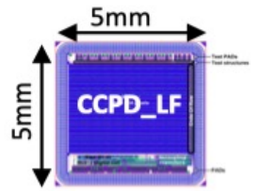

- About timing
  - 25 ns for pixels ⇨ = time-stamping
  - 50/100 ns for event ⇨ = sensitive window = integration time




T.Hemperek

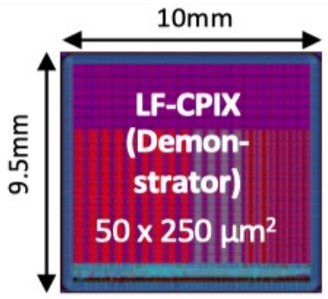
- Additional design work
  - Extend matrix width (TJ-180 nm max width = 31+ mm)
    - Expertise from MIMOSIS-1
  - Optimize powering scheme & data transmission
    - Expertise from MALTA (TJ-180nm) & RD53 (TSMS-65nm)

# TWO DEVELOPMENT LINES



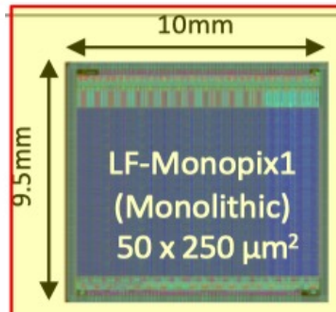

CCPD_LF

- *Subm.* ***Sep. 2014***
- *Fast R/O coupled to FE-I4*



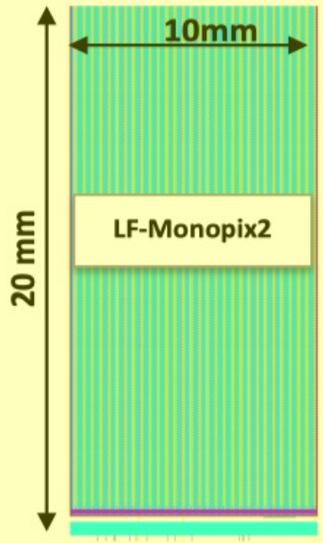

LF-CPIX (DEMO)

- *Subm.* ***Mar. 2016***
- *Fast R/O coupled to FE-I4*



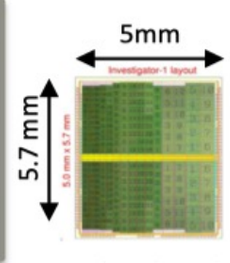

LF-Monopix1

- *Subm.* ***Aug. 2016***
- *Fast column drain R/O*



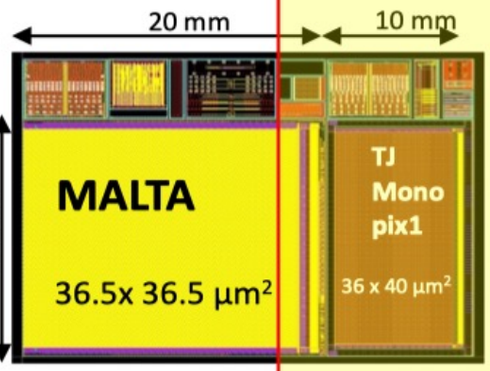

LF-Monopix2

- *subm.* **Q2/2020**
- *50 x 150 µm² pixels*
- *Full height matrix*
- *Fast column drain R/O*

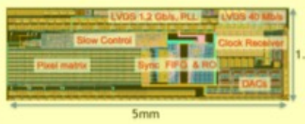

INVESTIGATOR

- ***2016***
- 8 x 8 pixel submatrices



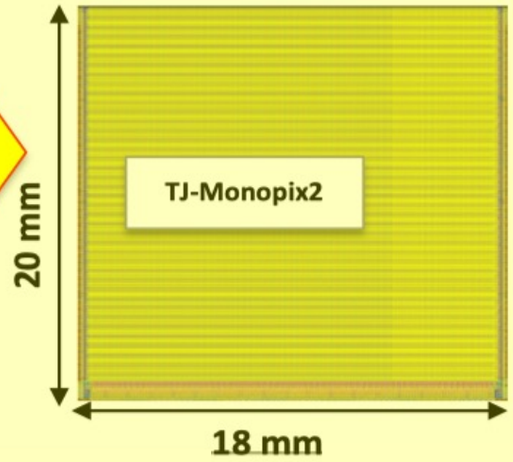

MALTA (asynchronous) & TJ-Monopix1 (column drain)

- subm. **2018**
- large matrices
- fast asynchr & col. drain R/O




miniMALTA

- subm. **2018**
- measures for rad. hardness




TJ-Monopix2

- *subm.* **Q4/2020**
- *33 x 33 µm² pixels*
- *Full height matrix*
- *Fast column drain R/O*

# Option 2: TJ-180 nm

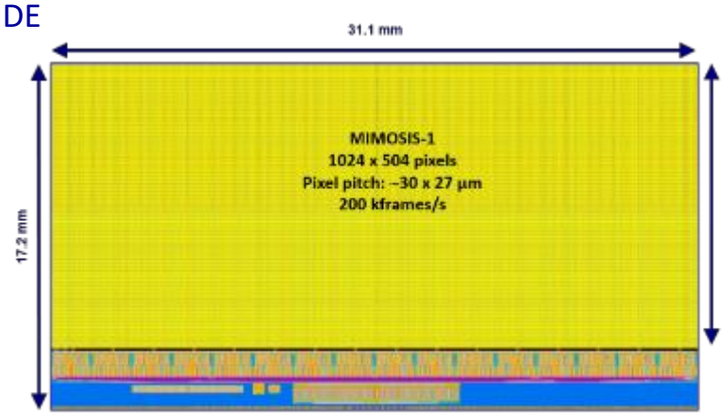
- Pixel array: 504 x 1024 pixels in 64 regions
- Pixel pitch: 26.88 x 30.24 µm²
- Active area: 30.97 x 13.55 mm²
- Chip dimension: 31.1 x 17.2 mm²
- **Integration time: 5 µs**

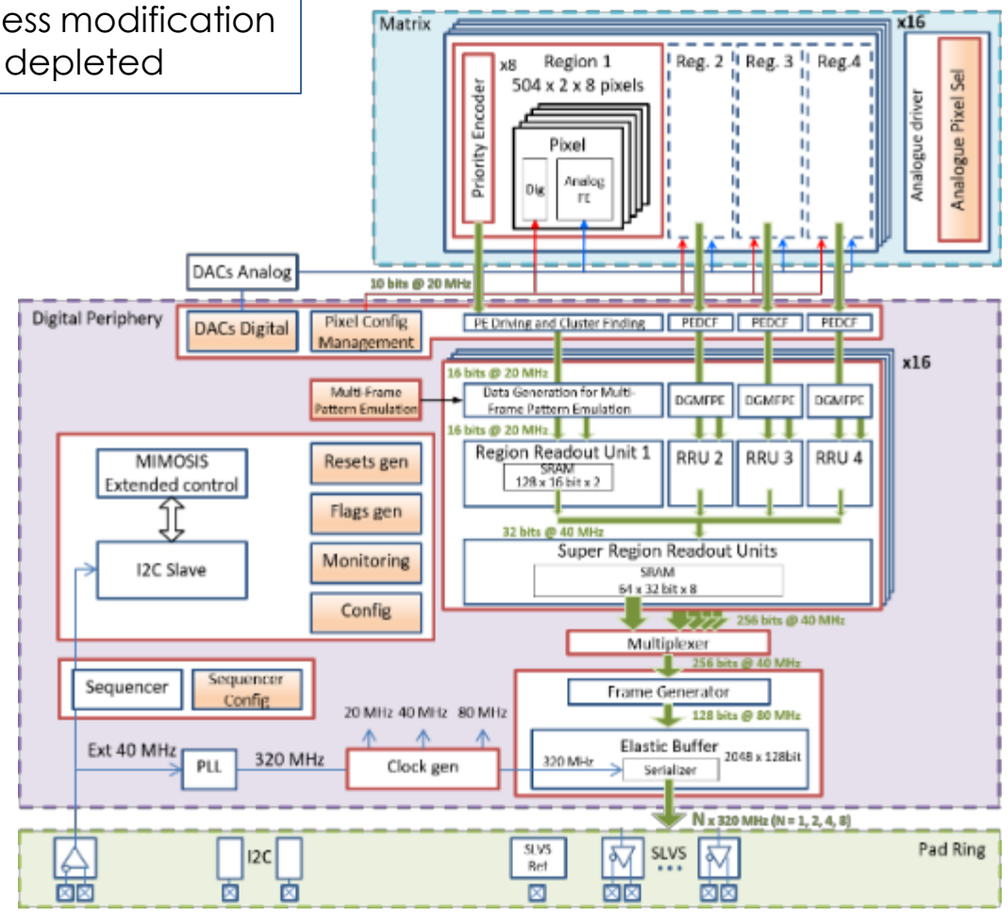
**MIMOSIS-1 sensor**
- Dvpmt by IPHC, IKF, GSI
- High resistivity with process modification but not necessarily fully depleted

- **Pixel matrix:**
  - Analog part of pixel similar to ALPIDE
  - 2 small-diode coupling options: DC & AC
  - Digital part of pixel redesigned: no trigger, leading-edge detect.
  - Priority encoder = ALPIDE with 20 or 40 MHz clock
- **Digital periphery:**
  - Fully reworked / ALPIDE
  - Multi-stage dataflow
  - Elastic buffer

- **Total Power ~ 50 mW/cm2**

- **1 to 8 Outputs:**
  - 320 MHz
  - Up to 2.5 Gbits/s



# TOWERJAZZ MONOPIX

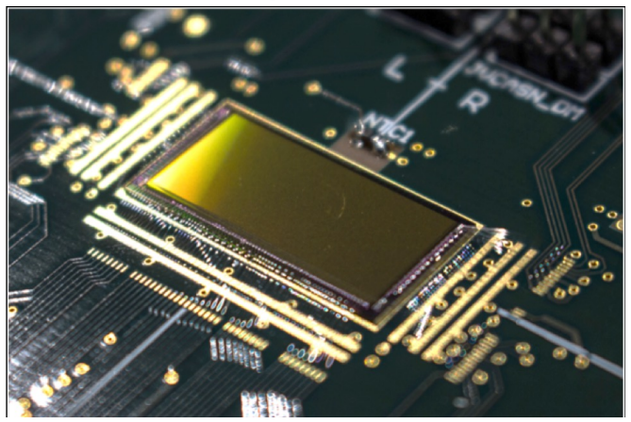
TowerJazz
180 nm CMOS
process

SiLAB Silizium Labor Bonn

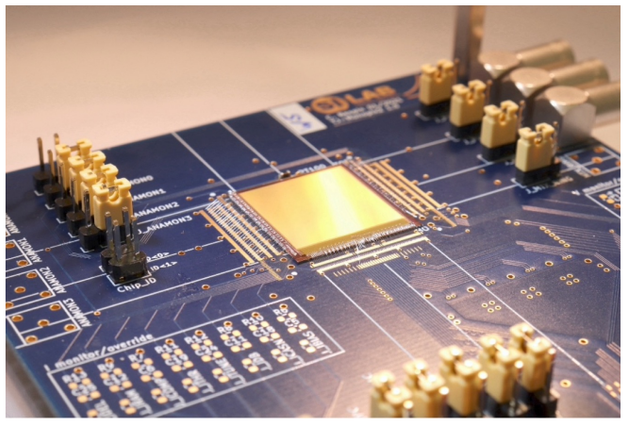
CERN

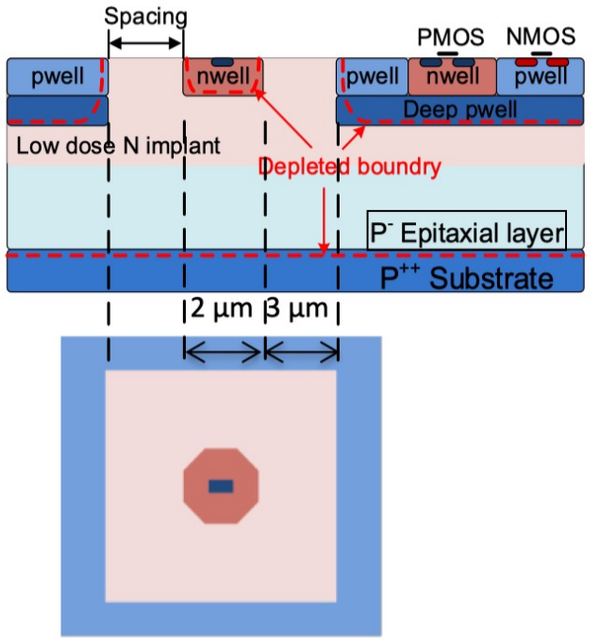
Derived from ALICE development (led by CERN)

## TJ-Monopix 1 (2018)



## TJ-Monopix 2 (2021)






- **Small electrode**
- Small capacitance ⇒ **low power and noise**
- High-resistivity epi layer: 1-8 kΩ cm
  (epi thickness: 18-40 $\mu$m)
- **Modified process** to improve **lateral depletion**