Fec test report:

Date: 2021-05-07 15:36:54

Tester name: Boris

Test#1 Monitoring values — Passed

0	FEC label	012	OK
1	FEC DC2438 ID	bf0000024ddcaa26	OK
2	FEC_T (to 35°C)	22.406	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.382	OK
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

Test#2 Slow control registers: — Passed

Test#3 Pedestal run: — Failed

Mean in range (245.0:255.0), 3.5 < rms < 8.0 (fpn 4.0)

8	After chip #8	Mean OK	STDDEV OK	OK
9	After chip #9	Mean OK	STDDEV OK	OK
10	After chip #10	Mean OK	STDDEV OK	OK
11	After chip #11	Mean OK	STDDEV OK	OK
12	After chip #12	Mean OK	STDDEV OK	OK
13	After chip #13	Mean OK	STDDEV OK	OK
14	After chip #14	Mean OK	STDDEV OK	OK
15	After chip #15	Mean FAILED	STDDEV OK	FAIL

Test#4 AD9637 test patterns — Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run — Passed

8	After chip #8	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3086	OK
9	After chip #9	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3049	OK
10	After chip #10	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3027	OK
11	After chip #11	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3101	OK
12	After chip #12	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3030	OK
13	After chip #13	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK
14	After chip #14	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3029	OK
15	After chip #15	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2899	OK

FEC test final result: Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_mask 0x1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x100000
1	fe fec_enable 2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x80000
2	fe 0 moni T 1	0	0 Tdcm(0) Fem(00) FEC_T: 22.406 degC
3	fe 0 moni V 1	0	0 Tdcm(0) Fem(00) FEC_Vdd: 3.290 V
4	fe 0 pulser 1 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
5	fe 0 pulser 1 base 0x3FFF	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
6	fe 0 pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
7	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
8	fe 0 moni I 1	0	0 Tdcm(0) Fem(00) FEC_I: 1.382 A
9	fe 0 moni S 1	0	0 Tdcm(0) Fem(00) FEC_Serial: bf0000024ddcaa26

Slow control registers test			
NO	Command	Error	Response
0	fe fec_mask 0x1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x100000
1	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
2	fe fec_enable 2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x80000
3	fe fec_enable	0	0 Tdcm(0) Fem(00) Reg(1) = 0x12188000 (303595520) FEC_Enable: 2
4	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
12	fe 0 after 8 wrchk 3 0x0 0x0909 0x0909	0	0 Tdcm(0) Fem(00) After(8) Reg(3) <- 0x0 0x909 0x909 (1 chip verified)
13	fe 0 after 9 wrchk 3 0x0 0x0a0a 0x0a0a	0	0 Tdcm(0) Fem(00) After(9) Reg(3) <- 0x0 0xa0a 0xa0a (1 chip verified)
14	fe 0 after 10 wrchk 3 0x0 0x0b0b 0x0b0b	0	0 Tdcm(0) Fem(00) After(10) Reg(3) <- 0x0 0xb0b 0xb0b (1 chip verified)
15	fe 0 after 11 wrchk 3 0x0 0x0c0c 0x0c0c	0	0 Tdcm(0) Fem(00) After(11) Reg(3) <- 0x0 0xc0c 0xc0c (1 chip verified)
16	fe 0 after 12 wrchk 3 0x0 0x0d0d 0x0d0d	0	0 Tdcm(0) Fem(00) After(12) Reg(3) <- 0x0 0xd0d 0xd0d (1 chip verified)
17	fe 0 after 13 wrchk 3 0x0 0x0e0e 0x0e0e	0	0 Tdcm(0) Fem(00) After(13) Reg(3) <- 0x0 0xe0e 0xe0e (1 chip verified)
18	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
19	fe 0 after 15 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(0) Fem(00) After(15) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
20	fe 0 after 8 read 3	0	0 Tdcm(0) Fem(00) After(8) Reg(3): 0x0 0x909 0x909
21	fe 0 after 9 read 3	0	0 Tdcm(0) Fem(00) After(9) Reg(3): 0x0 0xa0a 0xa0a
22	fe 0 after 10 read 3	0	0 Tdcm(0) Fem(00) After(10) Reg(3): 0x0 0xb0b 0xb0b
23	fe 0 after 11 read 3	0	0 Tdcm(0) Fem(00) After(11) Reg(3): 0x0 0xc0c 0xc0c
24	fe 0 after 12 read 3	0	0 Tdcm(0) Fem(00) After(12) Reg(3): 0x0 0xd0d 0xd0d
25	fe 0 after 13 read 3	0	0 Tdcm(0) Fem(00) After(13) Reg(3): 0x0 0xe0e 0xe0e
26	fe 0 after 14 read 3	0	0 Tdcm(0) Fem(00) After(14) Reg(3): 0x0 0x0 0x0
27	fe 0 after 15 read 3	0	0 Tdcm(0) Fem(00) After(15) Reg(3): 0x0 0x101 0x101
28	fe 0 after 8 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 9 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(9) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 10 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(10) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 11 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(11) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 12 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(12) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 13 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(13) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 14 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(14) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
35	fe 0 after 15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(15) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(0) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
12	fe adc 1 model AD9637	0	0 Tdcm(0) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 1 write 0x14 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 1 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 1 write 0x5 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 1 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 1 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 1 write 0x5 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)

19	fe adc 1 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 1 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
21	fe adc 1 write 0x5 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 1 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 1 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 1 write 0x5 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 1 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 1 write 0x4 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 1 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 1 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 1 write 0x4 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 1 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 1 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 1 write 0x4 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 1 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 1 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 1 write 0x4 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 1 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 1 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(0) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Curren
52	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 1 write 0x4 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 1 write 0x5 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 1 write 0xD 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
1	fe 0 after 8:15 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 8:15 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(0) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(0) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 1 enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 1 ft_enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 1 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 1 ampl 16383	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 1 delay 3000	0	0 Tdcm(0) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 1 enable 1	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(0) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(0) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(0) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(0) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(0) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done

35	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(0) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)
37	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfeff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfeff0000
40	fe 0 after 8 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(8) Reg(1) <- Test_mode=calibration
41	fe 0 after 8 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(8) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 8 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(8) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
69	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfdff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfdff0000
72	fe 0 after 9 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(9) Reg(1) <- Test_mode=calibration
73	fe 0 after 9 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(9) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 9 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(9) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
101	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfbff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfbff0000
104	fe 0 after 10 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(10) Reg(1) <- Test_mode=calibration
105	fe 0 after 10 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(10) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 10 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(10) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff

113	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
115	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
133	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xf7ff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xf7ff0000
136	fe 0 after 11 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(11) Reg(1) <- Test_mode=calibration
137	fe 0 after 11 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(11) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 11 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(11) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
165	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xefff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xefff0000
168	fe 0 after 12 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(12) Reg(1) <- Test_mode=calibration
169	fe 0 after 12 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(12) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 12 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(12) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
174	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
184	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)

191	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
193	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
197	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xdfff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xdfff0000
200	fe 0 after 13 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(13) Reg(1) <- Test_mode=calibration
201	fe 0 after 13 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(13) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 13 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(13) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
229	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xbfff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xbfff0000
232	fe 0 after 14 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(14) Reg(1) <- Test_mode=calibration
233	fe 0 after 14 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(14) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 14 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(14) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
261	fe 0 after 8:15 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 8:15 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(8:15) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0x7fff	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x7fff0000
264	fe 0 after 15 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(15) Reg(1) <- Test_mode=calibration
265	fe 0 after 15 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(15) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 15 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(15) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

269	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
271	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 1 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 1 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 1	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 1 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 8			CHIP 9			CHIP 10			CHIP 11			CHIP 12			CHIP 13			CHIP 14			CHIP 15		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	321.7	0.7	2 r	331.9	0.7	2 r	283.3	0.7	2 r	258.4	0.7	2 r	354.7	0.7	2 r	359.4	0.7	2 r	340.6	0.7	2 r	511.0	0.0
3	264.7	6.5	3	299.3	6.7	3	256.1	7.2	3	309.6	8.6	3	350.6	6.2	3	279.5	5.7	3	273.8	6.0	3	447.9	6.3
4	243.8	5.0	4	333.9	4.7	4	264.0	5.0	4	234.6	6.0	4	263.5	5.1	4	267.0	4.3	4	316.8	4.4	4	465.7	4.2
5	191.2	6.2	5	399.3	6.6	5	253.9	7.2	5	195.1	8.4	5	201.5	6.1	5	279.2	5.5	5	280.2	5.8	5	421.8	5.9
6	377.9	4.7	6	260.9	4.6	6	297.8	4.8	6	303.8	5.8	6	258.5	5.1	6	265.2	4.2	6	315.0	4.2	6	429.9	4.2
7	272.0	6.5	7	227.6	6.8	7	358.0	7.0	7	146.2	8.2	7	232.4	5.5	7	279.6	5.2	7	195.6	5.5	7	490.4	5.8
8	334.3	4.6	8	257.8	4.8	8	239.5	5.0	8	125.7	5.8	8	354.4	4.8	8	338.3	4.2	8	348.4	4.2	8	438.2	4.3
9	329.4	6.1	9	261.0	6.1	9	208.8	6.8	9	135.4	8.0	9	257.1	5.7	9	281.1	5.3	9	259.8	5.7	9	433.6	6.1
10	274.1	4.8	10	280.6	4.7	10	315.0	4.7	10	99.2	5.5	10	351.3	4.8	10	304.1	4.2	10	203.9	4.2	10	460.1	4.1
11	263.2	6.2	11	218.4	6.5	11	197.8	6.7	11	239.7	7.4	11	264.8	5.4	11	257.3	5.3	11	256.5	5.7	11	465.7	5.7
12	213.0	4.8	12	238.6	4.9	12	240.9	4.8	12	172.9	5.5	12	349.0	4.8	12	308.4	4.2	12	329.9	4.1	12	433.3	4.1
13	262.6	5.9	13	198.9	6.2	13	242.0	6.6	13	303.3	7.4	13	277.7	5.5	13	361.2	5.4	13	209.4	5.8	13	496.1	5.7
14	338.3	5.0	14	296.6	5.0	14	227.1	4.7	14	302.9	5.5	14	264.5	4.9	14	315.5	4.1	14	236.6	4.2	14	486.5	4.2
15 f	260.2	1.7	15 f	221.8	1.7	15 f	230.1	1.8	15 f	301.9	2.1	15 f	324.7	1.6	15 f	272.2	1.5	15 f	229.6	1.8	15 f	484.3	1.6
16	253.6	5.8	16	289.0	5.9	16	276.6	6.3	16	254.3	7.3	16	243.2	5.1	16	366.0	5.2	16	292.9	5.5	16	420.8	5.7
17	315.6	4.6	17	296.9	4.6	17	246.0	5.1	17	295.8	5.3	17	219.3	4.8	17	257.3	4.2	17	209.8	4.1	17	425.2	4.4
18	257.1	5.9	18	236.6	5.8	18	210.0	6.6	18	250.3	7.2	18	272.3	5.3	18	291.0	5.2	18	290.5	5.3	18	385.0	5.8
19	252.4	4.6	19	294.6	4.7	19	241.5	5.0	19	317.2	5.6	19	302.3	4.6	19	317.1	4.2	19	246.0	4.1	19	437.5	4.1
20	335.4	5.8	20	235.9	6.0	20	221.4	6.4	20	213.8	7.3	20	235.9	5.1	20	356.6	5.0	20	269.3	5.4	20	511.0	0.5
21	345.7	4.8	21	301.2	4.7	21	241.9	4.7	21	249.9	5.5	21	184.4	4.9	21	219.6	4.0	21	195.3	4.5	21	385.3	4.4
22	268.3	5.5	22	193.8	5.8	22	213.3	6.4	22	236.9	7.2	22	258.8	5.3	22	319.1	5.1	22	326.9	5.4	22	428.3	5.5
23	353.5	4.6	23	278.9	4.7	23	312.4	4.9	23	225.2	5.2	23	250.2	4.6	23	352.0	4.2	23	216.6	4.1	23	410.8	4.2
24	195.3	5.7	24	224.0	5.6	24	245.8	6.2	24	208.8	7.2	24	220.3	5.2	24	290.4	5.1	24	350.7	5.4	24	427.6	5.3
25	235.9	4.5	25	217.4	4.7	25	234.9	4.9	25	247.8	5.4	25	298.9	4.6	25	318.1	4.1	25	282.9	4.6	25	505.3	3.8
26	231.4	5.6	26	198.7	5.7	26	271.9	6.0	26	225.7	7.0	26	323.6	5.0	26	263.7	5.1	26	314.7	5.2	26	388.6	5.4
27	248.2	4.4	27	257.9	4.8	27	275.2	4.8	27	212.3	5.1	27	227.1	4.6	27	348.7	4.2	27	198.9	4.2	27	453.7	4.2
28 f	217.6	1.7	28 f	229.4	1.9	28 f	267.6	1.8	28 f	289.8	1.9	28 f	323.4	1.6	28 f	239.2	1.8	28 f	247.4	1.7	28 f	490.7	1.7
29	236.0	5.5	29	261.2	5.7	29	303.1	5.9	29	215.0	6.4	29	282.9	5.0	29	320.9	5.0	29	308.5	5.3	29	404.4	5.1
30	245.1	4.6	30	180.5	4.8	30	255.2	4.7	30	236.6	5.4	30	308.9	4.7	30	349.2	4.1	30	275.8	4.2	30	459.2	4.1
31	342.5	5.5	31	267.6	5.4	31	275.0	6.1	31	211.0	6.8	31	224.4	5.0	31	287.7	4.9	31	314.2	5.1	31	456.4	5.2
32	252.7	4.7	32	166.8	4.7	32	262.3	4.8	32	257.7	5.5	32	300.2	4.7	32	337.1	4.3	32	257.8	4.5	32	508.8	2.9
33	233.7	5.2	33	262.9	5.4	33	269.4	6.0	33	133.2	6.8	33	257.3	5.2	33	307.5	4.9	33	223.0	5.3	33	435.5	5.3
34	264.6	4.6	34	201.4	4.7	34	321.6	4.7	34	279.9	5.3	34	185.2	4.6	34	255.4	4.0	34	308.7	4.3	34	439.6	4.4
35	217.5	5.5	35	226.5	5.4	35	260.9	5.8	35	269.1	6.5	35	279.4	5.0	35	240.9	4.8	35	217.1	5.1	35	423.2	5.3
36	270.0	4.4	36	298.5	4.8	36	261.0	4.8	36	226.3	5.1	36	302.3	4.7	36	283.8	4.2	36	313.2	4.3	36	468.5	4.3
37	261.9	5.4	37	272.1	5.4	37	235.4	5.8	37	259.7	6.4	37	232.5	5.0	37	290.9	4.8	37	228.7	5.2	37	508.3	3.5
38	289.6	4.8	38	267.7	4.6	38	241.5	5.0	38	282.2	5.3	38	170.3	4.7	38	325.6	4.2	38	280.6	4.3	38	487.9	4.3
39	345.3	5.7	39	252.0	5.3	39	206.0	5.9	39	239.0	6.5	39	234.7	5.0	39	314.9	4.8	39	269.1	5.2	39	476.4	5.1
40	309.2	4.9	40	217.3	4.7	40	259.2	4.7	40	191.1	5.6	40	311.1	4.5	40	308.7	4.3	40	331.4	4.2	40	509.0	2.7
41	266.5	4.5	41	288.0	4.2	41	304.8	4.4	41	199.2	5.0	41	205.7	4.2	41	242.8	3.9	41	240.7	4.2	41	497.1	4.2
42	271.1	5.4	42	251.7	5.5	42	298.8	5.7	42	240.6	6.6	42	275.3	5.0	42	310.5	5.1	42	256.2	5.6	42	487.0	5.7
43	222.5	4.6	43	246.1	4.5	43	209.5	4.4	43	159.2	4.9	43	269.0	4.2	43	312.7	3.9	43	306.7	3.9	43	495.0	4.2
44	244.5	5.6	44	219.8	5.4	44	403.2	5.7	44	224.1	6.8	44	231.7	5.1	44	332.0	4.9	44	283.4	5.7	44	439.0	5.8
45	219.3	4.5	45	250.3	4.2	45	220.6	4.4	45	283.1	5.0	45	271.8	4.3	45	309.9	4.0	45	283.3	3.8	45	511.0	0.0
46	314.9	5.4	46	234.0	5.3	46	203.0	5.7	46	292.2	6.7	46	270.1	5.2	46	337.1	5.1	46	358.8	5.5	46	494.6	5.6
47	234.0	4.7	47	267.9	4.0	47	287.6	4.3	47	268.4	4.7	47	309.6	4.2	47	296.8	3.8	47	350.3	4.0	47	428.3	4.1
48	269.9	5.6	48	275.9	5.2	48	175.4	5.9	48	137.7	6.7	48	263.5	5.1	48	276.8	5.3	48	312.2	5.6	48	427.9	5.7
49	227.8	4.6	49	298.7	4.2	49	275.1	4.5	49	206.0	4.7	49	177.1	4.0	49	321.2	3.7	49	354.6	3.9	49	447.8	4.3
50	320.9	5.4	50	294.7	5.4	50	277.6	5.7	50	249.7	6.7	50	306.5	5.1	50	290.2	4.9	50	254.6	5.6	50	464.3	5.8
51	241.9	4.4	51	250.0	4.1	51	223.1	4.5	51	300.8	4.8	51	242.5	4.3	51	274.8	3.9	51	190.2	4.3	51	312.1	4.0
52	275.2	5.4	52	294.9	5.5	52	214.2	6.0	52	219.5	6.9	52	257.5	5.1	52	310.3	5.3	52	331.9	5.5	52	511.0	0.4
53 f	277.5	1.6	53 f	236.3	1.5	53 f	266.5	1.5	53 f	251.0	1.6	53 f	274.0	1.4	53 f	350.0	1.5	53 f	329.5	1.5	53 f	405.6	1.4
54	300.1	4.6	54	249.7	4.5	54	227.4	4.5	54	277.8	4.8	54	318.0	4.0	54	322.9	4.0	54	304.9	4.0	54	443.3	4.3
55	230.5	5.2	55	264.2	5.4	55	299.2	5.7	55	272.9	6.8	55	227.1	5.2	55	334.1	5.2	55	275.5	5.8	55	406.3	5.8
56	273.2	4.8	56	243.7	4.1	56	272.5	4.4	56	213.0	4.6	56	228.6	4.3	56	255.2	4.1	56	205.5	4.3	56	453.5	4.2
57	173.9	5.5	57	232.7	5.4	57	206.5	5.8	57	185.8	7.0	57	297.3	5.0	57	306.1	5.0	57	259.8	5.8	57	480.9	6.0
58	234.2	4.7	58	179.8	4.3	58	326.9	4.4	58	214.6	4.6	58	294.3	4.0	58	340.6	4.0	58	281.7	4.3	58	461.9	4.1
59	262.1	5.5	59	291.6	5.9	59	296.3	6.0	59	220.7	6.9	59	233.1	5.2	59	296.6	5.0	59	310.5	5.8	59	510.9	0.7
60	238.4	4.6	60	254.4	4.5	60	288.7	4.3	60	234.6	4.6	60	261.0	4.1	60	263.2	3.8	60	240.1	4.0	60	475.8	4.0
61	288.2	5.6	61	225.3	5.8	61	313.9	5.8	61	162.2	6.9	61	234.1	5.3	61	334.1	5.3	61	263.0	5.8	61	428.1	6.0
62	285.0	4.8	62	344.0	4.2	62	209.8	4.3	62	287.1	5.0	62	260.4	4.0	62	278.5	4.0	62	295.2	4.2	62	441.7	4.1
63	207.0	5.4	63	227.7	5.7	63	320.0	6.0	63	248.1	7.0	63	274.0	5.2	63	307.4	5.3	63	331.7	5.9	63	444.9	6.2
64	370.5	4.8	64	251.7	4.2	64	267.2	4.3	64	291.4	5.0	64	251.7	4.0	64	292.0	4.1	64	267.1	4.0	64	462.9	4.3
65	186.7	5.6	65	245.1	5.7	65	313.7	6.0	65	306.0	7.1	65	328.6	5.5	65	262.4	5.2	65	324.9	5.8	65	510.9	0.9
66 f	265.8	1.5	66 f	228.9	1.6	66 f	269.6	1.5	66 f	227.3	1.6	66 f	237.7	1.5	66 f	313.4	1.5	66 f	243.6	1.4	66 f	444.8	1.4
67	237.9	4.7	67	218.1	4.0	67	270.4	4.4	67	293.4	4.6	67	268.9	4.0	67	234.5	3.9	67	236.2	4.2	67	407.7	4.2
68	261.6	5.9	68	280.1	5.8	68	264.1	5.8	68	238.8	7.1	68	253.4	5.2	68	330.4	5.3	68	233.2	5.7	68	452.6	6.3
69	204.3	4.8	69	278.8	4.2	69	264.7	4.5	69	167.4	4.8	69	251.0	4.1	69	381.3	4.0	69	256.5	4.3	69	412.1	4.2
70	238.7	5.7	70	215.4	5.7	70	315.6	6.1	70	174.6	6.9	70	310.5	5.7	70	243.3	5.3	70	258.3	6.0	70	420.3	6.2
71	215.6	4.7	71	297.7	4.4	71	302.7	4.5	71	313.0	4.9	71	227.4	4.0	71	207.9	3.9	71	251.6	4.0	71	489.7	4.2
72	286.7	5.8	72	214.1	5.6	72	276.8	6.3	72	346.1	7.1	72	283.1	5.4	72	319.0	5.5	72	346.1	6.1	72	457.9	6.2
73	226.0	4.9	73	269.1	4.0	73	277.9	4.5	73	298.4	4.9	73	291.9	4.2	73	230.4	4.0	73	234.7	4.0	73	451.4	4.4
74	222.5	5.8	74	353.7	5.8	74	317.5	6.4	74	190.6	7.0	74	284.5	5.7	74	334.1	5.7	74	229.8	6.0	74	421.2	6.4
75	234.2	4.9	75	175.2	4.1	75	339.4	4.4	75	250.8	4.9	75	263.5	4.2	75	335.7	4.0	75	253.8	4.1	75	422.4	4.2
76	283.2	5.8	76	260.9	6.0	76	275.4	6.4	76	304.8	7.0	76	234.7	5.8	76	385.2	5.6	76	255.7	6.4	76	441.9	6.5
77	262.1	4.9	77	331.9	4.2	77	249.3	4.6	77	267.0	4.8	77	294.3	4.1	77	297.1	4.2	77	337.8	4.1	77	442.5	4.6
78	263.4	5.9	78	272.4	5.9	78	312.6	6.5	78	249.8	7.2	78	360.5	5.7	78	366.3	5.9	78	214.9	6.3	78	476.7	6.7

Pedestal after centermean.

CHIP 8		
CH	M	STD
0 r	250.0	0.0
1 r	495.0	6.7
2 r	249.5	0.7
3	248.4	5.6
4	250.4	4.4
5	251.6	5.1
6	251.3	4.3
7	250.8	5.3
8	250.2	4.4
9	250.1	5.3
10	251.1	4.3
11	248.8	5.4
12	250.8	4.7
13	250.4	5.1
14	249.4	4.3
15 f	251.1	1.7
16	249.9	4.9
17	250.3	4.3
18	251.4	5.0
19	251.0	4.5
20	249.5	4.8
21	249.7	4.3
22	251.6	4.7
23	249.7	4.5
24	251.3	5.1
25	249.4	4.2
26	251.2	4.8
27	249.8	4.1
28 f	249.0	1.7
29	250.8	4.6
30	251.0	4.2
31	251.1	4.7
32	250.1	4.3
33	250.1	4.9
34	249.5	4.2
35	249.6	4.8
36	251.1	4.3
37	250.2	4.6
38	248.9	4.4
39	251.5	4.9
40	249.8	4.2
41	251.1	4.4
42	250.9	4.5
43	250.2	4.1
44	250.4	4.6
45	250.5	4.2
46	250.3	4.8
47	249.4	4.2
48	249.8	4.6
49	250.4	4.3
50	250.4	4.6
51	250.7	4.2
52	249.7	4.6
53 f	249.8	1.6
54	250.2	4.1
55	250.2	4.8
56	249.8	4.1
57	250.2	4.6
58	250.8	4.2
59	250.1	4.6
60	250.8	4.2
61	250.6	5.0
62	249.9	4.3
63	249.9	4.6
64	248.8	4.5
65	250.0	4.7
66 f	249.9	1.6
67	250.3	4.4
68	250.0	4.9
69	250.1	4.4
70	250.2	5.0
71	249.7	4.1
72	250.5	5.0
73	250.1	4.6
74	251.3	5.0
75	251.7	4.5
76	249.4	4.9
77	250.2	4.7
78	250.1	4.9

CHIP 9		
CH	M	STD
0 r	250.0	0.0
1 r	394.5	9.9
2 r	250.1	0.7
3	250.7	5.5
4	250.4	4.6
5	250.0	5.6
6	250.3	4.4
7	249.4	5.5
8	251.0	4.4
9	250.3	5.4
10	249.8	4.3
11	250.0	5.2
12	250.1	4.4
13	251.5	5.3
14	250.4	4.3
15 f	250.6	1.6
16	250.4	4.9
17	250.9	4.5
18	248.9	5.0
19	250.5	4.6
20	250.7	4.8
21	250.9	4.4
22	250.6	5.2
23	249.4	4.6
24	249.3	4.8
25	251.6	4.4
26	249.2	4.9
27	249.7	4.3
28 f	250.5	2.0
29	250.5	4.8
30	249.8	4.5
31	249.5	4.9
32	250.9	4.3
33	249.8	4.8
34	252.3	4.3
35	250.5	4.7
36	251.2	4.5
37	250.3	4.8
38	249.8	4.3
39	249.8	4.9
40	251.9	4.5
41	250.2	3.9
42	250.0	4.6
43	249.7	4.3
44	251.9	4.5
45	250.2	4.0
46	249.0	4.5
47	250.2	3.9
48	250.8	4.8
49	250.1	4.2
50	250.6	4.7
51	251.5	4.0
52	251.6	4.7
53 f	250.0	1.5
54	249.9	4.0
55	251.3	4.5
56	249.4	4.0
57	250.1	4.8
58	249.8	4.3
59	250.0	4.5
60	250.3	4.0
61	250.3	5.0
62	249.1	4.1
63	249.7	4.8
64	250.1	4.0
65	251.0	4.7
66 f	250.5	1.5
67	250.7	4.2
68	250.9	4.8
69	248.9	4.3
70	250.3	4.8
71	250.0	4.0
72	249.7	4.9
73	249.8	4.1
74	249.0	4.9
75	250.3	4.0
76	252.2	4.9
77	250.1	4.2
78	250.8	4.9

CHIP 10		
CH	M	STD
0 r	250.0	0.0
1 r	334.3	10.6
2 r	250.4	0.7
3	250.8	5.7
4	251.3	4.5
5	250.6	6.0
6	250.1	4.5
7	251.1	5.7
8	250.3	4.2
9	251.0	5.6
10	250.1	4.7
11	250.6	5.4
12	250.4	4.5
13	249.8	5.5
14	250.4	4.5
15 f	250.9	1.7
16	250.5	5.0
17	249.4	4.6
18	250.9	5.1
19	250.6	4.3
20	251.1	5.2
21	249.9	4.4
22	250.5	5.2
23	251.0	4.4
24	250.8	5.3
25	250.8	4.5
26	250.8	4.9
27	251.0	4.4
28 f	249.8	1.8
29	250.0	5.2
30	250.9	4.3
31	249.9	4.9
32	249.4	4.4
33	249.8	4.9
34	250.7	4.1
35	249.4	5.1
36	249.7	4.4
37	251.6	5.1
38	250.8	4.4
39	249.4	5.1
40	249.6	4.4
41	249.9	4.1
42	249.4	4.6
43	249.6	4.3
44	251.6	4.9
45	251.1	4.1
46	251.1	5.0
47	249.7	4.2
48	250.5	4.9
49	250.2	4.2
50	249.6	4.7
51	250.4	4.1
52	250.2	4.8
53 f	250.8	1.5
54	250.8	4.2
55	250.9	4.9
56	250.6	4.4
57	249.9	5.0
58	250.0	4.2
59	252.6	4.9
60	250.6	4.1
61	251.0	4.9
62	249.1	4.2
63	249.7	5.0
64	249.9	4.1
65	251.0	5.1
66 f	249.5	1.6
67	251.9	4.1
68	250.8	5.0
69	250.1	4.3
70	250.8	5.1
71	249.6	4.4
72	250.3	5.1
73	250.2	4.2
74	248.6	5.4
75	251.2	4.1
76	250.9	5.1
77	251.2	4.3
78	250.3	5.2

CHIP 11		
CH	M	STD
0 r	250.0	0.0
1 r	380.9	11.0
2 r	250.7	0.6
3	250.5	6.6
4	251.1	4.8
5	251.1	6.3
6	249.4	4.9
7	250.5	6.5
8	251.6	5.3
9	250.9	6.1
10	250.1	5.0
11	251.7	6.0
12	249.2	4.8
13	251.8	6.1
14	250.7	4.9
15 f	250.1	1.8
16	251.1	5.7
17	249.6	5.0
18	253.0	5.7
19	249.9	4.7
20	249.6	5.7
21	250.4	4.9
22	250.5	5.7
23	252.1	5.1
24	250.3	5.8
25	250.3	4.7
26	250.8	5.6
27	252.0	4.7
28 f	250.4	1.7
29	250.9	5.6
30	250.1	4.7
31	250.8	5.7
32	252.3	4.5
33	251.9	5.3
34	251.3	4.9
35	249.4	5.4
36	251.7	4.7
37	250.4	5.5
38	250.5	5.0
39	250.2	5.3
40	250.4	4.8
41	251.3	4.5
42	250.2	5.5
43	250.2	4.4
44	249.8	5.4
45	249.8	4.5
46	251.0	5.2
47	251.3	4.5
48	250.1	5.5
49	250.5	4.3
50	250.0	5.4
51	250.8	4.2
52	250.9	5.4
53 f	250.0	1.8
54	250.0	4.4
55	250.8	5.4
56	252.0	4.4
57	249.8	5.6
58	250.9	4.7
59	250.0	5.6
60	250.9	4.6
61	252.2	5.4
62	250.3	4.3
63	250.7	5.5
64	250.7	4.3
65	249.7	5.5
66 f	250.7	1.5
67	250.0	4.5
68	249.8	5.3
69	252.4	4.5
70	249.9	5.4
71	249.8	4.5
72	248.9	5.8
73	249.3	4.5
74	250.3	5.5
75	250.4	4.6
76	251.4	5.6
77	251.1	4.5
78	251.5	5.8

CHIP 12		
CH	M	STD
0 r	250.0	0.0
1 r	495.3	8.8
2 r	249.8	0.7
3	250.1	5.1
4	251.0	4.6
5	250.4	5.0
6	251.1	4.5
7	251.3	5.0
8	251.2	4.4
9	251.3	4.8
10	250.7	4.4
11	248.9	4.6
12	249.1	4.4
13	250.1	4.7
14	250.5	4.4
15 f	250.0	1.6
16	251.3	4.8
17	251.6	4.3
18	251.1	4.7
19	251.6	4.5
20	250.9	4.6
21	250.5	4.4
22	249.6	4.7
23	251.0	4.4
24	250.7	4.7
25	251.3	4.3
26	251.5	4.6
27	250.5	4.2
28 f	250.6	1.6
29	249.8	4.6
30	251.6	4.6
31	251.3	4.5
32	251.2	4.4
33	252.9	4.6
34	251.4	4.4
35	250.2	4.3
36	251.1	4.3
37	249.9	4.6
38	248.8	4.2
39	250.7	4.7
40	249.9	4.2
41	251.3	3.8
42	248.5	4.5
43	250.4	3.9
44	250.0	4.3
45	251.2	4.0
46	251.4	4.5
47	249.8	3.9
48	250.3	4.6
49	250.3	3.9
50	250.1	4.5
51	250.7	4.2
52	248.0	4.5
53 f	250.0	1.5
54	249.4	3.8
55	250.1	4.4
56	251.2	3.8
57	250.8	4.6
58	250.6	3.9
59	250.3	4.6
60	251.1	3.9
61	250.0	4.4
62	250.6	4.0
63	249.5	4.7
64	250.9	4.1
65	249.4	4.8
66 f	249.7	1.4
67	249.8	4.1
68	249.6	4.8
69	251.2	4.0
70	249.4	4.6
71	252.2	3.7
72	249.0	4.9
73	250.6	4.0
74	251.3	4.7
75	249.6	4.2
76	250.4	4.8
77	251.1	4.1
78	250.0	4.8

CHIP 13		
CH	M	STD
0 r	250.0	0.0
1 r	367.2	9.4
2 r	250.5	0.7
3	249.6	5.2
4	250.1	4.3
5	249.9	4.9
6	250.2	4.3
7	250.2	4.7
8	249.6	4.3
9	251.1	4.8
10	251.8	4.2
11	252.2	4.9
12	251.3	4.0
13	249.5	4.5
14	248.9	4.2
15 f	250.0	1.6
16	249.4	4.5
17	250.5	4.0
18	250.3	4.6
19	251.3	4.1
20	249.1	4.7
21	250.3	4.0
22	249.3	4.5
23	249.5	3.9
24	250.8	4.5
25	251.2	4.2
26	249.2	4.5
27	247.7	4.0
28 f	250.3	1.6
29	251.3	4.2
30	250.7	4.2
31	250.7	4.5
32	251.1	4.2
33	249.6	4.5
34	252.6	4.1
35	250.1	4.3
36	251.1	4.0
37	250.8	4.3
38	249.5	3.8
39	249.9	4.2
40	249.9	4.0
41	249.7	3.7
42	250.8	4.5
43	248.6	3.8
44	249.7	4.6
45	250.1	3.8
46	253.0	4.4
47	250.3	3.9
48	249.9	4.5
49	250.7	3.9
50	250.2	4.4
51	250.1	3.8
52	250.8	4.4
53 f	250.2	1.4
54	250.2	3.8
55	251.9	4.5
56	250.5	3.8
57	251.2	4.4
58	249.7	3.8
59	249.6	4.6
60	250.5	3.9
61	251.1	4.6
62	249.8	3.9
63	250.8	4.5
64	250.6	3.8
65	251.7	4.6
66 f	250.6	1.4
67	251.2	4.0
68	251.7	4.5
69	251.4	3.9
70	251.9	4.7
71	250.8	3.8
72	251.0	4.6
73	249.9	3.8
74	250.4	4.6
75	249.0	4.0
76	249.1	4.8
77	250.4	3.9
78	250.4	4.9

CHIP 14		
CH	M	STD
0 r	250.0	0.0
1 r	345.7	9.6
2 r	249.4	0.7
3	250.2	5.2
4	251.4	4.1
5	250.2	5.0
6	249.4	4.3
7	249.8	4.8
8	249.6	4.1
9	249.7	5.0
10	250.2	4.2
11	249.4	4.9
12	250.7	4.1
13	249.6	4.9
14	250.7	4.3
15 f	249.5	1.8
16	250.9	4.6
17	248.8	4.0
18	249.3	4.5
19	250.9	3.8
20	249.9	4.9
21	250.6	4.1
22	249.9	4.6
23	250.8	4.1
24	249.2	4.7
25	249.7	4.1
26	249.4	4.7
27	250.1	4.4
28 f	251.0	1.8
29	250.8	4.6
30	250.5	4.0
31	250.2	4.4
32	250.1	4.0
33	249.0	4.6
34	250.2	4.2
35	249.7	4.5
36	250.1	4.3
37	249.5	4.5
38	248.5	4.3
39	249.8	4.4
40	250.7	4.2
41	247.8	3.9
42	249.6	4.6
43	249.8	3.8
44	251.4	4.7
45	250.5	3.9
46	248.3	4.7
47	251.9	4.0
48	250.0	4.6
49	249.7	4.0
50	250.2	4.8
51	249.3	3.9
52	250.3	4.8
53 f	251.1	1.5
54	250.5	4.1
55	249.1	4.9
56	251.0	4.0
57	250.4	4.8
58	248.8	3.9
59	248.5	4.9
60	249.6	3.8
61	250.1	4.9
62	249.9	4.0
63	249.3	4.8
64	249.7	3.7
65	250.5	5.1
66 f	249.2	1.4
67	249.3	3.9
68	250.3	5.2
69	250.0	4.1
70	250.8	5.0
71	248.9	3.9
72	251.1	5.0
73	248.8	3.8
74	250.5	5.2
75	249.9	3.9
76	249.5	5.0
77	249.0	4.0
78	249.9	5.4

CHIP 15		
CH	M	STD
0 r	250.0	0.0
1 r	473.7	10.1
2 r	279.2	0.7
3	250.0	5.2
4	249.2	4.0
5	251.8	5.0
6	249.8	3.9
7	250.6	4.9
8	250.4	4.0
9	249.2	4.9
10	249.8	4.0
11	249.3	4.9
12	250.2	4.1
13	249.1	4.9
14	250.3	4.0
15 f	250.2	1.6
16	249.6	4.7
17	249.9	3.9
18	250.8	4.6
19	251.4	3.9
20	268.0	4.6
21	249.7	3.9
22	250.0	4.6
23	249.1	3.9
24	250.1	4.6
25	250.2	3.9
26	249.5	4.5
27	249.3	4.2
28 f	250.0	1.7
29	250.1	4.7
30	249.5	3.9
31	250.6	4.8
32	254.7	4.2
33	250.2	4.6
34	250.3	4.0
35	250.0	4.5
36	249.0	4.2
37	253.1	4.5
38	249.9	3.9
39	250.9	4.6
40	254.8	4.0
41	251.3	3.8
42	247.7	4.7
43	250.0	3.7
44	251.1	4.7
45	279.7	3.9
46	250.7	4.9
47	252.0	3.7
48	248.9	4.7
49	247.6	4.0
50	250.7	4.9
51	250.0	3.7
52	278.8	5.0
53 f	249.3	1.4
54	250.7	3.8
55	249.8	4.6
56	250.3	3.8
57	249.1	4.9
58	248.5	3.9
59	271.5	5.0
60	248.3	4.0
61	249.7	4.9
62	249.9	3.8
63	250.6	4.9
64	249.8	4.0
65	270.9	4.9
66 f	249.8	1.4
67	248.9	3.9
68	250.5	4.9
69	250.5	3.8
70	250.8	5.1
71	249.7	4.0
72	251.1	5.0
73	250.8	3.9
74	250.6	5.0
75	250.1	3.9
76	249.5	5.4
77	249.8	3.9
78	250.0	5.5