Fec test report:

Date: 2021-07-20 10:24:33

Tester name: Boris

Test#1 Monitoring values — Passed

0	FEC label	010	OK
1	FEC DC2438 ID	5d0000024d9c7026	OK
2	FEC_T (to 35°C)	22.281	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.489	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers: Passed

Test#3 Pedestal run: Passed

Mean in range (245.0:255.0), 3.5 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns — Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run — Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3028	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3102	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3143	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3119	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3073	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3045	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3117	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3034	OK

FEC test final result: Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
2	fe 0 moni T 0	0	0 Tdcm(0) Fem(00) FEC_T: 22.281 degC
3	fe 0 moni V 0	0	0 Tdcm(0) Fem(00) FEC_Vdd: 3.290 V
4	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
5	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
6	fe 0 pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
7	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
8	fe 0 moni I 0	0	0 Tdcm(0) Fem(00) FEC_I: 1.489 A
9	fe 0 moni S 0	0	0 Tdcm(0) Fem(00) FEC_Serial: 5d0000024d9c7026

Slow control registers test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
2	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
3	fe fec_enable	0	0 Tdcm(0) Fem(00) Reg(1) = 0x2248000 (35946496) FEC_Enable: 1
4	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
12	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
13	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
14	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
15	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
16	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
17	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
18	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
19	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
20	fe 0 after 0 read 3	0	0 Tdcm(0) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
21	fe 0 after 1 read 3	0	0 Tdcm(0) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
22	fe 0 after 2 read 3	0	0 Tdcm(0) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
23	fe 0 after 3 read 3	0	0 Tdcm(0) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
24	fe 0 after 4 read 3	0	0 Tdcm(0) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
25	fe 0 after 5 read 3	0	0 Tdcm(0) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
26	fe 0 after 6 read 3	0	0 Tdcm(0) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
27	fe 0 after 7 read 3	0	0 Tdcm(0) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
28	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
35	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(0) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(0) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)

19	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
21	fe adc 0 write 0x5 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(0) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Curren
52	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(0) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(0) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(0) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(0) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(0) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(0) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(0) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(0) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done

35	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(0) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)
37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff

113	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xfff7	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)

191	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
193	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

269	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
271	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.4	1 r	508.5	5.2	1 r	511.0	0.0	1 r	474.8	12.2	1 r	511.0	0.0	1 r	511.0	0.0
2 r	320.3	0.7	2 r	282.5	0.7	2 r	272.0	0.7	2 r	266.8	0.7	2 r	302.1	0.7	2 r	307.2	0.7	2 r	265.0	0.6	2 r	333.5	0.7
3	303.8	6.2	3	203.9	6.4	3	258.1	7.4	3	230.8	9.3	3	263.9	7.9	3	207.2	7.1	3	250.7	7.2	3	335.6	7.8
4	196.0	4.4	4	282.6	4.8	4	204.8	5.0	4	306.9	5.7	4	311.5	6.2	4	272.4	5.3	4	171.9	5.2	4	272.4	5.5
5	244.6	6.2	5	210.7	6.9	5	223.7	7.3	5	240.8	9.2	5	334.4	7.1	5	280.6	6.6	5	268.2	6.7	5	263.3	7.4
6	122.5	4.6	6	241.3	4.5	6	272.6	4.7	6	196.9	5.8	6	327.6	6.5	6	287.3	5.2	6	162.1	5.2	6	181.7	5.4
7	218.2	6.0	7	188.0	6.5	7	258.2	7.3	7	210.3	8.7	7	213.8	7.0	7	264.4	6.2	7	224.0	6.7	7	307.6	7.4
8	157.5	4.6	8	151.3	4.6	8	147.4	4.9	8	199.0	5.8	8	311.2	6.3	8	264.5	5.3	8	249.1	5.1	8	233.3	5.2
9	128.0	6.0	9	207.5	6.1	9	239.6	7.2	9	283.4	8.3	9	265.4	7.1	9	200.1	6.2	9	179.1	6.8	9	281.5	6.9
10	179.5	4.3	10	278.1	4.5	10	194.4	4.5	10	288.8	5.5	10	306.2	6.4	10	249.6	5.2	10	205.7	5.2	10	312.2	5.4
11	207.6	5.8	11	174.7	6.1	11	201.8	6.7	11	182.4	7.8	11	274.7	6.5	11	171.4	6.4	11	214.4	6.8	11	231.8	7.2
12	257.2	4.8	12	202.4	4.7	12	268.3	4.5	12	197.5	5.6	12	346.5	6.6	12	242.7	4.9	12	188.6	5.3	12	258.7	5.3
13	175.7	5.9	13	189.7	6.0	13	167.5	6.6	13	222.5	7.6	13	210.4	7.0	13	218.2	6.3	13	101.1	6.7	13	259.3	7.0
14	136.5	4.6	14	118.4	4.4	14	184.4	4.8	14	186.9	5.4	14	251.5	6.1	14	289.9	5.2	14	226.6	5.2	14	250.0	5.5
15 f	256.2	1.6	15 f	112.9	1.7	15 f	126.6	1.8	15 f	127.4	1.7	15 f	248.9	1.6	15 f	170.8	1.7	15 f	166.2	1.8	15 f	278.4	1.6
16	180.7	5.7	16	211.3	6.0	16	192.2	6.4	16	204.4	7.9	16	261.0	6.7	16	155.9	5.9	16	209.0	6.7	16	284.0	6.9
17	213.0	4.5	17	232.3	4.6	17	244.4	4.7	17	197.5	5.6	17	201.4	6.1	17	361.7	5.1	17	220.2	5.3	17	300.6	5.6
18	163.9	5.8	18	210.9	6.0	18	195.6	6.6	18	296.8	7.8	18	279.9	6.5	18	339.3	5.9	18	230.9	6.6	18	260.6	6.7
19	160.2	4.3	19	152.4	4.7	19	266.0	4.7	19	213.3	5.7	19	236.6	6.3	19	238.9	5.3	19	257.4	4.9	19	279.4	5.4
20	214.6	5.7	20	278.3	5.9	20	162.1	6.4	20	234.6	7.6	20	257.2	6.2	20	90.6	6.2	20	198.8	6.4	20	200.1	6.9
21	254.6	4.4	21	203.4	4.6	21	248.3	4.8	21	103.1	5.2	21	288.9	6.1	21	282.0	5.3	21	231.6	5.4	21	202.9	5.4
22	247.5	5.5	22	194.2	5.6	22	232.3	6.4	22	201.3	7.7	22	241.6	6.2	22	245.9	5.9	22	161.4	6.3	22	265.3	6.8
23	246.3	4.6	23	218.1	4.7	23	295.3	4.5	23	198.9	5.3	23	228.7	6.7	23	262.6	5.2	23	186.7	5.0	23	283.6	5.5
24	199.7	5.4	24	177.8	6.0	24	213.0	6.0	24	234.0	7.3	24	268.1	6.4	24	260.3	6.0	24	244.8	6.2	24	168.8	6.8
25	122.5	4.5	25	157.0	4.5	25	262.9	4.7	25	154.1	5.5	25	259.1	6.1	25	294.6	5.1	25	186.9	5.2	25	285.6	5.1
26	268.9	5.3	26	205.9	5.8	26	237.9	6.0	26	226.8	7.5	26	322.0	6.2	26	251.3	5.8	26	199.2	6.1	26	187.0	6.8
27	224.1	4.3	27	241.8	4.7	27	215.8	4.6	27	297.1	5.2	27	219.5	6.1	27	202.6	5.3	27	183.3	5.4	27	232.1	5.3
28 f	274.8	1.6	28 f	246.3	1.9	28 f	145.5	1.8	28 f	207.1	1.7	28 f	283.0	1.8	28 f	142.3	1.8	28 f	196.8	1.9	28 f	209.1	1.7
29	203.8	5.1	29	119.3	5.5	29	235.4	6.1	29	227.8	7.1	29	263.6	6.2	29	280.9	5.9	29	227.4	6.3	29	325.6	6.5
30	176.3	4.5	30	310.1	4.3	30	242.3	4.5	30	235.0	5.2	30	208.9	6.3	30	222.4	5.2	30	250.1	5.2	30	265.3	5.5
31	184.5	5.5	31	177.6	5.7	31	133.5	6.0	31	223.8	7.1	31	235.0	6.2	31	261.6	5.8	31	270.7	6.2	31	213.6	6.8
32	171.3	4.5	32	187.4	4.7	32	279.0	4.5	32	203.8	5.4	32	243.8	6.1	32	166.6	5.2	32	135.5	5.2	32	239.7	5.4
33	197.8	5.2	33	151.8	5.4	33	315.6	5.8	33	222.3	6.8	33	234.8	6.6	33	248.7	6.0	33	195.9	6.0	33	261.6	6.4
34	247.6	4.4	34	225.1	4.5	34	211.1	4.4	34	207.9	5.4	34	238.5	6.1	34	265.4	5.2	34	228.3	5.5	34	169.8	5.5
35	252.0	5.2	35	128.5	5.3	35	226.6	5.8	35	229.4	6.7	35	249.8	6.1	35	354.9	5.7	35	161.6	6.3	35	238.0	6.4
36	229.3	4.2	36	229.8	4.5	36	207.0	4.7	36	293.5	5.1	36	300.7	6.1	36	214.6	5.3	36	214.9	5.1	36	246.7	5.5
37	260.0	5.2	37	113.9	5.4	37	143.9	5.7	37	158.6	6.7	37	298.1	6.2	37	250.3	5.7	37	151.8	6.0	37	320.6	6.3
38	202.2	4.6	38	116.7	4.6	38	161.3	4.3	38	244.9	5.3	38	282.3	6.2	38	296.2	5.2	38	314.3	5.3	38	263.5	5.5
39	280.6	5.3	39	234.3	5.1	39	209.3	5.6	39	210.4	6.7	39	207.5	7.0	39	171.1	6.1	39	175.4	6.3	39	160.0	6.9
40	227.0	4.8	40	200.5	4.7	40	169.3	4.6	40	211.7	5.2	40	239.0	6.4	40	240.7	5.8	40	322.6	5.4	40	214.3	6.0
41	221.2	4.8	41	252.9	4.1	41	148.7	4.3	41	162.0	5.2	41	222.0	5.5	41	293.2	4.8	41	165.3	5.1	41	274.7	5.2
42	238.7	5.1	42	134.4	5.3	42	171.8	6.0	42	231.3	6.9	42	275.1	6.3	42	232.3	5.9	42	171.9	6.3	42	231.0	7.1
43	209.2	4.6	43	240.7	4.4	43	263.8	4.5	43	181.8	4.9	43	162.1	5.0	43	315.0	4.8	43	181.6	4.9	43	255.0	5.1
44	199.8	5.6	44	192.2	5.3	44	251.6	6.0	44	253.2	7.0	44	259.9	6.3	44	203.7	6.2	44	240.2	6.6	44	242.2	7.0
45	259.8	4.7	45	241.9	4.4	45	198.4	4.4	45	287.1	5.1	45	242.2	5.1	45	255.0	4.9	45	206.7	4.9	45	244.5	5.0
46	226.3	5.4	46	142.7	5.2	46	228.4	6.0	46	195.7	7.2	46	219.0	6.3	46	170.8	6.1	46	234.2	6.6	46	241.7	7.0
47	202.8	4.7	47	206.0	4.2	47	170.9	4.7	47	213.0	4.8	47	245.0	5.0	47	353.6	4.7	47	210.7	4.7	47	306.8	5.3
48	228.0	5.5	48	158.9	5.4	48	199.2	6.1	48	172.8	7.3	48	202.9	6.0	48	186.4	5.9	48	208.8	6.5	48	243.0	7.2
49	199.2	4.6	49	189.1	4.2	49	236.3	4.3	49	191.0	4.8	49	276.9	5.1	49	195.1	4.7	49	216.4	4.9	49	265.8	5.1
50	255.2	5.5	50	190.2	5.5	50	239.7	6.0	50	216.4	7.1	50	295.8	6.0	50	247.2	6.1	50	147.4	6.5	50	352.9	7.3
51	234.1	4.3	51	245.7	4.3	51	160.2	4.5	51	267.7	4.8	51	151.9	5.1	51	195.0	4.7	51	210.9	4.8	51	324.0	4.9
52	249.1	5.3	52	149.0	5.4	52	243.4	6.0	52	254.1	7.3	52	290.5	6.2	52	255.2	6.0	52	150.3	6.8	52	306.3	7.2
53 f	217.3	1.6	53 f	182.6	1.7	53 f	235.2	1.6	53 f	199.1	1.6	53 f	289.5	1.5	53 f	212.3	1.6	53 f	207.0	1.5	53 f	256.9	1.4
54	252.4	4.6	54	163.7	4.2	54	204.0	4.4	54	212.6	4.9	54	290.9	5.0	54	319.3	4.7	54	232.1	5.0	54	224.7	5.1
55	120.2	5.5	55	281.9	5.6	55	235.7	6.1	55	172.7	7.0	55	291.1	6.0	55	251.1	6.2	55	184.7	6.6	55	307.8	7.1
56	239.9	4.5	56	189.3	4.2	56	177.1	4.2	56	319.9	4.7	56	249.3	5.0	56	234.6	4.7	56	219.2	4.8	56	297.7	5.2
57	295.2	5.4	57	170.1	5.7	57	202.6	5.9	57	220.4	7.0	57	182.9	5.8	57	244.4	6.0	57	94.1	6.4	57	222.5	7.2
58	210.9	4.6	58	218.4	4.4	58	190.2	4.3	58	298.7	4.7	58	296.6	5.0	58	342.9	4.6	58	190.7	4.7	58	199.6	5.2
59	174.4	5.4	59	224.5	5.7	59	300.9	6.0	59	225.2	7.1	59	269.2	6.0	59	291.5	6.2	59	231.7	6.5	59	337.3	7.3
60	159.2	4.5	60	185.6	4.3	60	184.8	4.6	60	292.6	4.9	60	299.4	4.9	60	279.6	4.5	60	205.3	4.6	60	303.0	5.1
61	197.5	5.4	61	221.3	5.6	61	288.5	6.2	61	148.4	7.4	61	210.2	6.0	61	234.0	6.0	61	245.0	6.7	61	304.0	7.3
62	173.5	4.8	62	257.7	4.2	62	234.9	4.5	62	255.6	4.9	62	291.9	4.8	62	221.4	4.8	62	192.2	4.5	62	197.3	5.1
63	198.0	5.6	63	219.2	5.9	63	205.3	6.1	63	225.4	7.3	63	262.9	6.4	63	270.1	6.3	63	236.4	7.0	63	283.6	7.5
64	270.2	4.8	64	205.6	4.3	64	213.3	4.4	64	230.2	4.8	64	319.1	5.1	64	208.9	4.6	64	195.1	4.8	64	247.5	5.3
65	174.9	5.8	65	221.3	5.8	65	267.3	6.2	65	253.8	7.2	65	258.3	6.3	65	241.2	6.2	65	254.0	6.7	65	254.4	7.5
66 f	230.4	1.5	66 f	196.9	1.5	66 f	222.2	1.6	66 f	329.4	1.6	66 f	367.6	1.7	66 f	244.0	1.6	66 f	169.7	1.4	66 f	307.1	1.4
67	153.9	4.8	67	227.8	4.4	67	297.2	4.2	67	155.9	4.6	67	289.4	4.9	67	231.1	4.6	67	226.6	4.6	67	242.3	5.1
68	278.9	5.5	68	202.0	5.7	68	183.8	6.5	68	195.2	7.3	68	331.3	6.2	68	179.8	6.2	68	164.7	6.8	68	316.2	7.6
69	184.7	4.8	69	239.3	4.3	69	229.5	4.6	69	203.7	4.8	69	294.9	4.8	69	274.8	4.6	69	230.4	4.8	69	158.7	5.2
70	294.9	5.8	70	168.9	5.8	70	192.1	6.3	70	238.1	7.2	70	223.1	6.3	70	219.7	6.4	70	170.7	7.1	70	226.2	7.5
71	274.6	4.8	71	266.2	4.3	71	204.7	4.6	71	134.7	5.0	71	323.1	5.3	71	281.9	4.7	71	174.9	4.8	71	193.9	5.4
72	254.5	5.9	72	267.5	6.0	72	224.8	6.3	72	228.6	7.4	72	334.8	6.3	72	247.3	6.5	72	121.9	6.8	72	226.8	7.7
73	205.4	4.8	73	222.9	4.6	73	224.4	4.6	73	205.5	4.8	73	358.4	4.9	73	329.9	4.9	73	91.5	4.9	73	236.8	5.4
74	171.8	5.9	74	197.6	5.9	74	277.2	6.6	74	174.5	7.5	74	288.8	6.5	74	203.0	6.5	74	192.0	6.9	74	243.8	7.9
75	221.6	4.8	75	212.8	4.4	75	183.9	4.5	75	218.2	4.8	75	239.4	5.0	75	276.1	4.7	75	162.6	5.0	75	294.5	5.3
76	296.0	6.1	76	140.2	5.8	76	334.2	6.8	76	310.2	7.5	76	338.9	6.8	76	259.9	6.5	76	147.9	7.1	76	247.7	8.2
77	217.1	5.0	77	150.3	4.7	77	301.3	4.5	77	190.0	5.0	77	274.2	4.9	77	235.4	4.7	77	203.1	4.9	77	251.7	5.4
78	297.5	6.1	78	247.5	6.0	78	313.1	6.7	78	271.8	7.7	78	305.0	6.8	78	210.8	6.8	78	243.8	7.2	78	290.2	8.1

Pedestal after centermean.

CHIP 0		
CH	M	STD
0 r	250.0	0.0
1 r	386.8	11.0
2 r	249.9	0.7
3	249.4	5.3
4	249.9	4.4
5	249.0	5.4
6	248.5	4.4
7	250.6	5.1
8	250.3	4.4
9	247.9	5.2
10	249.9	4.6
11	248.6	5.1
12	249.3	4.7
13	248.9	5.2
14	249.9	4.4
15 f	249.9	1.6
16	249.3	5.0
17	250.7	4.2
18	249.8	5.0
19	249.5	4.3
20	250.5	4.9
21	249.0	4.6
22	249.8	5.0
23	250.9	4.5
24	248.9	5.1
25	249.2	4.6
26	249.9	4.8
27	249.3	4.3
28 f	249.6	1.6
29	249.5	4.9
30	249.1	4.2
31	250.5	4.7
32	249.7	4.3
33	249.7	4.9
34	249.5	4.2
35	248.2	4.6
36	249.6	4.3
37	249.7	5.1
38	250.4	4.3
39	249.2	4.5
40	250.2	4.3
41	250.0	4.3
42	249.5	5.1
43	248.6	4.1
44	250.9	4.7
45	250.9	4.4
46	249.3	4.7
47	249.7	4.3
48	249.2	4.7
49	251.0	4.3
50	249.9	4.7
51	251.9	4.3
52	250.7	4.6
53 f	249.4	1.6
54	249.4	4.2
55	250.4	4.8
56	250.1	4.4
57	250.8	4.7
58	249.7	4.5
59	250.3	4.7
60	250.2	4.3
61	248.7	4.9
62	251.2	4.4
63	249.7	5.0
64	250.4	4.4
65	250.7	5.1
66 f	250.3	1.6
67	250.9	4.5
68	249.6	4.8
69	249.2	4.3
70	251.0	5.0
71	248.2	4.6
72	248.6	4.8
73	250.8	4.5
74	249.3	5.2
75	249.7	4.4
76	249.4	5.2
77	249.4	4.6
78	250.8	5.1

CHIP 1		
CH	M	STD
0 r	250.0	0.0
1 r	315.6	8.5
2 r	250.6	0.7
3	250.4	5.7
4	249.7	4.7
5	248.4	5.5
6	251.6	4.2
7	250.1	5.6
8	250.6	4.5
9	250.1	5.5
10	250.7	4.5
11	249.4	5.3
12	250.9	4.4
13	249.8	5.3
14	250.7	4.3
15 f	249.5	1.6
16	250.6	5.3
17	251.3	4.3
18	248.3	5.1
19	251.3	4.6
20	251.6	5.4
21	249.4	4.5
22	249.6	5.0
23	251.5	4.4
24	248.9	5.0
25	250.0	4.2
26	250.7	4.9
27	249.9	4.4
28 f	250.2	1.8
29	249.9	5.0
30	250.2	4.5
31	250.1	4.8
32	249.5	4.5
33	251.0	4.9
34	249.7	4.2
35	251.8	4.7
36	249.6	4.5
37	250.2	4.7
38	250.3	4.1
39	249.9	4.6
40	250.0	4.2
41	249.5	4.1
42	250.0	4.9
43	249.5	4.3
44	251.1	5.0
45	251.2	4.2
46	249.1	4.8
47	250.7	4.0
48	250.6	4.8
49	251.1	4.0
50	252.5	4.8
51	250.6	4.2
52	248.8	4.7
53 f	249.6	1.5
54	249.9	4.3
55	249.8	5.0
56	249.7	4.1
57	250.7	4.8
58	251.2	4.1
59	250.8	4.8
60	249.3	4.5
61	249.1	4.8
62	250.2	4.2
63	250.8	5.1
64	250.5	4.1
65	249.4	5.0
66 f	250.1	1.6
67	250.6	4.2
68	251.0	5.1
69	250.6	4.1
70	249.4	5.3
71	250.3	4.1
72	250.3	5.1
73	249.5	4.1
74	249.7	5.3
75	251.2	4.3
76	250.2	4.8
77	250.0	4.2
78	249.1	5.4

CHIP 2		
CH	M	STD
0 r	250.0	0.0
1 r	285.7	11.3
2 r	249.9	0.7
3	249.7	6.5
4	248.7	4.7
5	249.4	6.1
6	248.9	4.4
7	249.9	6.4
8	251.2	4.4
9	250.5	5.7
10	251.1	4.4
11	249.5	5.7
12	250.2	4.5
13	249.3	5.6
14	252.5	4.4
15 f	249.8	1.8
16	249.6	5.8
17	250.9	4.6
18	248.7	5.8
19	251.6	4.4
20	250.8	5.6
21	250.1	4.6
22	251.0	5.5
23	249.1	4.5
24	248.9	5.5
25	250.7	4.4
26	249.3	5.3
27	248.5	4.3
28 f	249.9	1.7
29	249.4	5.2
30	249.3	4.0
31	248.7	5.3
32	250.1	4.3
33	248.8	5.3
34	250.1	4.5
35	248.3	5.1
36	250.2	4.5
37	249.3	5.2
38	250.1	4.3
39	250.6	4.9
40	250.8	4.3
41	251.5	4.4
42	249.2	5.1
43	250.7	4.4
44	249.5	5.2
45	250.9	4.3
46	250.8	5.3
47	248.1	4.3
48	249.7	5.2
49	250.1	4.3
50	249.1	5.3
51	250.2	4.3
52	250.0	5.3
53 f	250.8	1.6
54	250.3	4.4
55	248.7	5.2
56	249.9	4.3
57	250.5	5.1
58	250.6	4.3
59	249.7	5.2
60	250.6	4.3
61	250.9	5.1
62	250.5	4.1
63	250.9	5.2
64	251.7	4.1
65	250.8	5.4
66 f	249.9	1.6
67	249.4	4.1
68	249.2	5.5
69	250.0	4.4
70	251.2	5.3
71	250.3	4.4
72	250.1	5.5
73	248.9	4.5
74	249.3	5.5
75	248.7	4.4
76	249.3	5.7
77	249.3	4.2
78	250.5	5.5

CHIP 3		
CH	M	STD
0 r	250.0	0.0
1 r	260.8	12.0
2 r	249.6	0.7
3	249.3	7.2
4	249.7	5.0
5	249.9	7.5
6	250.5	5.2
7	252.8	7.2
8	249.8	5.2
9	249.7	7.0
10	249.3	5.0
11	251.2	6.5
12	248.3	5.0
13	251.0	6.5
14	250.8	4.8
15 f	250.0	1.8
16	250.2	6.3
17	250.2	4.8
18	249.6	6.7
19	249.5	5.1
20	250.1	6.2
21	251.5	5.3
22	250.3	6.4
23	250.4	4.7
24	249.4	6.3
25	249.8	4.9
26	249.6	6.1
27	251.2	4.9
28 f	250.1	1.6
29	249.3	6.0
30	248.5	4.5
31	250.8	6.0
32	249.7	4.8
33	249.3	5.8
34	248.8	4.7
35	250.9	6.0
36	248.9	4.6
37	251.6	5.8
38	249.6	4.8
39	250.4	5.5
40	250.3	4.7
41	250.7	4.8
42	249.8	5.7
43	250.4	4.5
44	250.8	6.0
45	249.8	4.5
46	249.3	5.8
47	250.8	4.3
48	250.6	5.8
49	249.0	4.6
50	250.1	5.8
51	250.3	4.5
52	249.7	5.8
53 f	249.9	1.6
54	250.1	4.5
55	248.1	5.7
56	249.4	4.5
57	249.8	6.1
58	249.2	4.4
59	249.2	6.0
60	248.8	4.3
61	249.8	6.0
62	249.5	4.4
63	252.0	6.3
64	250.5	4.5
65	249.3	5.8
66 f	250.4	1.6
67	249.1	4.4
68	249.3	6.1
69	251.3	4.4
70	250.0	6.0
71	250.3	4.5
72	250.1	6.2
73	249.9	4.4
74	248.1	6.3
75	250.9	4.3
76	250.6	6.4
77	250.8	4.5
78	249.8	6.3

CHIP 4		
CH	M	STD
0 r	250.0	0.0
1 r	316.2	11.8
2 r	250.1	0.7
3	250.1	6.3
4	250.0	5.6
5	249.4	6.2
6	249.8	5.3
7	250.0	6.1
8	250.9	5.5
9	250.3	6.0
10	250.9	5.5
11	250.2	5.7
12	250.0	5.6
13	250.4	5.8
14	248.9	5.2
15 f	250.0	1.6
16	249.9	5.6
17	250.7	5.4
18	250.1	5.7
19	250.8	5.2
20	249.7	5.5
21	249.8	5.2
22	249.8	5.5
23	249.2	5.3
24	249.9	5.5
25	249.5	5.2
26	251.0	5.3
27	250.5	5.2
28 f	250.3	1.7
29	249.4	5.2
30	250.0	5.3
31	249.2	5.6
32	250.6	5.5
33	250.0	5.3
34	249.8	5.5
35	250.8	5.5
36	249.2	5.3
37	249.5	5.5
38	250.7	5.5
39	250.6	5.8
40	249.9	5.4
41	250.8	4.8
42	250.2	5.4
43	249.2	4.7
44	250.5	5.0
45	250.3	4.7
46	249.3	5.0
47	249.9	4.3
48	250.6	5.2
49	249.8	4.7
50	249.6	4.9
51	249.5	5.1
52	249.5	5.1
53 f	249.3	1.6
54	251.2	4.5
55	249.7	5.1
56	250.9	4.5
57	250.8	5.3
58	249.8	4.7
59	250.7	5.0
60	250.1	4.7
61	250.8	5.4
62	249.5	4.3
63	250.2	5.2
64	249.0	4.6
65	249.4	5.1
66 f	249.8	1.7
67	250.3	4.6
68	250.7	5.3
69	250.7	4.3
70	250.9	5.5
71	249.0	4.6
72	250.1	5.6
73	250.1	4.6
74	250.5	5.4
75	249.8	4.6
76	249.8	5.7
77	251.3	4.7
78	250.7	5.6

CHIP 5		
CH	M	STD
0 r	250.0	0.0
1 r	249.2	11.9
2 r	250.1	0.7
3	249.0	6.0
4	249.9	4.7
5	249.6	5.5
6	250.2	5.0
7	250.7	5.4
8	249.9	4.9
9	250.8	5.3
10	249.7	4.7
11	250.2	5.2
12	250.4	4.7
13	250.2	5.6
14	249.8	4.7
15 f	250.1	1.7
16	249.7	5.1
17	249.2	4.6
18	252.4	5.1
19	250.8	4.7
20	249.7	5.2
21	248.8	4.7
22	249.3	5.1
23	249.7	5.0
24	250.1	5.1
25	249.2	4.8
26	250.5	5.0
27	250.2	4.7
28 f	250.1	1.8
29	251.2	5.3
30	250.8	4.7
31	250.2	5.2
32	249.8	4.7
33	250.2	5.0
34	251.0	4.7
35	250.6	5.1
36	249.4	5.0
37	250.3	5.2
38	251.5	5.0
39	250.6	5.2
40	250.7	5.0
41	249.5	4.1
42	250.5	5.2
43	251.0	4.3
44	250.2	5.1
45	249.7	4.4
46	249.2	4.9
47	248.0	4.3
48	251.6	4.9
49	250.6	4.4
50	250.2	5.1
51	250.8	4.4
52	250.2	5.0
53 f	249.8	1.6
54	250.4	4.4
55	249.2	5.1
56	248.4	4.4
57	250.6	5.2
58	250.2	4.3
59	250.6	5.3
60	250.0	4.4
61	249.1	5.2
62	250.0	4.2
63	249.5	5.2
64	250.0	4.6
65	251.3	5.5
66 f	249.6	1.5
67	250.2	4.3
68	249.5	5.3
69	250.5	4.6
70	249.3	5.6
71	250.2	4.3
72	249.9	5.2
73	250.0	4.3
74	249.2	5.3
75	249.2	4.5
76	250.2	5.3
77	250.8	4.6
78	250.3	5.5

CHIP 6		
CH	M	STD
0 r	250.0	0.0
1 r	303.8	9.4
2 r	250.0	0.6
3	249.0	6.0
4	249.9	4.9
5	251.0	5.8
6	250.2	4.9
7	250.7	5.6
8	250.2	4.8
9	250.5	6.0
10	250.0	5.0
11	249.7	5.6
12	249.9	4.6
13	249.3	5.6
14	250.6	4.6
15 f	250.1	1.7
16	248.6	5.3
17	250.1	4.6
18	250.2	5.5
19	251.6	4.8
20	250.6	5.8
21	249.4	4.8
22	250.4	5.2
23	251.1	4.5
24	249.2	5.5
25	250.0	4.7
26	250.1	5.3
27	251.2	4.9
28 f	249.8	1.8
29	250.6	5.4
30	250.1	4.8
31	250.3	5.4
32	250.6	4.9
33	249.0	5.4
34	250.8	4.6
35	249.7	5.4
36	248.9	4.6
37	249.7	5.2
38	249.7	4.9
39	249.3	5.6
40	251.2	4.9
41	249.6	4.5
42	250.8	5.5
43	249.0	4.7
44	250.6	5.3
45	252.3	4.7
46	249.6	5.4
47	249.2	4.4
48	250.5	5.3
49	249.7	4.3
50	251.8	5.6
51	250.0	4.4
52	250.3	5.5
53 f	250.2	1.5
54	250.6	4.4
55	249.1	5.4
56	249.9	4.4
57	250.6	5.5
58	249.9	4.4
59	249.5	5.4
60	250.8	4.5
61	250.1	5.6
62	249.9	4.3
63	248.8	5.8
64	250.7	4.2
65	250.5	5.5
66 f	249.6	1.4
67	251.2	4.5
68	249.9	5.7
69	248.6	4.4
70	251.3	6.0
71	250.2	4.6
72	249.3	5.6
73	249.7	4.7
74	250.6	5.8
75	249.9	4.6
76	250.1	5.9
77	249.5	4.5
78	249.7	6.3

CHIP 7		
CH	M	STD
0 r	250.0	0.0
1 r	468.1	7.6
2 r	250.0	0.7
3	249.9	6.5
4	250.2	5.0
5	251.2	6.2
6	250.0	4.8
7	249.6	6.5
8	250.1	4.8
9	250.5	6.1
10	249.1	5.1
11	249.9	5.8
12	249.1	4.7
13	249.5	5.8
14	249.8	4.9
15 f	249.7	1.6
16	250.1	5.8
17	247.8	4.8
18	249.4	5.8
19	250.5	4.9
20	250.1	5.7
21	248.9	4.7
22	250.7	5.7
23	250.5	4.9
24	250.7	5.8
25	249.0	4.7
26	250.8	5.5
27	248.0	4.9
28 f	249.4	1.7
29	249.8	5.6
30	248.8	4.7
31	248.2	5.6
32	248.7	4.9
33	249.0	5.4
34	249.4	4.9
35	249.9	5.5
36	249.4	4.9
37	249.2	5.4
38	249.3	5.2
39	250.1	5.5
40	249.9	5.0
41	251.0	4.5
42	248.6	6.0
43	250.8	4.6
44	250.4	5.9
45	249.7	4.7
46	250.3	5.9
47	250.4	4.6
48	251.4	5.7
49	249.1	4.6
50	249.2	5.7
51	249.8	4.4
52	251.0	5.9
53 f	249.7	1.5
54	249.5	4.6
55	250.1	5.9
56	249.8	4.4
57	249.9	6.0
58	248.6	4.4
59	250.2	6.1
60	249.4	4.4
61	251.0	6.1
62	250.5	4.6
63	249.6	6.1
64	251.3	4.7
65	250.7	6.0
66 f	250.0	1.4
67	251.2	4.8
68	248.9	6.2
69	249.3	4.6
70	249.4	6.4
71	249.6	4.8
72	249.8	6.3
73	249.7	4.7
74	250.5	6.6
75	248.6	4.7
76	249.0	6.2
77	250.4	5.1
78	248.2	6.6