Thank you for the reports and I understand the basic idea but what I'd like to know is the final design of the proposal with components (modules) and their specifications, including further details of the hardware and software of each component.
I'll send the questions about the technical details but let me send my questions about the overall design of your proposal. I think the grand design is essential information when we review for the technical decision.

Q1) I'd like to see the block diagram like Figure 1.

There is a block diagrams in the proposal (Fig.3) but I'd like to see not the conceptual but the actual implementation as the "system".

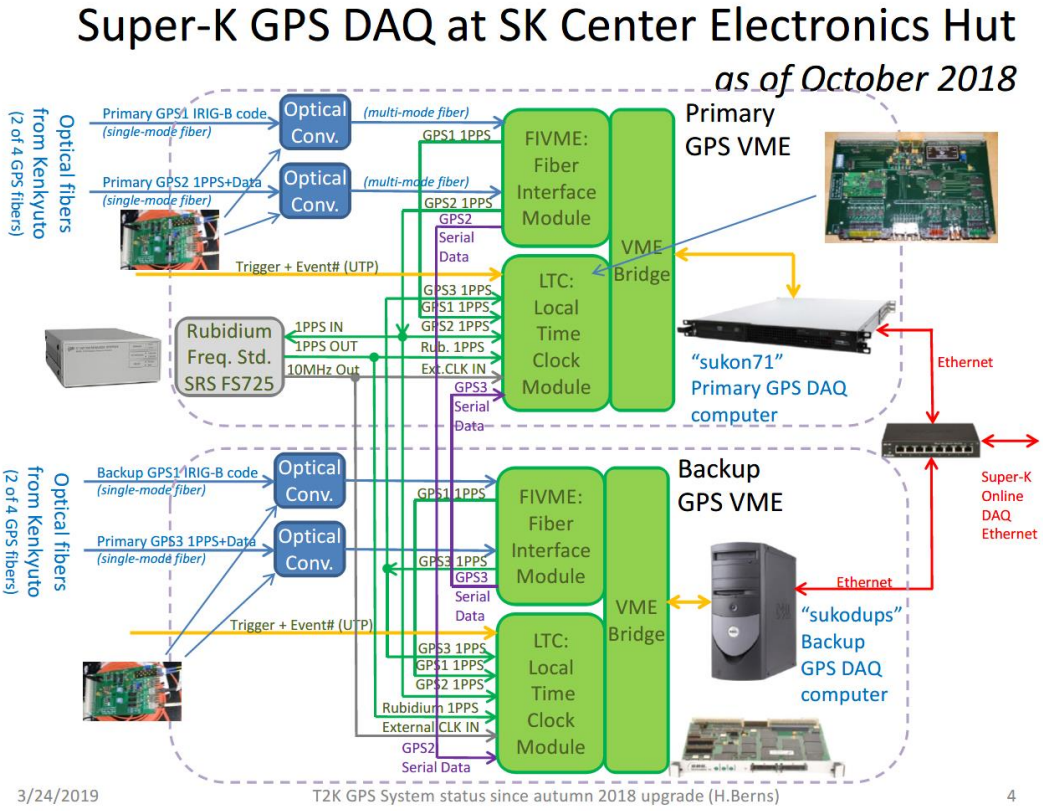

Figure 1 Block diagram of the SK GPS system

Q2) What is the plan to associate the timestamp (UTC) with the data (timing)? Also, what is the plan to record the timestamp information?

I'd like to know your plan to associate the timestamp (UTC) with the data blocks (the timing information of the digitizer) and the method to recording the timestamp in the data stream.

The following is our initial idea based on our SK experience. At this moment, we don't send the UTC time stamp to each front-end board but record the timestamp at 60kHz, every time TDC is reset and one of the counters, so-called 32bit hardware (HW) counter, is incremented. (In Figure 1, this counter is expressed as "Event #", which is not the actual "event" number but the counter incremented every TDC reset @60kHz.)

1) There are two UTC timestamps with 1pps signals from two main GPS receivers.
2) The value of the 32bit counter of LTC is recorded when the GPS 1pps pulse comes in. Here, each 32bit counter of LTC (Local time clock) is incremented at 60MHz. The source clock of the LTC counter is Rb atomic clock, which is compensated by GPS 1pps. (There are 2 GPS receivers and thus, there are two numbers.)
3) The value of the 32bit counter of LTC when TDC reset pulses come in. The TDC reset pulse is generated every 1024 cycles of the reference 60MHz clock. (1 tick of TDC is 1/1920MHz ~ 0.52ns, and 1024 cycles of 60MHz clock corresponds to 32768 TDC counts.)
4) GPS readout computer records the latest LTC counts of two GPS 1pps and the TDC reset timing together with the 32bit HW counter, whenever the TDC reset is issued.

Based on our experience, I think it is sufficient to send a 32-bit counter, which counts up every 16384 ns (2048 cycles of 125 MHz clock), to each front-end boards for the `global' synchronization just as we did in SK together with the external input signals. The possible diagram is shown in

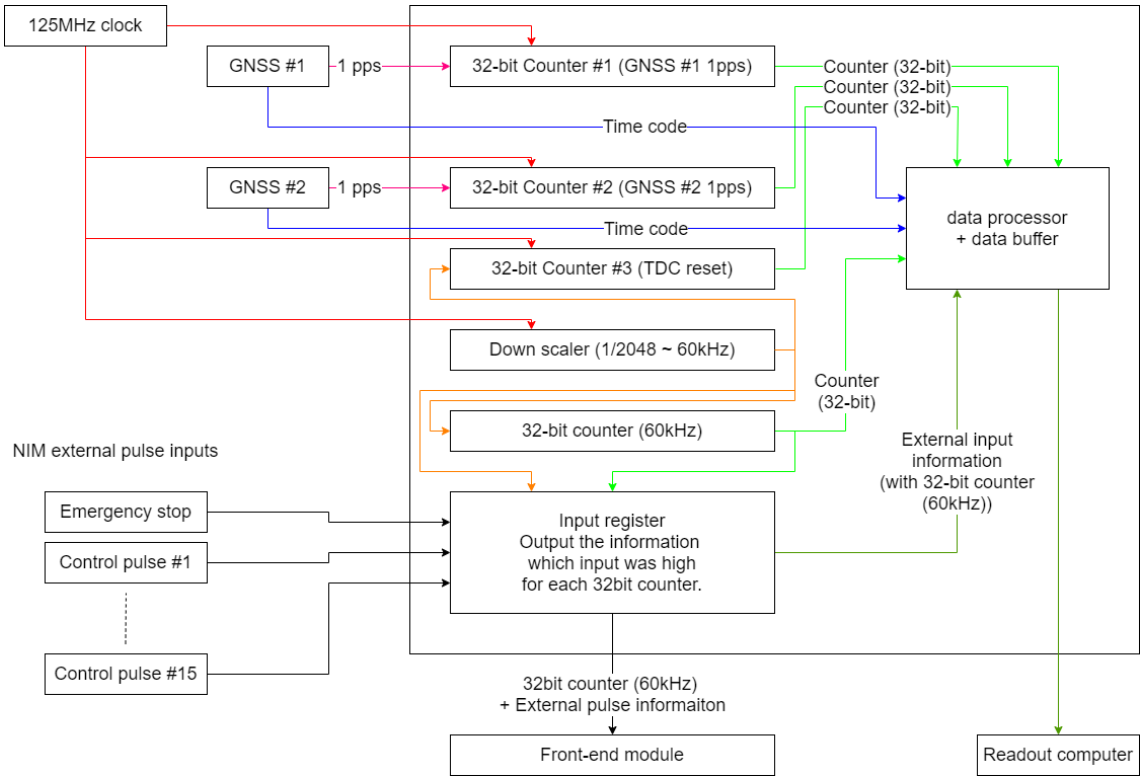

Figure 2. In this case, the information sent to the front-end board via optical transmission are

1) 32-bit counter (60kHz) of TDC reset. This counter incremented every 16384 ns (= 8 x 2048 ~60kHz).
2) External input pulse information, i.e., bit pattern of external input.

The data sent to the readout computer are

1) 32-bit counter (60kHz) of TDC reset. This counter incremented every 16384 ns (= 8 x 2048 ~60kHz).
2) 32-bit counter value when the TDC reset occurs. This counter is incremented at 125MHz.
3) 32-bit counter value when the last 1pps pulse from GNSS #1 comes. This counter is incremented at 125MHz.
4) 32-bit counter value when the last 1pps pulse from GNSS #2 comes. This counter is incremented at 125MHz.

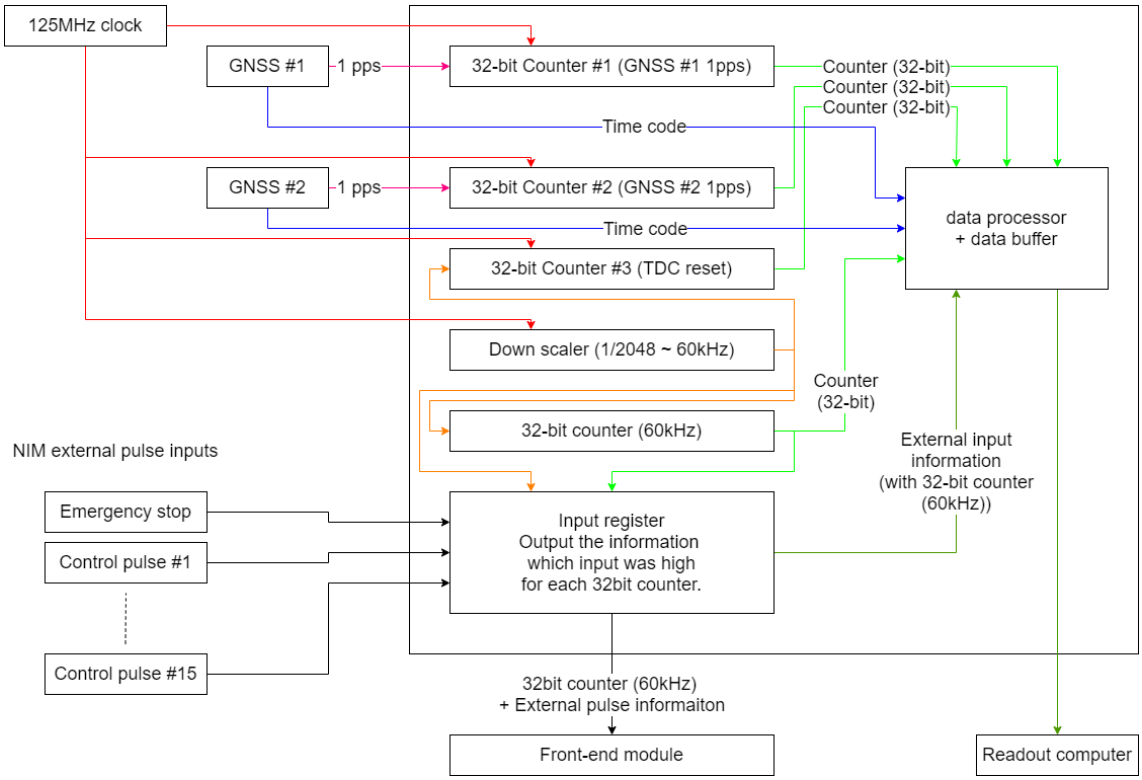

Figure 2 Possible diagram for HK

Q3) What is the plan to implement the external inputs in case of WR case?

Q4) What is the plan to send bac the information from the front-end electronics in case of WR?

Q5) How many distributors you are going to use for WR and custom solutions?