

## Fec test report:

Date: 2021-04-28 09:12:55

Tester name: LC

### Test#1 Monitoring values

Passed

0	FEC label	060	OK
1	FEC DC2438 ID	c80000024db61e26	OK
2	FEC_T (to 35°C)	22.469	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.514	OK
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

### Test#2 Slow control registers:

Passed

### Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

### Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

### Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3079	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3070	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3085	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3056	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3127	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3047	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3081	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3014	OK

## FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 22.469 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.757 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: c80000024db61e26

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG )
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 ( Aligned SCA_Write )
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS )
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE )
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 ( Aligned Dev_Ready )
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c ( CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 TdcM(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
142	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 TdcM(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.930 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 ( WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

## Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.1	1 r	511.0	0.0	1 r	511.0	0.0	1 r	451.1	12.1	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	286.4	0.7	2 r	260.3	0.7	2 r	359.3	0.7	2 r	295.2	0.7	2 r	266.7	0.7	2 r	285.0	0.7	2 r	296.9	0.7	2 r	303.8	0.6
3	202.1	4.9	3	293.7	4.9	3	250.1	5.0	3	211.1	6.2	3	174.8	5.8	3	258.9	5.4	3	262.2	5.7	3	298.4	6.1
4	240.7	4.6	4	255.9	4.5	4	304.4	4.1	4	174.2	5.4	4	133.8	6.0	4	205.9	4.8	4	266.6	5.1	4	302.8	5.4
5	235.2	4.9	5	197.5	5.0	5	252.5	4.7	5	247.5	6.0	5	178.1	5.8	5	219.8	5.2	5	279.6	5.3	5	180.2	5.6
6	187.0	4.5	6	153.5	4.3	6	326.9	4.6	6	150.1	5.1	6	155.3	5.8	6	182.2	4.9	6	175.8	5.0	6	211.0	5.6
7	331.5	4.8	7	184.4	5.0	7	308.0	4.7	7	275.7	6.1	7	94.9	5.7	7	313.4	4.8	7	301.2	4.9	7	154.9	5.6
8	178.3	4.4	8	190.9	4.5	8	368.6	4.1	8	239.8	5.2	8	171.5	5.9	8	183.2	5.0	8	249.3	4.9	8	224.8	5.4
9	235.3	4.7	9	189.0	4.9	9	351.0	4.5	9	216.0	5.7	9	182.1	5.4	9	223.8	5.0	9	194.6	5.3	9	261.4	5.4
10	310.7	4.3	10	242.3	4.6	10	415.7	4.0	10	219.2	5.1	10	238.9	5.5	10	284.4	4.8	10	248.8	5.0	10	198.7	5.5
11	229.8	4.3	11	179.1	4.8	11	347.4	4.5	11	211.4	5.5	11	151.2	5.3	11	344.6	4.8	11	240.1	5.1	11	255.0	5.5
12	255.7	4.3	12	170.6	4.3	12	354.0	4.2	12	265.8	5.0	12	206.4	6.0	12	291.8	4.9	12	295.2	5.0	12	262.3	5.5
13	227.6	4.7	13	182.8	4.9	13	339.5	4.5	13	289.7	5.4	13	232.3	5.4	13	297.4	5.1	13	265.9	4.7	13	212.9	5.3
14	217.0	4.5	14	234.0	4.6	14	398.1	4.3	14	246.6	5.0	14	171.2	5.4	14	222.9	4.7	14	210.1	4.9	14	269.4	5.4
15 f	148.2	1.7	15 f	181.5	2.0	15 f	334.2	1.7	15 f	245.6	1.7	15 f	127.4	1.6	15 f	201.4	1.7	15 f	210.3	1.7	15 f	249.1	1.8
16	177.7	4.7	16	148.7	4.7	16	233.3	4.5	16	118.0	5.5	16	210.8	5.2	16	282.2	4.9	16	239.3	4.8	16	279.4	5.3
17	156.3	4.5	17	202.9	4.4	17	404.9	4.3	17	199.2	4.9	17	193.3	5.3	17	244.2	4.9	17	308.1	4.9	17	251.3	5.0
18	209.5	4.6	18	163.8	4.6	18	324.3	4.5	18	203.8	5.4	18	190.3	5.1	18	267.1	4.8	18	250.2	4.7	18	234.1	5.3
19	304.3	4.3	19	146.2	4.4	19	304.9	4.4	19	221.0	4.8	19	137.1	5.6	19	250.3	4.8	19	196.0	4.7	19	264.9	5.3
20	296.2	5.0	20	279.1	4.8	20	339.3	4.5	20	266.6	5.3	20	115.0	5.3	20	237.7	4.8	20	207.2	4.8	20	254.5	5.2
21	216.1	4.3	21	136.3	4.7	21	280.8	4.0	21	218.9	5.0	21	180.3	5.3	21	163.3	4.6	21	230.2	5.2	21	212.9	5.4
22	222.3	4.7	22	191.3	4.7	22	315.8	4.3	22	217.7	5.3	22	113.2	5.2	22	209.4	4.9	22	206.5	5.3	22	261.7	5.1
23	242.9	4.4	23	142.1	4.2	23	243.3	4.1	23	200.3	4.7	23	150.8	5.5	23	225.2	4.7	23	259.6	4.8	23	297.6	5.4
24	178.1	4.6	24	180.7	4.5	24	311.3	4.4	24	272.9	5.5	24	145.5	5.0	24	174.8	4.9	24	241.8	5.0	24	260.3	5.2
25	192.0	4.3	25	159.7	4.4	25	343.6	4.2	25	195.0	4.9	25	176.5	5.4	25	279.4	4.7	25	206.5	4.9	25	317.9	5.5
26	225.8	4.7	26	224.6	4.7	26	273.4	4.3	26	232.1	5.3	26	216.2	5.2	26	249.6	4.8	26	172.2	4.9	26	279.5	5.2
27	191.3	4.2	27	214.7	4.4	27	340.6	4.3	27	276.9	4.8	27	123.5	5.5	27	221.4	4.6	27	244.6	4.9	27	311.7	5.4
28 f	280.0	1.7	28 f	128.6	1.8	28 f	426.1	1.8	28 f	253.2	1.6	28 f	133.4	1.8	28 f	215.3	1.9	28 f	231.4	1.8	28 f	286.4	1.8
29	170.1	4.6	29	147.2	4.8	29	363.7	4.3	29	178.8	5.2	29	90.6	4.9	29	277.7	4.7	29	208.1	4.8	29	193.9	5.1
30	261.2	4.2	30	142.4	3.9	30	411.9	4.2	30	218.1	4.8	30	137.7	5.3	30	304.2	4.7	30	252.7	5.0	30	218.3	5.4
31	254.0	4.6	31	205.2	4.5	31	338.3	4.3	31	270.5	5.3	31	79.3	4.9	31	174.8	4.7	31	197.9	4.8	31	234.0	5.4
32	210.5	4.5	32	182.0	4.5	32	355.0	4.1	32	225.3	4.8	32	186.1	5.4	32	271.7	4.8	32	190.3	4.9	32	292.0	5.5
33	216.2	4.3	33	119.0	4.5	33	329.0	4.3	33	329.3	5.1	33	123.7	5.3	33	230.6	4.6	33	266.5	4.8	33	147.0	5.1
34	256.0	4.2	34	182.0	4.4	34	364.5	4.1	34	282.6	4.9	34	214.0	5.3	34	277.0	5.0	34	286.4	4.9	34	175.9	5.6
35	206.9	4.7	35	203.1	4.3	35	379.2	4.3	35	193.4	4.9	35	196.7	5.2	35	238.4	4.7	35	293.2	4.9	35	219.6	5.2
36	310.3	4.2	36	247.3	4.1	36	300.3	4.2	36	228.4	4.8	36	192.6	5.4	36	248.3	5.0	36	335.6	4.9	36	177.9	5.6
37	269.1	4.7	37	255.9	4.6	37	274.4	4.5	37	189.1	4.9	37	205.9	4.9	37	320.1	4.8	37	250.4	4.8	37	199.5	5.4
38	210.2	4.2	38	175.1	4.1	38	280.1	4.0	38	247.3	4.8	38	129.4	5.2	38	272.2	4.9	38	277.0	5.0	38	198.7	5.6
39	220.9	4.6	39	140.8	4.4	39	337.0	4.7	39	154.9	5.3	39	108.9	5.8	39	310.7	5.4	39	308.7	5.3	39	314.9	6.1
40	230.1	4.2	40	168.4	4.2	40	323.2	4.0	40	241.6	4.7	40	169.7	5.6	40	290.1	5.0	40	224.3	5.0	40	284.3	5.9
41	264.2	4.2	41	172.4	4.1	41	325.1	3.9	41	228.2	4.4	41	150.4	4.5	41	220.2	4.1	41	268.1	4.5	41	215.5	5.3
42	251.9	4.2	42	213.5	4.5	42	350.9	4.1	42	277.3	4.3	42	215.2	4.7	42	272.8	4.5	42	229.3	5.1	42	252.0	5.7
43	238.5	4.2	43	86.8	4.1	43	297.1	3.8	43	251.8	4.2	43	106.2	4.5	43	213.6	4.2	43	243.2	4.5	43	227.2	4.7
44	181.8	4.3	44	91.9	4.2	44	274.8	4.0	44	199.0	4.5	44	148.2	5.1	44	272.7	4.6	44	217.9	4.6	44	176.6	5.5
45	207.5	4.1	45	225.3	4.2	45	266.0	3.9	45	220.9	4.2	45	181.6	4.7	45	285.0	4.2	45	256.3	4.6	45	156.3	4.9
46	231.6	4.3	46	116.7	4.5	46	314.5	4.2	46	255.1	4.6	46	148.3	4.6	46	258.6	4.6	46	181.9	4.8	46	204.3	5.4
47	270.8	4.4	47	194.6	4.2	47	331.1	3.9	47	275.8	4.2	47	109.2	4.7	47	333.1	4.2	47	210.3	4.7	47	299.5	5.0
48	243.3	4.3	48	226.9	4.3	48	313.1	4.2	48	206.1	4.6	48	250.8	4.7	48	244.8	4.6	48	248.7	4.8	48	262.1	5.5
49	214.5	4.1	49	166.6	4.1	49	303.6	4.3	49	220.2	4.2	49	172.9	4.5	49	260.7	4.3	49	270.0	4.5	49	227.9	4.9
50	141.8	4.3	50	148.1	4.3	50	340.7	4.0	50	192.8	4.6	50	208.0	4.8	50	273.3	4.6	50	286.0	4.7	50	183.0	5.5
51	197.5	4.0	51	141.5	4.1	51	296.9	3.9	51	170.1	4.1	51	179.1	4.6	51	287.1	4.2	51	160.3	4.3	51	276.6	5.0
52	226.5	4.4	52	170.4	4.5	52	362.8	4.3	52	233.7	4.9	52	241.9	5.0	52	241.4	4.6	52	214.0	4.7	52	336.4	5.6
53 f	285.2	1.5	53 f	203.9	1.5	53 f	412.6	1.4	53 f	234.7	1.5	53 f	172.3	1.5	53 f	240.5	1.6	53 f	262.3	1.4	53 f	288.7	1.4
54	177.5	4.0	54	162.4	4.0	54	280.4	3.9	54	235.6	4.1	54	133.6	4.5	54	324.2	4.5	54	261.1	4.5	54	256.9	4.9
55	264.7	4.3	55	185.4	4.5	55	393.8	4.1	55	298.6	4.7	55	80.9	4.8	55	308.4	4.6	55	224.6	4.9	55	342.7	5.7
56	197.9	4.2	56	172.3	4.0	56	269.5	3.8	56	226.6	3.8	56	83.0	4.7	56	273.8	4.7	56	208.4	4.5	56	164.4	4.8
57	218.7	4.5	57	222.7	4.6	57	339.3	4.2	57	289.6	4.6	57	124.6	4.8	57	273.7	4.5	57	233.3	4.6	57	232.5	5.6
58	298.8	4.2	58	141.8	4.0	58	297.2	3.7	58	245.0	4.1	58	186.0	4.7	5								

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	276.0	10.7	1 r	345.5	11.1	1 r	318.2	8.6	1 r	249.8	12.2	1 r	351.0	8.6	1 r	292.7	11.3	1 r	300.4	11.3	1 r	449.1	8.9
2 r	250.8	0.7	2 r	250.6	0.7	2 r	250.3	0.6	2 r	250.4	0.7	2 r	250.3	0.7	2 r	250.3	0.7	2 r	250.3	0.7	2 r	249.9	0.6
3	250.3	5.0	3	249.1	4.9	3	250.2	5.1	3	249.3	6.0	3	250.0	5.7	3	251.9	5.4	3	249.9	5.7	3	250.9	6.1
4	249.8	4.6	4	249.9	4.5	4	249.7	4.4	4	250.4	5.0	4	249.4	5.6	4	250.6	4.9	4	250.1	4.9	4	249.4	5.4
5	251.8	4.9	5	250.6	5.0	5	251.1	4.8	5	248.6	5.8	5	251.0	5.9	5	249.9	5.2	5	250.5	5.4	5	250.9	5.7
6	249.9	4.5	6	251.1	4.7	6	249.5	4.3	6	249.4	4.9	6	252.1	5.7	6	250.9	4.9	6	249.9	4.8	6	249.4	5.5
7	251.8	5.1	7	251.8	5.0	7	249.7	4.7	7	249.9	5.9	7	251.0	5.5	7	251.4	5.0	7	250.7	5.1	7	248.6	5.4
8	250.5	4.3	8	250.6	4.4	8	250.1	4.2	8	249.2	4.8	8	250.4	5.4	8	250.7	4.8	8	250.9	4.8	8	250.9	5.2
9	250.2	4.8	9	250.5	4.7	9	250.8	4.7	9	250.2	5.8	9	249.9	5.4	9	250.0	4.9	9	249.9	5.2	9	250.3	5.6
10	249.4	4.5	10	252.2	4.8	10	249.8	4.1	10	250.5	5.0	10	249.2	5.7	10	252.1	4.7	10	250.6	4.8	10	251.2	5.3
11	250.5	4.9	11	249.2	4.8	11	251.2	4.8	11	250.8	5.3	11	251.4	5.5	11	248.5	4.9	11	251.1	5.1	11	250.3	5.5
12	250.3	4.2	12	250.5	4.5	12	249.6	4.3	12	249.4	4.7	12	252.2	5.6	12	248.9	4.8	12	249.1	5.0	12	253.7	5.2
13	250.1	4.6	13	250.6	4.5	13	250.0	4.6	13	249.0	5.1	13	249.2	5.2	13	250.1	4.7	13	250.5	5.2	13	249.1	5.6
14	249.3	4.2	14	250.9	4.3	14	249.4	4.4	14	248.9	4.8	14	250.3	5.4	14	251.0	4.9	14	250.2	4.9	14	250.7	5.3
15 f	250.5	1.6	15 f	250.1	1.8	15 f	250.2	1.6	15 f	249.9	1.7	15 f	250.2	1.7	15 f	250.6	1.7	15 f	250.1	1.7	15 f	250.7	1.7
16	251.6	4.4	16	249.8	4.8	16	251.0	4.3	16	250.0	5.3	16	249.6	5.1	16	251.5	4.8	16	251.3	5.0	16	252.5	5.4
17	250.7	4.2	17	250.0	4.2	17	251.0	4.3	17	249.8	4.9	17	250.6	5.2	17	249.3	4.8	17	249.0	4.9	17	251.5	5.2
18	249.6	4.7	18	248.7	4.7	18	250.3	4.4	18	250.5	5.2	18	251.3	5.4	18	250.5	5.4	18	251.1	4.9	18	251.1	5.4
19	250.7	4.2	19	250.8	4.4	19	250.6	4.3	19	250.1	4.7	19	250.8	5.6	19	251.3	4.8	19	249.7	4.7	19	249.2	5.3
20	251.1	4.7	20	249.9	4.5	20	249.9	4.0	20	248.4	5.3	20	249.6	5.2	20	250.3	4.8	20	249.6	4.8	20	252.1	5.5
21	250.9	4.3	21	252.0	4.3	21	248.6	4.2	21	247.9	4.8	21	250.8	5.2	21	249.8	5.1	21	250.7	4.7	21	250.4	5.3
22	250.8	4.5	22	251.4	4.7	22	249.3	4.3	22	250.7	5.3	22	251.3	5.2	22	251.9	4.8	22	251.6	5.3	22	250.4	5.3
23	249.2	4.5	23	251.3	4.3	23	251.2	4.3	23	250.4	4.6	23	249.2	5.4	23	249.3	4.7	23	250.0	4.8	23	250.2	5.3
24	250.2	4.6	24	249.7	4.6	24	249.9	4.3	24	250.4	5.0	24	250.4	5.0	24	249.1	4.5	24	249.4	4.8	24	249.9	5.4
25	250.5	4.2	25	251.0	4.2	25	249.5	4.3	25	249.4	4.8	25	249.5	5.2	25	251.3	4.7	25	249.2	4.7	25	250.6	5.2
26	250.3	4.4	26	249.6	4.5	26	251.0	4.6	26	250.7	5.1	26	249.9	5.2	26	251.2	4.7	26	251.0	5.1	26	248.3	5.4
27	251.2	4.2	27	250.8	4.4	27	249.5	4.0	27	250.1	4.5	27	248.5	5.4	27	250.1	4.7	27	249.4	5.1	27	250.3	5.5
28 f	250.9	1.7	28 f	250.1	1.8	28 f	250.7	1.7	28 f	250.2	1.7	28 f	251.1	1.8	28 f	251.0	1.9	28 f	251.1	1.8	28 f	250.9	1.8
29	250.7	4.5	29	251.1	4.6	29	250.2	4.5	29	251.3	5.0	29	249.5	5.0	29	251.1	4.7	29	250.2	4.8	29	248.8	5.4
30	251.2	4.3	30	250.1	4.3	30	248.5	4.2	30	249.5	4.6	30	250.8	5.7	30	249.0	4.7	30	248.4	4.8	30	250.4	5.2
31	250.1	4.8	31	250.4	4.6	31	250.3	4.4	31	248.7	5.0	31	250.2	5.2	31	249.8	4.9	31	251.5	4.8	31	249.4	5.2
32	248.5	4.8	32	249.7	4.4	32	250.0	4.2	32	250.0	4.7	32	249.8	5.1	32	251.1	4.7	32	251.4	4.8	32	249.6	5.2
33	250.7	4.7	33	250.1	4.7	33	249.6	4.3	33	249.2	5.3	33	249.9	4.8	33	249.0	4.8	33	250.8	4.7	33	251.0	5.5
34	251.2	4.1	34	249.5	4.4	34	249.4	4.3	34	249.6	4.6	34	250.8	5.3	34	251.2	4.8	34	251.3	4.6	34	249.4	5.2
35	250.8	4.6	35	250.2	4.7	35	250.1	4.3	35	250.5	4.7	35	251.3	5.1	35	250.1	4.8	35	251.3	4.8	35	250.1	5.5
36	249.9	4.5	36	251.1	4.5	36	251.4	4.2	36	250.9	4.5	36	249.6	5.4	36	250.1	5.1	36	250.6	4.8	36	250.1	5.6
37	249.7	4.6	37	251.1	4.4	37	250.2	4.5	37	250.5	4.7	37	249.5	5.0	37	249.5	4.7	37	250.3	4.9	37	249.4	5.5
38	250.3	4.3	38	250.3	4.0	38	250.1	4.1	38	251.3	4.8	38	248.8	5.4	38	251.6	4.9	38	250.5	5.0	38	249.8	5.5
39	250.4	4.7	39	249.6	4.5	39	249.2	4.2	39	250.4	4.9	39	250.6	5.5	39	250.7	5.1	39	248.5	5.4	39	248.9	5.9
40	250.7	4.4	40	251.7	4.2	40	251.7	4.1	40	250.6	4.9	40	251.3	5.5	40	250.4	4.8	40	250.3	5.1	40	250.5	5.7
41	250.4	4.1	41	249.6	4.0	41	249.4	3.9	41	249.7	4.2	41	251.5	4.6	41	251.0	4.2	41	249.0	4.2	41	249.2	4.8
42	250.3	4.3	42	249.8	4.3	42	250.7	4.0	42	250.9	4.7	42	251.3	5.1	42	249.7	4.9	42	252.7	4.7	42	250.8	5.6
43	250.1	4.3	43	249.2	4.1	43	249.4	3.9	43	249.5	4.2	43	251.1	4.6	43	250.5	4.2	43	251.1	4.3	43	250.0	4.8
44	250.8	4.2	44	251.5	4.1	44	250.3	4.2	44	250.0	4.5	44	250.9	4.7	44	250.4	4.5	44	250.3	4.7	44	249.7	5.6
45	248.8	4.0	45	249.1	3.9	45	250.0	4.1	45	249.0	4.0	45	250.5	4.6	45	250.1	4.4	45	250.3	4.4	45	250.0	4.8
46	250.0	4.3	46	251.3	4.3	46	249.7	4.2	46	249.4	4.5	46	249.3	4.6	46	248.4	4.5	46	250.4	4.8	46	248.5	5.8
47	250.3	4.4	47	249.7	4.1	47	249.1	3.9	47	249.4	3.9	47	253.5	4.4	47	250.2	4.2	47	250.9	4.2	47	250.4	4.8
48	249.4	4.4	48	249.2	4.4	48	249.3	4.1	48	250.3	4.8	48	249.1	4.7	48	250.0	4.5	48	250.2	4.8	48	250.6	5.5
49	251.0	4.3	49	249.9	4.1	49	249.0	3.9	49	249.4	4.2	49	250.9	4.5	49	250.0	4.3	49	250.2	4.3	49	249.2	4.8
50	249.2	4.2	50	250.5	4.4	50	249.0	4.2	50	250.8	4.5	50	251.8	4.5	50	251.6	4.5	50	249.9	4.6	50	250.3	5.5
51	251.0	4.2	51	248.6	3.9	51	250.2	3.8	51	249.5	4.2	51	250.2	4.4	51	250.2	4.3	51	249.9	4.3	51	249.9	4.8
52	250.2	4.5	52	249.3	4.7	52	249.7	4.0	52	250.6	4.6	52	250.2	4.6	52	250.1	4.5	52	250.5	4.7	52	252.7	5.6
53 f	250.6	1.6	53 f	250.2	1.5	53 f	250.1	1.4	53 f	249.4	1.5	53 f	251.1	1.5	53 f	251.4	1.5	53 f	250.6	1.4	53 f	250.1	1.4
54	250.1	4.3	54	249.8	4.1	54	249.9	4.1	54	249.8	4.2	54	249.8	4.2	54	249.7	4.5	54	251.1	4.4	54	250.1	4.9
55	248.2	4.4	55	251.2	4.4	55	249.4	4.4	55	249.6	4.5	55	251.0	4.5	55	251.3	4.6	55	250.9	4.9	55	248.7	5.6
56	249.6	4.3	56	251.2	4.0	56	249.9	3.8	56	250.6	4.2	56	251.4	4.7	56	248.9	4.3	56	250.6	4.3	56	250.0	4.9
57	249.3	4.4	57	248.5	4.3	57	251.8	4.2	57	249.5	4.4	57	248.9	4.6	57	250.2	4.7	57	251.6	4.6	57	250.0	5.8
58	249.4	4.4	58	248.6	4.0	58	250.0	3.9	58	249.8	4.2												