

Fec test report:

Date: 2021-03-31 14:42:02

Tester name: lc

Test#1 Monitoring values

Failed

0	FEC label	061	OK
1	FEC DC2438 ID	ad0000024d9e0526	OK
2	FEC_T (to 35°C)	25.594	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.6A)	1.674	FAIL
5	FEC_Vad (1.9V to 2.0V)	1.940	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3020	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3084	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3001	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3086	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3057	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3025	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3029	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3028	OK

FEC test final result:

Failed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 25.594 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.837 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: ad0000024d9e0526

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x12048000 (302284800) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdc(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdc(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdc(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdc(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdc(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdc(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdc(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdc(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdc(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdc(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdc(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdc(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdc(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdc(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdc(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdc(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdc(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdc(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdc(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdc(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdc(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdc(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdc(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdc(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdc(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdc(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdc(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdc(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdc(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdc(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdc(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdc(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdc(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V

115	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xff7	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdc(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdc(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
191	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.940 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.940 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	510.7	1.2	1 r	511.0	0.0	1 r	510.1	2.3	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	300.7	0.7	2 r	285.0	0.7	2 r	316.0	0.7	2 r	340.7	0.7	2 r	264.9	0.7	2 r	354.9	0.7	2 r	272.4	0.7	2 r	339.3	0.7
3	240.5	5.4	3	183.9	5.5	3	228.1	5.8	3	245.1	6.8	3	173.5	6.0	3	301.3	5.2	3	218.6	5.8	3	351.1	6.0
4	203.0	4.5	4	270.2	4.5	4	309.3	4.6	4	269.5	5.3	4	235.5	5.4	4	293.3	4.7	4	223.1	4.9	4	345.8	5.4
5	228.7	5.1	5	182.1	5.4	5	220.2	5.8	5	294.6	6.4	5	115.6	5.6	5	247.3	5.0	5	230.4	5.3	5	210.5	5.8
6	242.4	4.7	6	248.4	4.6	6	236.1	4.4	6	266.0	5.1	6	159.1	5.4	6	318.8	4.9	6	180.8	5.0	6	218.8	5.2
7	161.4	5.2	7	222.6	5.4	7	285.0	5.3	7	212.0	6.4	7	218.3	5.5	7	173.1	4.7	7	150.3	5.3	7	299.2	5.8
8	163.1	4.5	8	196.4	4.8	8	166.1	4.3	8	340.6	5.1	8	155.3	5.6	8	284.8	4.5	8	122.7	4.6	8	298.3	5.2
9	183.2	5.2	9	139.4	5.2	9	242.2	5.2	9	190.9	6.0	9	195.4	5.5	9	161.8	4.9	9	171.8	5.2	9	344.4	5.7
10	205.0	4.8	10	165.8	4.5	10	274.5	4.4	10	317.4	5.0	10	114.2	5.2	10	189.2	4.6	10	152.4	4.9	10	262.2	5.4
11	233.6	5.2	11	184.8	5.1	11	285.8	5.2	11	219.5	5.8	11	233.6	5.4	11	247.4	4.9	11	186.8	5.1	11	261.0	5.7
12	158.3	4.5	12	204.1	4.5	12	251.8	4.2	12	263.3	5.0	12	171.1	5.2	12	350.4	4.7	12	242.4	5.0	12	289.9	5.3
13	215.6	5.0	13	216.7	5.0	13	273.6	5.2	13	282.8	5.8	13	178.8	5.5	13	224.8	4.8	13	198.8	5.1	13	220.6	5.7
14	241.1	4.6	14	171.6	4.5	14	190.0	4.5	14	177.8	5.1	14	189.0	5.2	14	306.4	4.7	14	183.7	4.9	14	322.8	5.2
15 f	159.4	1.8	15 f	226.0	1.6	15 f	302.9	1.6	15 f	186.2	1.5	15 f	139.6	1.6	15 f	249.0	1.7	15 f	130.8	1.6	15 f	296.1	1.6
16	242.7	4.9	16	250.7	5.0	16	268.6	5.3	16	211.5	5.8	16	79.0	5.2	16	241.2	4.9	16	189.2	5.2	16	306.3	5.7
17	186.9	4.4	17	117.7	4.5	17	279.1	4.4	17	219.0	5.1	17	120.4	5.0	17	278.0	4.7	17	199.3	4.7	17	278.5	5.0
18	205.8	5.0	18	288.5	5.0	18	242.6	5.0	18	231.4	5.8	18	45.8	5.2	18	305.4	4.8	18	136.7	5.4	18	296.9	5.4
19	182.9	4.3	19	118.9	4.4	19	323.3	4.4	19	268.2	4.6	19	168.6	5.3	19	265.7	4.6	19	238.5	4.8	19	338.2	5.2
20	216.9	4.9	20	205.4	4.7	20	267.4	5.0	20	267.9	5.7	20	114.6	5.3	20	267.6	4.7	20	109.4	5.1	20	333.8	5.1
21	235.1	4.4	21	228.3	4.6	21	305.8	4.5	21	254.3	4.8	21	193.4	5.2	21	248.2	4.8	21	191.1	4.8	21	265.2	5.0
22	159.0	5.0	22	229.4	4.8	22	229.8	5.1	22	201.9	5.8	22	166.2	5.1	22	273.6	4.8	22	175.6	5.1	22	269.2	5.4
23	235.2	4.4	23	146.6	4.4	23	256.9	4.5	23	258.1	4.7	23	181.0	5.2	23	249.4	4.5	23	135.2	4.9	23	253.6	5.2
24	231.3	4.9	24	230.5	5.0	24	221.2	5.0	24	194.1	5.4	24	191.1	5.4	24	286.6	4.8	24	96.4	5.2	24	338.3	5.5
25	268.5	4.6	25	151.4	4.5	25	252.3	4.3	25	258.5	4.5	25	105.1	4.9	25	227.0	4.5	25	190.1	4.7	25	269.5	5.0
26	278.3	4.8	26	159.8	4.7	26	324.8	4.9	26	327.6	5.5	26	217.9	5.0	26	282.4	4.8	26	133.9	5.1	26	341.1	5.7
27	220.2	4.6	27	250.2	4.5	27	287.7	4.1	27	209.0	4.7	27	204.7	5.3	27	275.3	4.6	27	167.7	4.8	27	221.4	5.3
28 f	159.8	1.9	28 f	152.2	1.9	28 f	304.8	1.6	28 f	231.4	1.6	28 f	232.1	1.8	28 f	246.7	1.7	28 f	120.5	1.7	28 f	353.1	1.8
29	278.6	4.9	29	180.1	5.0	29	243.4	5.0	29	199.9	5.3	29	198.1	5.0	29	226.1	4.8	29	189.2	5.0	29	320.9	5.3
30	258.7	4.5	30	130.5	4.4	30	303.9	4.1	30	225.5	4.7	30	245.2	5.1	30	214.7	4.7	30	104.9	4.8	30	200.4	5.3
31	172.7	4.7	31	229.9	4.6	31	223.9	4.9	31	158.1	5.3	31	199.2	5.3	31	229.2	4.7	31	167.5	4.8	31	234.8	5.3
32	271.6	4.5	32	167.6	4.4	32	244.4	4.5	32	268.1	4.5	32	154.0	5.0	32	230.8	4.8	32	186.9	4.7	32	298.1	5.2
33	274.6	4.8	33	196.9	4.7	33	227.4	4.8	33	171.3	5.3	33	223.5	5.0	33	242.6	4.9	33	162.1	5.1	33	222.9	5.4
34	177.1	4.4	34	206.8	4.2	34	268.4	4.2	34	260.1	4.7	34	167.3	5.1	34	294.9	4.7	34	169.6	4.8	34	276.6	5.2
35	208.1	5.1	35	234.0	4.9	35	176.2	5.0	35	310.0	5.3	35	176.0	5.4	35	363.3	4.7	35	152.1	5.1	35	344.0	5.5
36	325.0	4.3	36	230.2	4.4	36	242.5	4.3	36	295.3	4.8	36	128.0	5.3	36	278.6	4.7	36	243.8	4.8	36	284.7	5.3
37	244.3	4.9	37	146.0	5.0	37	284.2	4.7	37	206.2	5.2	37	194.1	5.0	37	242.9	4.8	37	168.3	5.0	37	303.1	5.4
38	224.3	4.8	38	122.5	4.4	38	185.9	4.4	38	227.7	4.6	38	162.7	5.2	38	232.1	4.8	38	205.1	4.7	38	215.4	5.2
39	171.8	4.9	39	197.7	4.8	39	299.1	4.6	39	260.5	5.2	39	260.0	5.4	39	272.0	5.0	39	169.7	5.4	39	233.9	5.7
40	149.5	4.3	40	237.3	4.2	40	246.2	4.3	40	306.1	4.6	40	252.2	5.1	40	224.3	4.7	40	270.7	4.8	40	185.3	5.3
41	302.4	4.2	41	204.8	3.9	41	224.4	4.0	41	173.8	3.9	41	240.4	4.3	41	322.3	4.1	41	164.3	4.2	41	251.7	4.7
42	235.3	4.4	42	209.3	4.2	42	298.0	4.5	42	189.5	4.9	42	198.0	4.6	42	290.6	4.6	42	213.8	4.8	42	300.1	5.7
43	254.3	4.5	43	264.5	4.2	43	291.1	3.9	43	293.0	4.0	43	119.8	4.6	43	210.8	4.0	43	226.8	4.1	43	202.3	4.6
44	225.2	4.1	44	217.2	4.4	44	308.3	4.3	44	337.1	4.7	44	202.5	4.7	44	259.7	4.4	44	181.4	4.7	44	308.3	5.5
45	245.4	4.0	45	231.4	4.0	45	272.2	3.9	45	247.3	4.0	45	183.2	4.5	45	238.6	3.9	45	144.8	4.3	45	260.9	4.5
46	193.6	4.8	46	154.1	4.5	46	285.8	4.3	46	324.1	4.9	46	158.7	4.6	46	288.1	4.3	46	188.5	4.6	46	228.5	5.2
47	240.0	4.0	47	221.9	4.1	47	201.5	4.0	47	190.2	3.9	47	82.0	4.5	47	171.4	4.2	47	196.6	4.1	47	278.0	4.6
48	192.5	4.5	48	124.4	4.3	48	350.6	4.5	48	285.9	5.0	48	199.8	4.7	48	271.2	4.5	48	157.1	4.7	48	244.3	5.4
49	215.0	3.8	49	228.3	4.0	49	327.1	4.2	49	245.0	4.0	49	257.3	4.5	49	250.2	4.3	49	209.8	4.2	49	246.7	4.8
50	187.6	4.5	50	133.8	4.3	50	258.0	4.4	50	304.9	4.7	50	181.3	4.5	50	344.2	4.3	50	74.2	4.7	50	293.5	5.3
51	253.7	4.1	51	177.1	4.0	51	238.2	3.9	51	297.8	4.0	51	175.7	4.7	51	264.4	4.0	51	107.4	4.5	51	268.6	4.5
52	169.6	4.4	52	210.6	4.3	52	227.6	4.4	52	234.9	4.8	52	132.0	4.9	52	189.8	4.4	52	132.1	4.8	52	267.4	5.6
53 f	252.3	1.5	53 f	223.1	1.5	53 f	232.6	1.4	53 f	212.7	1.5	53 f	180.9	1.5	53 f	279.3	1.4	53 f	181.0	1.4	53 f	269.7	1.5
54	211.3	4.2	54	177.7	4.1	54	170.8	3.9	54	206.2	4.0	54	87.3	4.4	54	269.7	4.2	54	112.5	4.3	54	377.3	4.7
55	227.7	4.2	55	228.1	4.6	55	255.0	4.3	55	224.6	4.4	55	167.8	4.5	55	180.7	4.3	55	221.1	4.6	55	264.4	5.5
56	166.8	4.0	56	141.2	4.1	56	314.3	4.1	56	256.2	4.0	56	143.6	4.5	56	185.0	4.2	56	134.6	4.2	56	176.8	4.7
57	198.1	4.6	57	174.2	4.5	57	368.4	4.4	57	270.3	4.8	57	147.4	5.0	57	229.7	4.3	57	236.8	4.8	57	315.7	5.4
58	254.7	4.1	58	208.7	3.8	58	279.2</																

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	374.0	7.9	1 r	267.6	10.5	1 r	368.8	9.2	1 r	265.2	11.7	1 r	289.0	9.5	1 r	440.1	8.1	1 r	333.7	8.9	1 r	354.6	12.6
2 r	249.8	0.7	2 r	250.1	0.7	2 r	250.1	0.7	2 r	249.9	0.7	2 r	250.4	0.7	2 r	250.0	0.7	2 r	250.8	0.7	2 r	250.3	0.7
3	249.1	4.9	3	250.6	5.0	3	249.8	5.2	3	250.8	6.0	3	252.3	5.5	3	251.7	4.9	3	250.3	5.3	3	249.9	5.6
4	250.5	4.6	4	250.8	4.4	4	250.1	4.7	4	251.1	5.0	4	251.8	5.0	4	250.4	4.5	4	250.4	4.9	4	249.3	5.0
5	250.3	4.9	5	251.3	5.0	5	250.4	5.0	5	251.6	5.8	5	249.8	5.1	5	250.2	4.9	5	252.2	5.1	5	249.4	5.4
6	252.0	4.3	6	250.6	4.4	6	251.3	4.3	6	250.4	4.9	6	250.4	5.0	6	251.4	4.5	6	249.1	5.0	6	249.8	5.1
7	250.5	5.1	7	250.5	5.1	7	250.7	5.4	7	251.2	5.7	7	249.8	5.0	7	251.0	4.7	7	250.7	5.1	7	251.3	5.2
8	250.7	4.5	8	249.8	4.2	8	250.9	4.5	8	250.0	4.7	8	252.9	5.0	8	250.7	4.5	8	250.0	4.8	8	250.6	4.9
9	249.2	4.8	9	251.3	4.9	9	250.8	4.7	9	250.2	5.3	9	251.8	5.2	9	250.1	4.7	9	251.1	4.9	9	251.3	5.7
10	251.7	4.4	10	249.8	4.8	10	251.7	4.2	10	250.0	4.7	10	251.6	5.0	10	250.8	4.8	10	251.2	4.7	10	250.7	4.9
11	249.7	4.9	11	250.0	4.5	11	249.1	4.7	11	250.0	5.2	11	250.7	4.8	11	249.6	4.6	11	249.2	4.8	11	252.1	5.3
12	250.3	4.5	12	250.3	4.4	12	250.4	4.5	12	252.3	4.8	12	250.0	5.0	12	251.4	4.7	12	251.1	4.7	12	249.7	5.0
13	250.7	4.6	13	250.1	4.9	13	250.5	4.7	13	249.9	5.5	13	250.7	4.8	13	250.7	4.7	13	251.0	5.0	13	250.2	5.5
14	250.8	4.2	14	248.8	4.3	14	250.7	4.5	14	250.3	4.4	14	251.2	4.7	14	252.5	4.6	14	249.7	4.7	14	250.1	4.9
15 f	250.4	1.8	15 f	250.5	1.7	15 f	249.7	1.6	15 f	250.7	1.6	15 f	249.8	1.7	15 f	249.7	1.6	15 f	249.9	1.6	15 f	250.6	1.6
16	250.3	4.5	16	249.7	4.7	16	251.6	4.9	16	250.7	5.2	16	250.6	5.0	16	250.8	4.6	16	252.1	4.8	16	250.8	5.2
17	250.2	4.4	17	250.2	4.3	17	250.8	4.4	17	249.9	4.5	17	250.1	4.8	17	251.7	4.7	17	251.4	4.8	17	250.6	5.0
18	249.7	4.6	18	249.7	4.3	18	250.2	4.6	18	251.4	5.0	18	250.1	5.0	18	250.9	4.7	18	250.4	4.9	18	250.1	5.2
19	249.4	4.2	19	249.6	4.1	19	250.4	4.2	19	250.0	4.2	19	250.0	5.0	19	250.0	4.4	19	250.7	4.6	19	250.3	4.7
20	250.2	4.7	20	250.5	4.6	20	251.4	4.7	20	250.6	5.0	20	249.5	4.8	20	250.3	4.5	20	250.7	4.7	20	249.5	5.0
21	250.5	4.2	21	250.3	4.3	21	251.3	4.6	21	251.1	4.7	21	250.8	5.0	21	249.7	4.7	21	251.0	4.5	21	250.2	4.9
22	249.7	4.5	22	250.8	4.7	22	251.6	4.6	22	250.4	5.0	22	251.4	4.9	22	249.7	4.3	22	250.8	4.7	22	251.3	5.0
23	250.8	4.2	23	250.5	4.3	23	251.2	4.6	23	250.8	4.4	23	252.9	4.8	23	250.7	4.4	23	249.6	4.4	23	251.2	4.8
24	250.3	4.5	24	248.7	4.5	24	250.0	4.6	24	249.0	4.8	24	251.7	4.9	24	250.2	4.6	24	250.9	4.7	24	250.4	5.2
25	249.5	4.3	25	249.4	4.3	25	250.9	4.4	25	251.0	4.5	25	250.2	4.8	25	250.5	4.4	25	250.7	4.4	25	249.0	4.9
26	250.4	4.6	26	250.4	4.7	26	252.2	4.5	26	250.3	4.9	26	251.5	4.9	26	252.2	4.4	26	252.1	4.6	26	249.3	4.9
27	252.1	4.3	27	249.8	4.4	27	251.1	4.5	27	251.7	4.5	27	249.5	4.8	27	251.7	4.4	27	251.2	4.7	27	251.3	4.9
28 f	249.9	1.8	28 f	250.7	1.9	28 f	250.1	1.8	28 f	251.4	1.6	28 f	250.9	1.8	28 f	250.5	1.7	28 f	251.5	1.7	28 f	249.8	1.7
29	248.9	4.5	29	249.7	4.4	29	251.4	4.6	29	251.2	4.9	29	248.1	4.8	29	251.4	4.3	29	251.1	4.9	29	250.2	5.1
30	251.2	4.3	30	250.9	4.2	30	250.6	4.5	30	250.4	4.4	30	250.8	4.8	30	249.3	4.3	30	250.8	4.5	30	249.8	5.3
31	249.8	4.3	31	249.7	4.6	31	250.2	4.5	31	250.8	4.8	31	251.2	4.8	31	249.2	4.6	31	249.2	4.6	31	249.9	5.2
32	249.6	4.5	32	250.8	4.3	32	251.1	4.3	32	250.2	4.3	32	251.1	4.9	32	249.8	4.4	32	251.0	4.7	32	249.2	4.9
33	251.0	4.8	33	250.3	4.6	33	251.2	4.4	33	249.9	4.5	33	249.9	4.6	33	250.4	4.7	33	251.0	4.8	33	249.9	5.0
34	250.9	4.3	34	249.2	4.1	34	249.9	4.1	34	250.3	4.5	34	252.6	4.7	34	248.9	4.6	34	250.1	4.5	34	250.0	4.9
35	249.5	4.5	35	250.7	4.6	35	250.5	4.4	35	251.1	4.6	35	250.7	4.7	35	250.1	4.3	35	251.6	4.6	35	250.3	5.1
36	249.0	4.0	36	251.2	4.3	36	250.8	4.1	36	251.5	4.3	36	250.9	4.9	36	249.1	4.5	36	252.3	4.7	36	249.5	4.9
37	250.6	4.4	37	250.5	4.6	37	251.6	4.6	37	252.0	4.6	37	250.2	4.4	37	251.5	4.4	37	251.4	5.0	37	251.1	4.9
38	250.8	4.3	38	248.8	4.5	38	250.6	4.4	38	250.2	4.3	38	250.5	4.8	38	249.5	4.7	38	251.2	4.7	38	250.7	5.0
39	251.0	4.6	39	249.3	4.4	39	251.2	4.6	39	250.4	4.8	39	250.0	5.1	39	249.7	5.0	39	251.6	4.9	39	249.9	5.5
40	248.7	4.2	40	250.8	4.2	40	250.8	4.1	40	248.7	4.3	40	250.8	5.0	40	250.5	4.4	40	250.5	4.7	40	251.1	5.2
41	251.0	4.1	41	250.2	4.0	41	251.1	4.0	41	250.4	4.0	41	250.8	4.2	41	250.6	4.2	41	251.6	4.1	41	250.5	4.8
42	250.2	4.5	42	251.5	4.7	42	251.1	4.3	42	249.0	4.4	42	250.5	4.8	42	251.0	4.4	42	250.8	5.0	42	250.7	5.3
43	250.2	4.3	43	248.9	4.0	43	251.4	3.8	43	250.7	4.1	43	251.2	4.3	43	250.2	4.3	43	250.4	4.3	43	250.2	4.9
44	251.0	4.3	44	250.8	4.5	44	250.0	4.3	44	249.4	4.6	44	251.4	4.5	44	251.0	4.4	44	251.1	4.6	44	251.0	5.5
45	249.2	4.0	45	250.5	4.1	45	250.6	4.0	45	251.1	4.1	45	251.4	4.3	45	249.5	4.2	45	252.4	4.2	45	249.3	4.7
46	248.9	4.5	46	249.8	4.5	46	250.3	4.5	46	250.1	4.6	46	251.9	4.8	46	249.8	4.5	46	250.7	4.8	46	249.7	5.4
47	250.1	4.0	47	250.6	4.0	47	249.4	3.9	47	251.6	4.0	47	249.3	4.4	47	251.3	4.3	47	251.0	4.3	47	248.6	4.7
48	249.4	4.6	48	251.3	4.2	48	249.2	4.5	48	250.5	4.5	48	248.5	4.8	48	251.0	4.4	48	250.3	4.5	48	250.8	5.4
49	250.2	4.3	49	249.2	4.0	49	251.0	4.0	49	249.6	3.7	49	253.0	4.3	49	249.9	4.0	49	250.7	4.5	49	251.7	4.9
50	249.2	4.6	50	251.5	4.3	50	250.5	4.4	50	250.4	4.6	50	251.1	4.5	50	249.2	4.4	50	250.5	4.8	50	249.7	5.4
51	249.6	4.0	51	250.6	4.0	51	249.4	4.0	51	248.2	3.9	51	250.3	4.3	51	250.9	4.3	51	250.9	4.3	51	250.0	4.5
52	250.4	4.6	52	250.8	4.5	52	250.0	4.4	52	250.6	4.8	52	251.1	4.8	52	250.6	4.4	52	250.1	4.6	52	249.9	5.5
53 f	250.6	1.5	53 f	250.2	1.5	53 f	249.9	1.6	53 f	250.3	1.4	53 f	250.9	1.7	53 f	250.4	1.5	53 f	250.5	1.4	53 f	249.8	1.6
54	250.2	4.1	54	250.3	4.1	54	250.2	4.3	54	251.3	3.9	54	250.7	4.3	54	250.4	4.0	54	250.8	4.3	54	251.1	4.8
55	250.6	4.4	55	252.0	4.6	55	251.8	4.5	55	250.1	4.6	55	251.2	4.8	55	251.2	4.8	55	252.8	4.9	55	251.3	5.4
56	250.8	4.3	56	250.2	4.0	56	249.6	3.9	56	249.6	4.4	56	251.4	4.5	56	250.4	4.2	56	249.7	4.2	56	249.4	4.6
57	250.2	4.5	57	250.0	4.3	57	250.7	4.6	57	250.4	4.9	57	250.0	4.9	57	250.5	4.5	57	250.8	4.8	57	249.4	5.3
58	250.8	4.1	58	250.9	4.0	58	249.8	4.0	58	250.7	4.0												