

Fec test report:

Date: 2021-04-28 08:17:16

Tester name: LC

Test#1 Monitoring values

Passed

0	FEC label	058	OK
1	FEC DC2438 ID	2d0000024d9ea126	OK
2	FEC_T (to 35°C)	25.500	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.2A to 1.6A)	1.406	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.3 < rms < 8.0 (fpm 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3025	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3073	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3068	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3032	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3081	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3048	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2946	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3006	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(2) Fem(00) FEC_T: 25.500 degC
2	fe 0 moni V 0	0	0 Tdcm(2) Fem(00) FEC_Vdd: 3.290 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(2) Fem(00) FEC_I: 0.703 A
8	fe 0 moni S 0	0	0 Tdcm(2) Fem(00) FEC_Serial: 2d0000024d9ea126

Slow control registers test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe fec_enable 1	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x40000
2	fe fec_enable	0	0 Tdcm(2) Fem(00) Reg(1) = 0x2048000 (33849344) FEC_Enable: 1
3	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
4	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0101 0x0101 (1 chip verified)
12	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0202 0x0202 (1 chip verified)
13	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0303 0x0303 (1 chip verified)
14	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0404 0x0404 (1 chip verified)
15	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0505 0x0505 (1 chip verified)
16	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0606 0x0606 (1 chip verified)
17	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0707 0x0707 (1 chip verified)
18	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0808 0x0808 (1 chip verified)
19	fe 0 after 0 read 3	0	0 Tdcm(2) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
20	fe 0 after 1 read 3	0	0 Tdcm(2) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
21	fe 0 after 2 read 3	0	0 Tdcm(2) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
22	fe 0 after 3 read 3	0	0 Tdcm(2) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
23	fe 0 after 4 read 3	0	0 Tdcm(2) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
24	fe 0 after 5 read 3	0	0 Tdcm(2) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
25	fe 0 after 6 read 3	0	0 Tdcm(2) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
26	fe 0 after 7 read 3	0	0 Tdcm(2) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
27	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
28	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(2) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFF F	0	0 Tdcm(2): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(2) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)
19	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)

21	fe adc 0 write 0x5 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(2) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(2) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(2) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(2) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(2) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(2) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFF F	0	0 Tdcm(2): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(2) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(2) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(2) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(2) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(2) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(2) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(2) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(2) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(2) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(2) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(2) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(2) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(2) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(2) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(2) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(2) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(2) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(2) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(2) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
35	be 0 restart	0	0 Tdcm(2) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(2) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)

37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(2) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(2) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(2) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
113	fe pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V

115	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xffff	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffff0000
136	fe 0 after 3 test_mode 0x1	0	0 TdcM(2) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 TdcM(2) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 TdcM(2) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 TdcM(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 TdcM(2) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 TdcM(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 TdcM(2) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 TdcM(2) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 TdcM(2) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 TdcM(2) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 TdcM(2) Fem(00) Reg(1) <- 0x

193	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdc(2) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdc(2) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdc(2) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdc(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdc(2) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdc(2) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdc(2) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdc(2) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdc(2) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdc(2) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdc(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
269	fe 0 moni A 0	0	0 Tdc(2) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdc(2) Fem(00) Pulser_Amplitude <- 0x3e1c

271	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
273	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
278	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
283	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(2) Fem(00) Pulser_Base <- 0x3fff
288	fe 0 pulser 0 load	0	0 Tdcm(2) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(2) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(2) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(2) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(2) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(2) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	309.1	0.7	2 r	329.3	0.7	2 r	310.8	0.7	2 r	289.3	0.7	2 r	288.2	0.7	2 r	299.1	0.7	2 r	404.2	0.6	2 r	398.6	0.7
3	253.4	5.2	3	328.0	5.5	3	306.2	5.4	3	251.8	6.5	3	237.1	6.2	3	213.7	5.4	3	288.6	5.0	3	348.9	5.5
4	297.9	4.8	4	358.2	4.5	4	308.7	4.8	4	232.0	5.6	4	184.3	6.3	4	232.0	4.9	4	430.3	4.8	4	393.7	5.4
5	224.3	5.0	5	254.5	5.3	5	258.6	5.3	5	288.5	6.3	5	262.4	5.7	5	224.9	5.0	5	339.6	4.7	5	342.9	5.5
6	319.8	4.5	6	260.6	4.4	6	238.5	4.6	6	216.0	5.6	6	225.1	6.0	6	247.4	4.8	6	323.0	4.6	6	275.8	5.2
7	260.8	5.3	7	305.4	5.1	7	282.3	5.3	7	247.2	6.3	7	218.7	5.5	7	248.7	5.0	7	288.3	4.9	7	339.4	5.3
8	222.0	4.6	8	250.5	4.5	8	261.6	4.5	8	293.9	5.5	8	229.0	5.8	8	180.6	4.9	8	335.4	4.8	8	342.2	5.3
9	262.4	5.0	9	255.2	5.3	9	284.9	4.9	9	235.8	5.9	9	234.9	5.5	9	259.2	5.0	9	281.1	4.8	9	253.6	5.3
10	291.2	4.4	10	251.7	4.3	10	270.4	4.4	10	245.3	5.5	10	221.6	6.3	10	200.1	4.9	10	358.1	4.6	10	329.2	5.6
11	218.9	4.9	11	295.5	4.9	11	267.9	4.8	11	233.4	5.8	11	293.9	5.3	11	277.2	4.9	11	282.4	4.7	11	328.4	5.3
12	234.8	4.7	12	297.9	4.6	12	187.2	4.4	12	262.0	5.3	12	180.9	5.9	12	171.5	4.8	12	390.4	4.5	12	344.8	5.1
13	280.1	5.0	13	287.2	4.8	13	194.2	4.9	13	230.7	5.6	13	214.1	5.5	13	199.4	4.8	13	340.7	4.5	13	260.4	5.2
14	185.6	4.4	14	278.9	4.4	14	258.3	4.3	14	191.4	5.2	14	176.8	5.7	14	257.4	4.7	14	328.7	4.5	14	402.4	5.1
15 f	298.2	1.7	15 f	291.6	1.8	15 f	235.7	1.7	15 f	207.2	1.8	15 f	242.4	1.7	15 f	224.0	1.8	15 f	357.3	1.5	15 f	365.8	1.7
16	236.0	5.0	16	266.5	4.5	16	269.6	4.8	16	277.6	5.7	16	229.9	5.4	16	184.3	4.8	16	310.8	4.2	16	287.5	5.3
17	242.7	4.5	17	341.4	4.4	17	232.4	4.5	17	247.6	5.5	17	213.2	5.5	17	186.3	5.0	17	300.8	4.5	17	256.5	4.9
18	253.9	5.1	18	339.3	4.8	18	163.0	4.9	18	239.3	5.6	18	217.5	5.2	18	267.5	4.6	18	369.0	4.3	18	275.2	5.1
19	236.6	4.4	19	283.0	4.5	19	248.2	4.4	19	267.1	5.0	19	238.6	5.8	19	217.7	4.7	19	333.9	4.4	19	427.3	5.2
20	228.8	5.0	20	390.9	4.8	20	161.7	4.9	20	296.2	5.6	20	222.9	5.1	20	207.3	4.7	20	306.6	4.5	20	304.6	5.0
21	200.4	4.5	21	278.6	4.5	21	386.6	4.2	21	274.8	5.3	21	322.5	5.5	21	192.6	4.8	21	326.4	4.5	21	286.1	5.2
22	284.7	4.8	22	224.4	4.7	22	286.0	4.6	22	201.8	5.6	22	194.1	5.2	22	287.7	4.8	22	306.8	4.4	22	252.1	5.0
23	290.9	4.6	23	247.9	4.3	23	258.9	4.3	23	173.6	5.3	23	238.3	5.3	23	252.7	4.7	23	376.0	4.4	23	254.5	5.2
24	237.5	4.9	24	258.8	4.5	24	198.7	4.7	24	280.3	5.1	24	225.3	5.5	24	257.6	4.7	24	274.7	4.4	24	281.7	5.1
25	248.0	4.4	25	289.8	4.4	25	183.8	4.3	25	248.8	5.2	25	321.1	5.6	25	277.9	4.7	25	319.7	4.5	25	298.1	5.2
26	262.3	4.8	26	298.8	5.1	26	301.3	4.8	26	234.5	5.4	26	176.7	5.1	26	255.3	4.8	26	273.5	4.6	26	323.7	5.0
27	278.6	4.5	27	417.3	4.5	27	265.0	4.1	27	209.2	5.1	27	285.4	5.5	27	199.3	4.9	27	336.5	4.5	27	348.2	5.3
28 f	235.3	1.8	28 f	241.2	2.0	28 f	249.7	1.8	28 f	190.6	1.9	28 f	138.5	1.8	28 f	185.5	1.7	28 f	318.1	1.7	28 f	366.4	1.8
29	246.2	4.5	29	325.2	4.8	29	183.6	4.8	29	257.8	5.3	29	253.5	5.2	29	255.9	4.6	29	363.3	4.5	29	201.6	5.0
30	299.2	4.5	30	272.8	4.3	30	227.2	4.6	30	267.1	5.1	30	177.3	5.3	30	194.8	4.7	30	353.1	4.7	30	292.4	5.6
31	356.3	4.8	31	359.5	4.6	31	193.6	4.9	31	200.9	5.3	31	275.1	5.1	31	253.4	4.8	31	313.7	4.4	31	388.9	5.1
32	267.9	4.3	32	313.5	4.2	32	264.3	4.3	32	256.3	5.3	32	268.6	5.6	32	181.7	4.8	32	233.3	4.4	32	392.1	5.3
33	308.2	4.8	33	278.9	4.8	33	217.0	4.5	33	246.3	5.4	33	174.6	5.2	33	245.7	5.0	33	338.5	4.4	33	334.6	5.4
34	196.7	4.4	34	271.7	4.3	34	237.4	4.1	34	278.8	5.2	34	195.4	5.5	34	211.3	5.0	34	296.7	4.8	34	352.2	5.1
35	188.9	4.6	35	339.5	4.7	35	234.1	4.8	35	290.6	5.3	35	258.2	5.0	35	269.2	4.8	35	260.0	4.6	35	299.1	5.2
36	291.6	4.5	36	243.9	4.4	36	240.2	4.5	36	280.4	5.1	36	258.0	5.5	36	180.0	4.7	36	332.5	4.5	36	283.3	5.3
37	310.7	4.5	37	307.4	4.8	37	220.1	4.7	37	234.9	5.2	37	280.6	5.3	37	244.2	4.8	37	317.6	4.5	37	296.2	4.8
38	259.4	4.2	38	225.5	4.5	38	292.6	4.5	38	210.8	5.2	38	262.5	5.2	38	297.2	4.8	38	292.8	4.5	38	413.6	5.3
39	157.6	4.9	39	213.4	4.8	39	287.0	4.5	39	207.2	5.6	39	269.4	5.9	39	159.5	5.1	39	330.5	5.0	39	366.0	5.8
40	232.4	4.7	40	302.9	4.4	40	249.1	4.3	40	304.2	5.2	40	198.8	5.7	40	307.3	5.1	40	366.6	4.6	40	379.0	5.6
41	234.4	4.2	41	336.2	4.0	41	239.2	3.9	41	274.8	4.3	41	199.0	4.7	41	260.0	4.5	41	307.9	4.2	41	317.4	4.9
42	258.6	4.3	42	254.2	4.5	42	213.0	4.4	42	274.2	4.6	42	224.0	4.6	42	229.6	4.5	42	289.9	4.5	42	421.7	5.3
43	319.6	4.3	43	196.6	4.1	43	307.8	4.0	43	260.4	4.1	43	222.6	4.7	43	316.0	4.2	43	312.3	4.0	43	308.5	4.7
44	293.9	4.7	44	258.0	4.2	44	251.8	4.3	44	331.2	4.9	44	309.6	4.8	44	179.6	4.4	44	356.6	4.5	44	222.9	5.0
45	270.6	4.2	45	286.0	4.0	45	221.8	4.1	45	148.9	4.5	45	298.1	4.4	45	228.6	4.3	45	314.7	4.1	45	307.4	4.7
46	237.1	4.7	46	187.8	4.3	46	349.4	4.2	46	234.8	4.7	46	279.7	4.7	46	227.4	4.6	46	366.6	4.1	46	333.6	5.2
47	367.7	4.6	47	309.6	4.0	47	259.7	4.0	47	265.9	4.5	47	233.4	4.7	47	264.4	4.5	47	338.6	3.9	47	252.2	4.8
48	137.8	4.3	48	241.3	4.4	48	216.5	4.5	48	303.8	4.7	48	229.9	4.5	48	293.5	4.6	48	273.5	4.0	48	285.2	5.1
49	324.6	4.3	49	308.7	3.9	49	295.1	4.3	49	251.1	4.3	49	211.3	4.6	49	302.8	4.3	49	312.0	4.0	49	343.9	4.7
50	236.2	4.4	50	229.4	4.2	50	323.7	4.4	50	271.3	4.8	50	186.2	4.7	50	248.9	4.3	50	368.7	4.2	50	368.2	5.1
51	260.6	4.4	51	261.6	4.3	51	253.7	4.2	51	260.9	4.2	51	238.7	4.7	51	251.6	4.4	51	310.8	4.1	51	328.3	4.9
52	194.1	4.7	52	264.2	4.5	52	317.3	4.3	52	275.0	4.9	52	257.3	4.6	52	250.6	4.5	52	219.0	4.3	52	328.1	5.1
53 f	345.6	1.6	53 f	332.1	1.6	53 f	224.1	1.7	53 f	247.2	1.7	53 f	221.4	1.6	53 f	183.2	1.5	53 f	308.1	1.4	53 f	350.5	1.5
54	278.7	4.3	54	279.5	4.2	54	242.0	4.0	54	322.9	4.1	54	218.6	4.5	54	277.4	4.1	54	238.9	4.0	54	359.8	5.0
55	255.5	4.9	55	280.6	4.3	55	235.2	4.5	55	226.9	4.6	55	184.2	4.8	55	242.8	4.5	55	251.1	4.2	55	252.2	5.0
56	192.1	4.5	56	253.2	4.1	56	246.4	4.2	56	268.1	4.1	56	149.2	4.6	56	180.9	4.5	56	350.1	4.2	56	307.3	4.9
57	220.3	4.7	57	262.7	4.4	57	302.9	4.6	57	257.2	4.7	57	261.1	5.0	57	236.6	4.5	57	263.3	4.4	57	327.0	5.1
58	273.1	4.4	58	329.4	4.1	58	246.6	4.0	58	219.7	4.3	58	287.2	4.2									

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	333.6	9.8	1 r	400.9	10.8	1 r	366.2	11.0	1 r	305.2	11.5	1 r	417.4	7.3	1 r	356.0	7.2	1 r	443.6	6.2	1 r	464.2	7.9
2 r	250.1	0.7	2 r	250.3	0.7	2 r	249.8	0.7	2 r	250.3	0.7	2 r	250.2	0.7	2 r	250.2	0.7	2 r	250.2	0.6	2 r	249.8	0.6
3	250.6	5.1	3	250.8	5.0	3	250.2	5.0	3	248.6	6.1	3	249.9	5.7	3	249.8	5.1	3	249.0	5.0	3	248.8	5.5
4	249.1	4.4	4	249.2	4.6	4	248.5	4.3	4	249.4	5.8	4	250.1	5.7	4	250.6	4.8	4	249.1	4.5	4	249.9	4.8
5	250.5	5.0	5	250.3	4.7	5	248.0	4.8	5	249.6	5.9	5	251.4	5.6	5	250.2	5.1	5	248.4	4.6	5	249.2	5.2
6	248.2	4.5	6	250.0	4.3	6	251.0	4.4	6	250.0	5.1	6	250.0	5.6	6	249.8	4.7	6	250.8	4.3	6	250.2	5.0
7	249.0	4.8	7	250.4	4.9	7	249.4	4.8	7	249.6	5.7	7	250.5	5.3	7	250.0	4.6	7	249.0	4.6	7	249.7	5.1
8	249.9	4.4	8	251.4	4.4	8	248.5	4.3	8	249.4	5.4	8	249.6	5.7	8	249.3	4.6	8	250.4	4.3	8	250.7	5.1
9	249.9	4.9	9	250.4	5.0	9	249.5	4.6	9	249.8	5.7	9	250.3	5.4	9	250.5	4.6	9	250.7	4.5	9	250.4	5.1
10	248.8	4.3	10	250.3	4.3	10	249.7	4.2	10	250.1	5.1	10	250.1	5.5	10	250.3	4.6	10	249.9	4.5	10	249.4	5.0
11	248.9	4.5	11	249.7	5.0	11	248.9	4.8	11	249.3	5.5	11	250.5	5.2	11	250.0	4.7	11	250.4	4.8	11	250.6	5.0
12	249.7	4.4	12	249.2	4.3	12	249.7	4.1	12	251.0	5.0	12	248.6	5.6	12	249.8	4.6	12	250.5	4.4	12	250.9	4.9
13	249.0	4.8	13	250.3	4.6	13	250.8	4.8	13	249.7	5.5	13	249.9	5.0	13	250.0	4.7	13	250.7	4.4	13	249.9	5.0
14	249.9	4.6	14	249.9	4.6	14	250.7	4.2	14	249.0	5.0	14	250.2	5.2	14	251.1	4.6	14	249.1	4.5	14	251.2	4.9
15 f	250.2	1.7	15 f	250.0	1.7	15 f	249.6	1.7	15 f	250.2	1.6	15 f	250.3	1.7	15 f	250.9	1.6	15 f	250.6	1.5	15 f	249.8	1.6
16	250.1	5.0	16	247.6	4.7	16	250.0	4.5	16	249.2	5.3	16	249.4	4.9	16	248.8	4.6	16	249.2	4.4	16	248.3	5.0
17	249.8	4.0	17	249.5	4.3	17	250.6	4.3	17	249.8	5.0	17	249.9	5.1	17	249.9	4.5	17	249.1	4.2	17	250.3	5.2
18	249.4	4.7	18	248.9	4.5	18	249.6	4.7	18	249.4	5.3	18	248.8	4.8	18	249.3	4.9	18	249.8	4.2	18	250.5	5.3
19	248.5	4.2	19	248.2	4.2	19	250.4	4.4	19	250.5	4.8	19	249.1	5.0	19	249.8	4.6	19	249.6	4.5	19	249.9	4.8
20	249.7	4.7	20	250.0	4.6	20	249.1	4.5	20	250.2	5.1	20	249.9	4.7	20	249.3	4.8	20	250.2	4.3	20	250.1	4.8
21	250.5	4.4	21	250.9	4.4	21	250.4	4.3	21	249.7	4.9	21	248.9	5.3	21	249.9	4.8	21	250.2	4.6	21	249.7	4.8
22	249.1	4.8	22	250.2	4.5	22	251.1	4.5	22	249.9	5.2	22	250.5	4.8	22	250.2	4.8	22	248.9	4.3	22	250.6	4.9
23	249.9	4.6	23	249.3	4.4	23	250.0	4.1	23	249.3	5.1	23	249.3	5.0	23	249.4	4.7	23	249.0	4.1	23	250.9	4.9
24	251.7	4.8	24	250.3	4.4	24	249.1	4.4	24	249.6	5.2	24	249.6	4.8	24	250.9	4.6	24	248.9	4.5	24	249.0	4.9
25	250.5	4.4	25	249.7	4.3	25	248.9	4.4	25	250.1	4.8	25	250.3	5.2	25	250.5	4.5	25	249.2	4.5	25	249.5	4.9
26	251.0	4.5	26	250.1	4.6	26	252.2	4.6	26	250.9	5.2	26	251.5	5.2	26	249.9	4.6	26	251.0	4.3	26	250.3	5.0
27	250.9	4.4	27	250.3	4.5	27	250.6	4.2	27	249.0	4.7	27	250.0	5.0	27	250.4	4.6	27	250.8	4.2	27	250.6	5.0
28 f	250.8	1.8	28 f	249.8	1.9	28 f	249.5	1.8	28 f	249.7	1.9	28 f	250.1	1.8	28 f	249.2	1.9	28 f	250.7	1.8	28 f	250.8	1.7
29	250.1	4.4	29	251.5	4.8	29	249.2	4.5	29	249.1	5.2	29	248.6	4.6	29	249.9	4.8	29	250.9	4.4	29	250.2	4.7
30	250.5	4.4	30	250.1	4.2	30	248.3	4.2	30	248.8	4.8	30	249.7	5.1	30	250.0	4.8	30	249.9	4.4	30	250.0	5.0
31	249.8	4.5	31	251.1	4.6	31	249.6	4.7	31	247.7	5.3	31	248.1	4.9	31	250.7	4.7	31	248.5	4.3	31	250.8	4.9
32	249.0	4.2	32	249.6	4.3	32	250.0	4.4	32	251.5	5.2	32	249.3	5.1	32	249.5	4.5	32	248.7	4.4	32	248.7	4.8
33	250.7	4.7	33	249.7	4.5	33	250.8	4.5	33	250.7	4.9	33	248.9	5.2	33	250.1	4.5	33	250.1	4.6	33	249.9	4.8
34	248.7	4.0	34	249.1	4.2	34	249.6	4.1	34	250.6	4.8	34	250.5	4.9	34	250.1	4.8	34	248.5	4.7	34	249.9	4.9
35	249.4	4.4	35	250.6	4.4	35	251.0	4.5	35	250.0	4.8	35	249.6	4.7	35	250.2	4.4	35	251.1	4.4	35	251.3	5.0
36	248.7	4.6	36	248.7	4.3	36	250.6	4.1	36	250.2	4.9	36	249.6	5.0	36	250.2	4.4	36	251.6	4.3	36	250.7	5.1
37	249.6	4.9	37	249.8	4.6	37	249.3	4.8	37	250.8	4.8	37	246.9	5.0	37	251.0	4.6	37	249.3	4.5	37	250.8	4.8
38	251.4	4.2	38	249.2	4.2	38	249.6	4.1	38	250.2	4.8	38	249.9	5.3	38	251.0	4.6	38	250.2	4.5	38	249.7	5.1
39	250.4	5.0	39	250.1	4.7	39	249.3	4.5	39	249.7	5.3	39	250.0	5.4	39	249.9	4.9	39	249.1	4.6	39	249.6	5.2
40	249.5	4.3	40	250.1	4.3	40	250.1	4.2	40	250.3	4.9	40	249.3	5.1	40	251.4	4.5	40	248.9	4.4	40	250.0	5.6
41	249.8	4.4	41	249.6	4.3	41	249.1	3.9	41	250.9	4.4	41	249.4	4.6	41	249.6	4.2	41	250.2	4.0	41	251.8	4.7
42	249.6	4.4	42	248.5	4.4	42	250.4	4.2	42	250.4	4.5	42	251.1	4.9	42	249.1	4.4	42	250.1	4.4	42	248.9	5.1
43	248.6	4.3	43	250.3	4.0	43	251.0	4.4	43	250.5	4.3	43	250.0	4.3	43	251.1	4.2	43	249.7	4.0	43	250.7	4.8
44	248.9	4.5	44	250.3	4.2	44	250.8	4.2	44	250.5	4.7	44	249.8	4.5	44	250.1	4.5	44	249.0	4.4	44	249.3	5.1
45	250.2	4.3	45	250.3	4.0	45	249.7	4.0	45	249.3	4.2	45	250.3	4.2	45	249.8	4.2	45	248.4	3.9	45	251.3	4.7
46	249.1	4.3	46	250.2	4.3	46	250.5	4.4	46	250.1	4.6	46	250.6	4.6	46	250.0	4.5	46	249.4	4.2	46	249.8	5.1
47	248.1	4.3	47	249.5	3.9	47	248.7	3.9	47	249.5	4.3	47	250.8	4.4	47	250.0	4.5	47	249.9	4.2	47	251.1	4.8
48	250.0	4.3	48	251.0	4.4	48	250.0	4.3	48	248.2	4.6	48	249.8	4.6	48	251.2	4.3	48	249.4	4.2	48	249.7	5.3
49	249.8	4.4	49	250.4	4.2	49	250.3	4.2	49	248.8	4.3	49	250.7	4.4	49	250.4	4.1	49	250.2	4.0	49	250.9	4.6
50	250.4	4.4	50	251.4	4.5	50	248.9	4.4	50	250.1	4.7	50	248.9	4.7	50	250.6	4.5	50	249.4	4.2	50	250.8	5.4
51	249.1	4.3	51	249.7	4.5	51	249.9	4.0	51	250.1	4.5	51	248.1	4.4	51	247.9	4.2	51	249.5	3.8	51	250.2	4.8
52	250.5	4.5	52	249.6	4.2	52	248.5	4.3	52	250.5	4.7	52	251.5	4.5	52	250.5	4.5	52	250.0	4.5	52	251.5	5.1
53 f	249.8	1.6	53 f	250.2	1.7	53 f	250.0	1.8	53 f	250.7	1.6	53 f	250.7	1.6	53 f	250.8	1.5	53 f	250.1	1.6	53 f	249.5	1.5
54	249.1	4.3	54	251.0	4.1	54	249.8	4.1	54	249.9	4.3	54	249.3	4.4	54	249.9	4.5	54	251.2	4.0	54	248.0	4.5
55	249.8	4.7	55	250.0	4.3	55	252.1	4.4	55	250.0	4.5	55	249.5	4.5	55	251.3	4.6	55	250.5	4.4	55	249.5	5.6
56	249.2	4.4	56	249.7	4.0	56	250.3	4.0	56	250.0	4.2	56	249.6	4.4	56	249.1	4.1	56	249.3	4.1	56	250.2	4.7
57	249.0	4.7	57	249.3	4.7	57	249.2	4.4	57	249.7	4.9	57	248.6	4.6	57	248.9	4.6	57	250.0	4.7	57	250.6	5.3
58	248.4	4.3	58	249.6	4.2	58	249.7	4.0	58	250.0	4.4												