OMEGA ROC ASICs : Integrated Readout Electonics for Gazeous detectors

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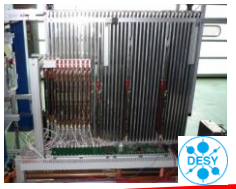
OMEGA microelectronics
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr
& WEEROC SAS
http://weeroc.com

Organization for Micro-Electronics desiGn and Applications

OMEGA ASICs : manufactured & used ASICs

Omega



2006

SKIROC

SPIROC

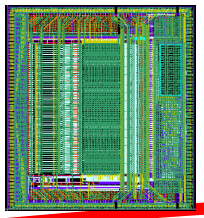
MAROC3

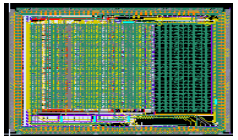
HARDROC

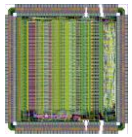
MICROROC

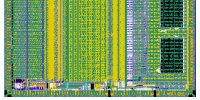
SPACIROC

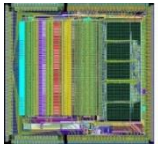
PETIROC

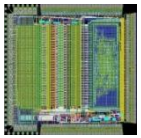












AMS
350nm
SiGe

TSMC
130nm

TRIROC

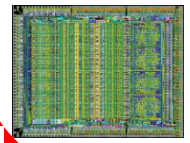
CITIROC

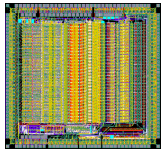
CATIROC

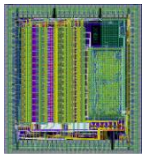
SKIROC2_CMS

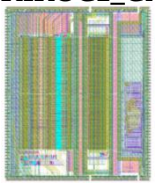
ALTIROC

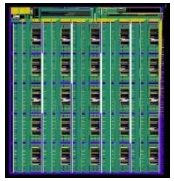
HGCROC

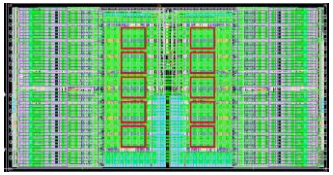




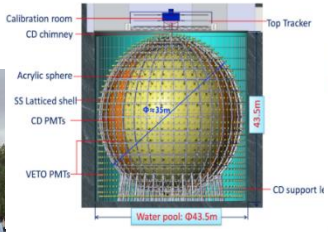


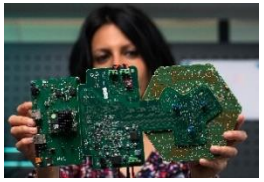






2021

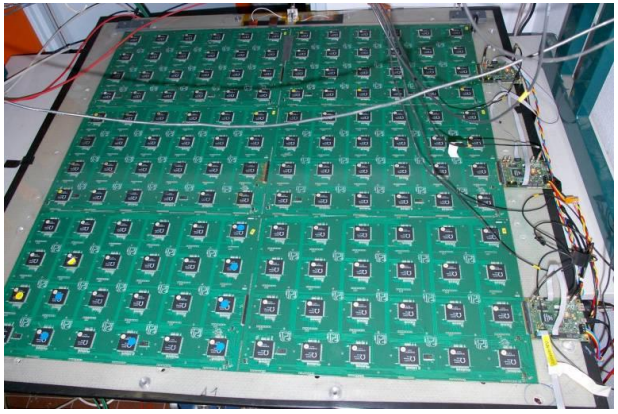


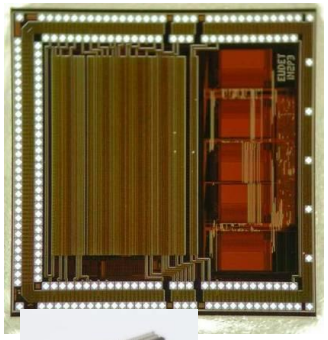


HARDROC2 for RPC readout

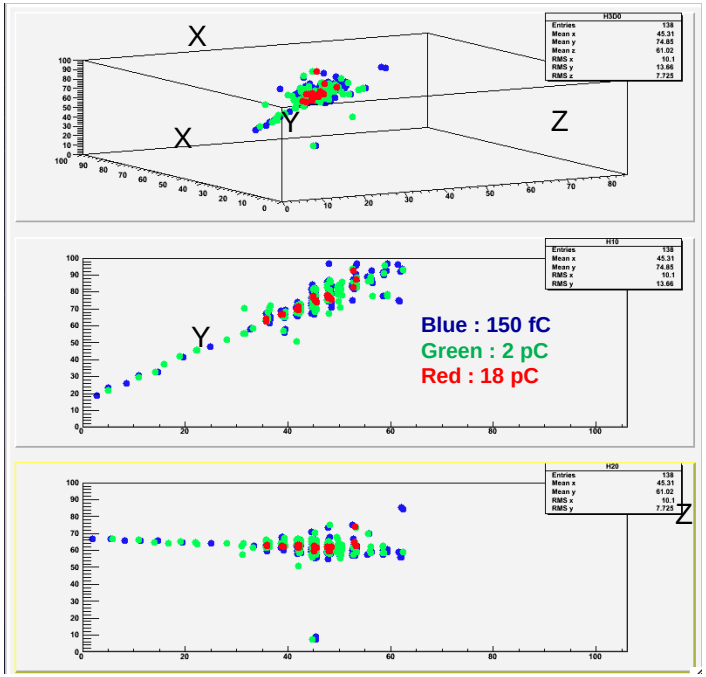
1 m³ RPC detector, 40 layers
370 000 channels

- **HARDROC2: 64 channels (RPC DHCAL)**
  - preamp + shaper+ 3 discri (semi digital readout)
  - Auto trigger on 10fC up to 20 pC
  - five 0.5 Kbytes memories to store 127 events
  - Full power pulsing => 7.5 µW/ch
  - Fully integrated ILC sequential readout
  - 10 000 chips produced to equip 400 000 ch
  - SDHCAL technological proto with 40 layers (5760 HR2 chips) built in 2010-2011.
    - Successful TB in 2012 : 40 layers in AutoTrigger with Power Pulsing mode
      - High Granularity (PAD size : 1 cm x 1 cm)



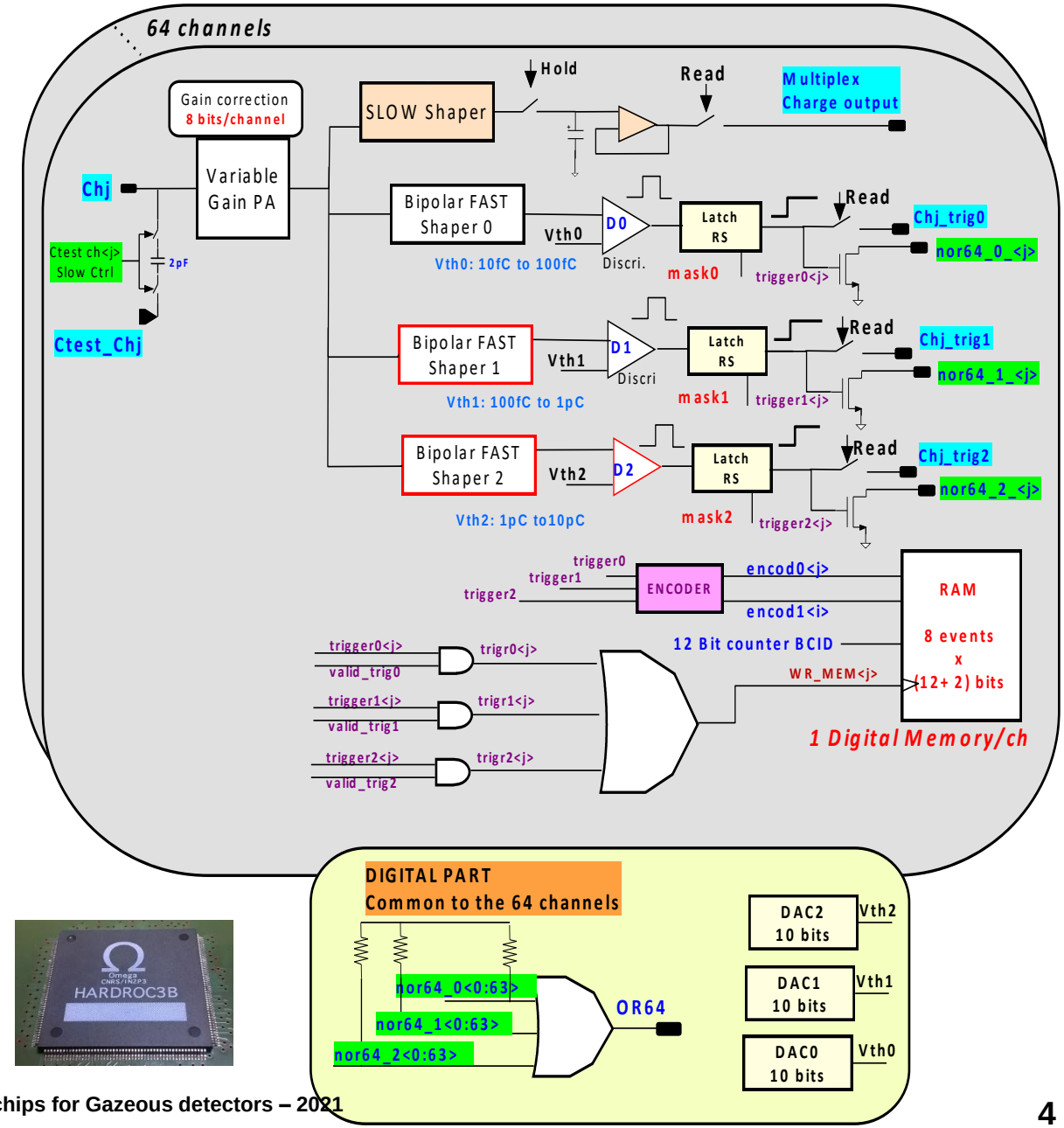


Cosmic hadronic shower



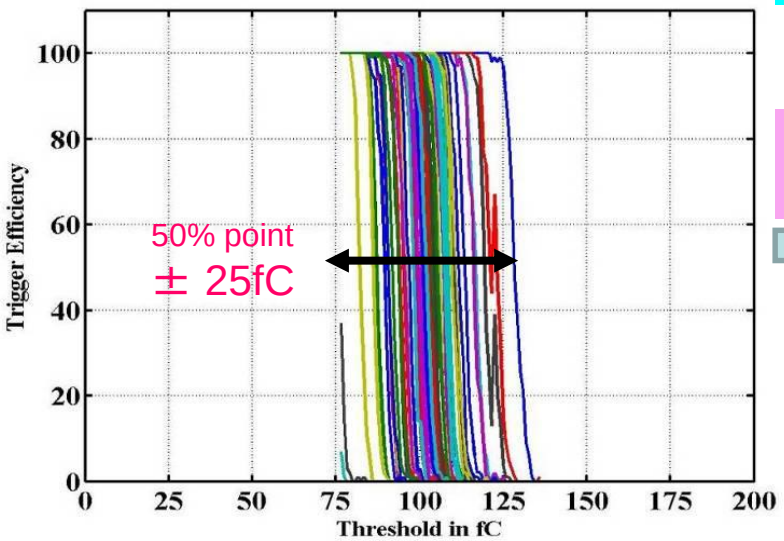
HARDROC3: Simplified schematics

- 64 channels with current preamplifiers
- Trigger less mode (auto trigger 15fC up to 50pC)
- Gain correction (max factor 2)
- 3 shapers + 3 discriminators (encoded in 2 bits for readout)
- I2C link with triple voting for Slow Control Parameters
- 64 Independent channels with zero suppress
- Max 8 events / channel with 12-b time stamping
- Integrated clock generator: PLL
- All bias and reference voltage internal (with power pulsing)
  - No decoupling capacitances required on bias and references voltages
- Token Ring ReadOut

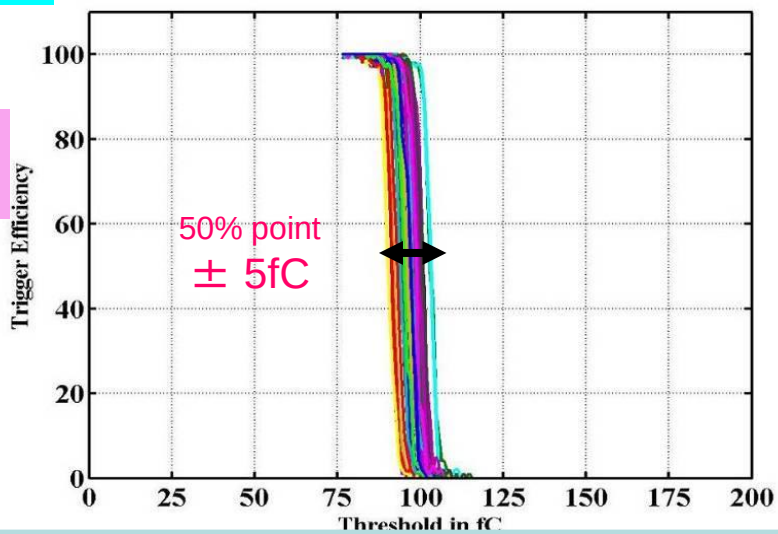


Gain correction / Scurves

Qinj=100fC

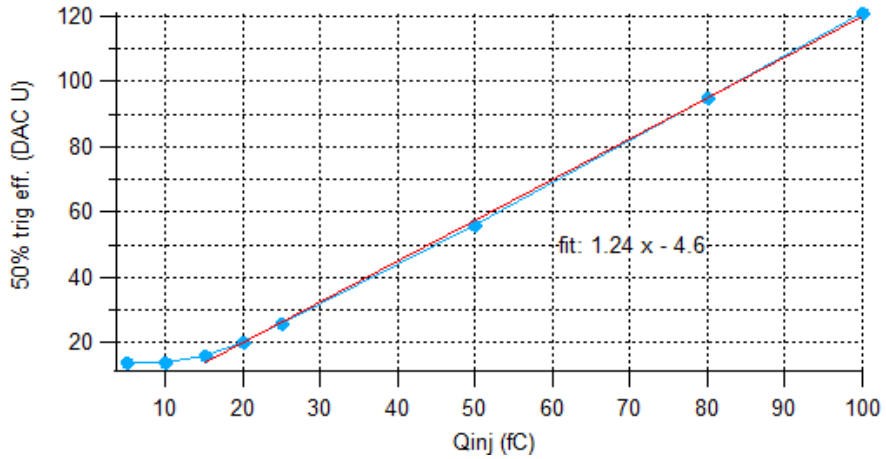


HR2 gain correction



HR3

50% trig. Eff. (DAC units) vs Qinj (fC)



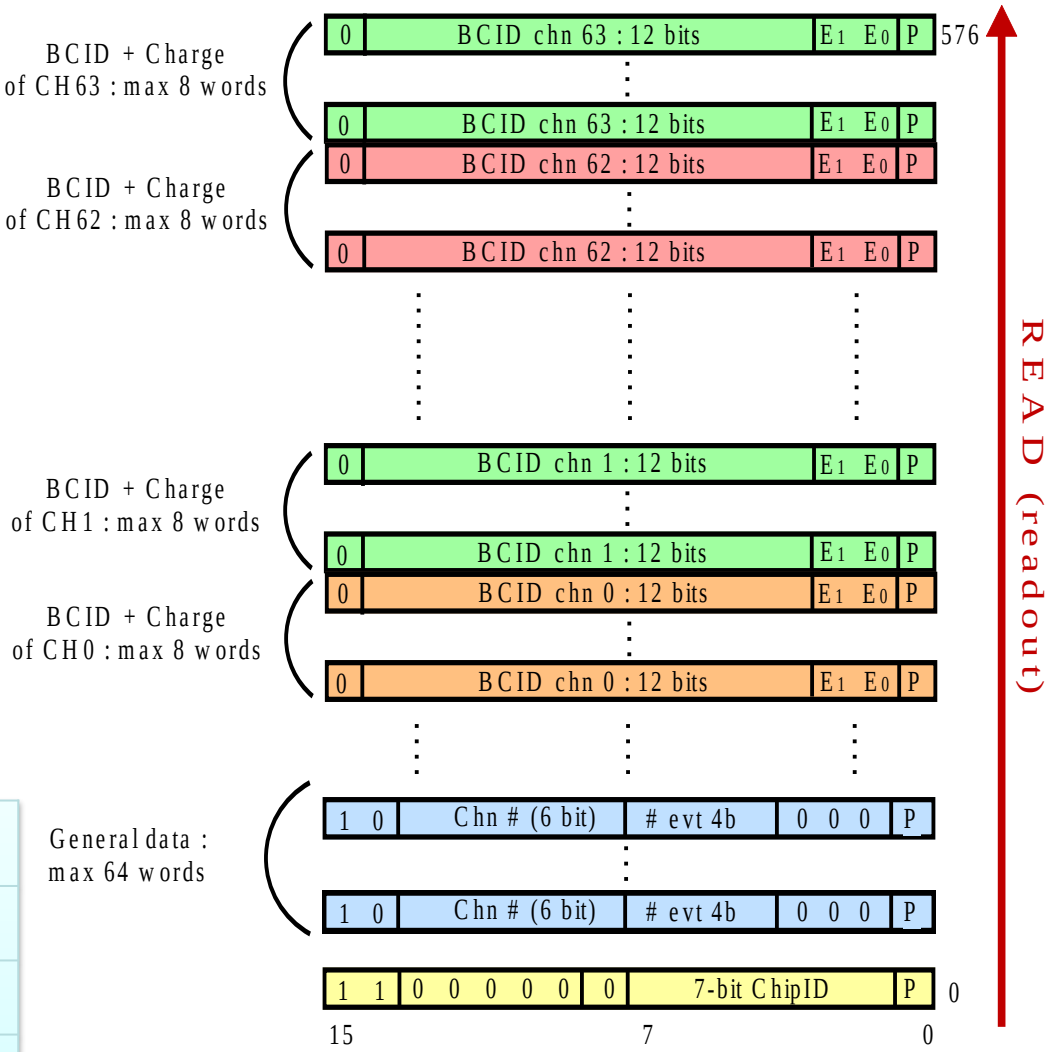
ASIC Dynamic range: 15fC - 50pC

FSB0: 5σ noise limit= 15fC

Zero suppress: Memory mapping

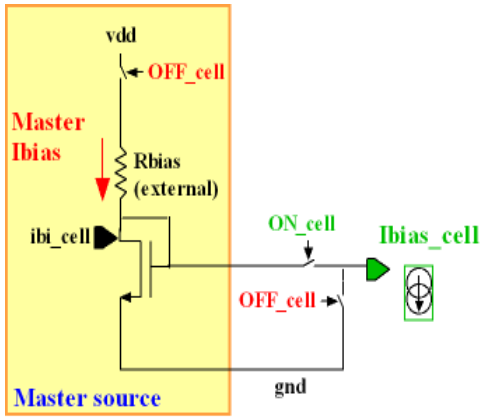
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch. number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



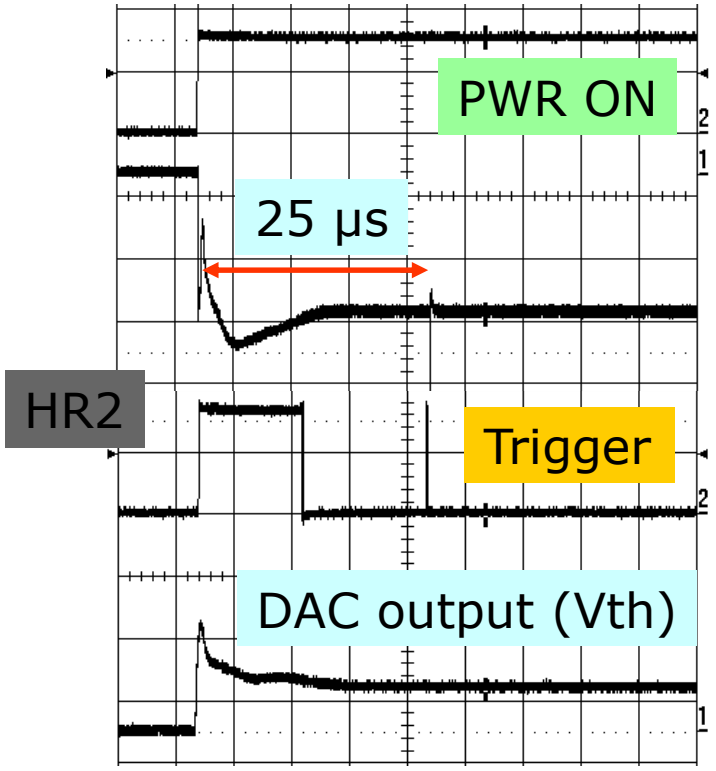
Power pulsing in HR chips

- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
  - No decoupling capacitance on bias and voltage references



- Compared to HR2, HR3 power consumption is higher due to:
  - The extended dynamic range (from 15pC to 50pC)
  - The integration of the zero suppress algorithm
- If the PLL is used, the power consumption is increased by 3% (due to the PLL VCO)

Power supply	HR3 with LVDS (5M + 40M) µW / channel	HR2 with LVDS (5M + 40M) µW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	**12,2**	**7,5**



MICROROC (GEMROC)

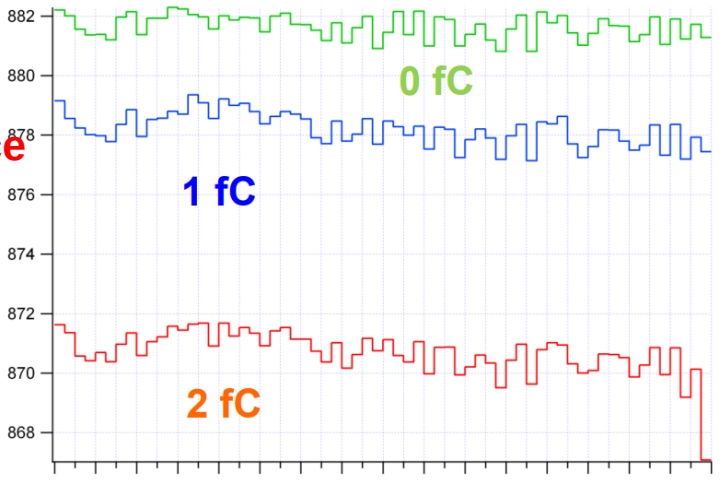
64 channels for µMegas (sDHCAL ILC)

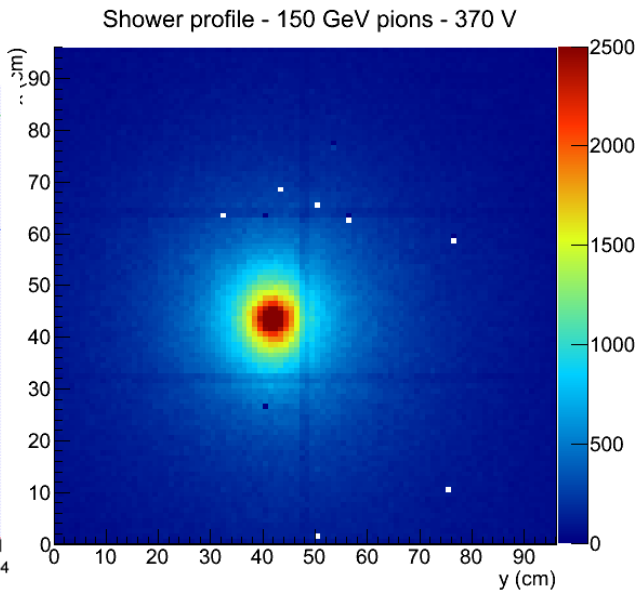
- Very similar to HARDROC except :
  - Input (charge) preamp
  - Slower shapers (100-150 ns)
  - HV Spark protections
- Noise: **0.2fC (Cd=80 pF). Auto trigger on 1fC** up to 500fC
- Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- 4 Micromegas prototypes of 1x1 m2 were constructed in 2011-2012 and tested in particle beams inside the DHCAL steel structure in 2012

1m² Micromegas detector
144 Microroc : 10 000 channels

Test Beam :

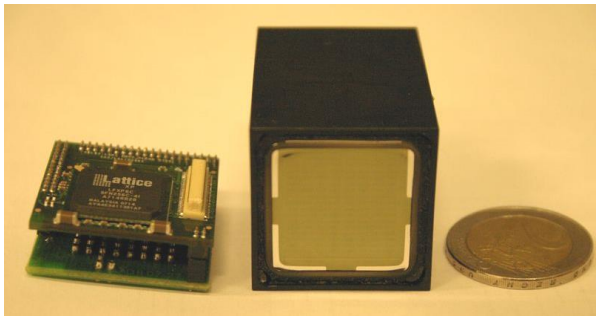
Very good performance of the electronics and detector (Threshold set to 1fC)

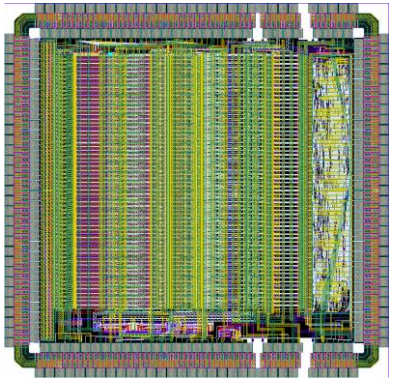


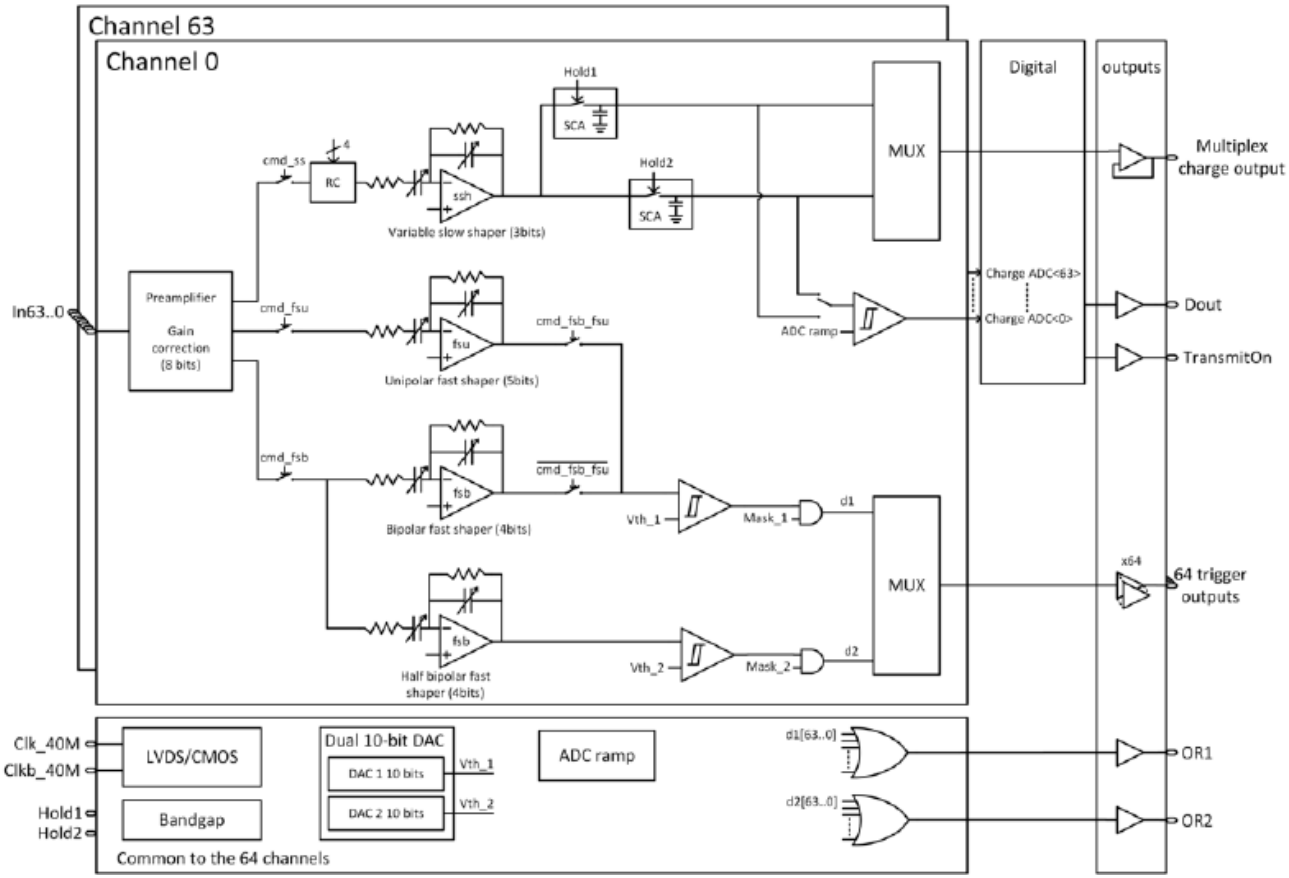


MAROC3 : MultiAnode Read-Out Chip

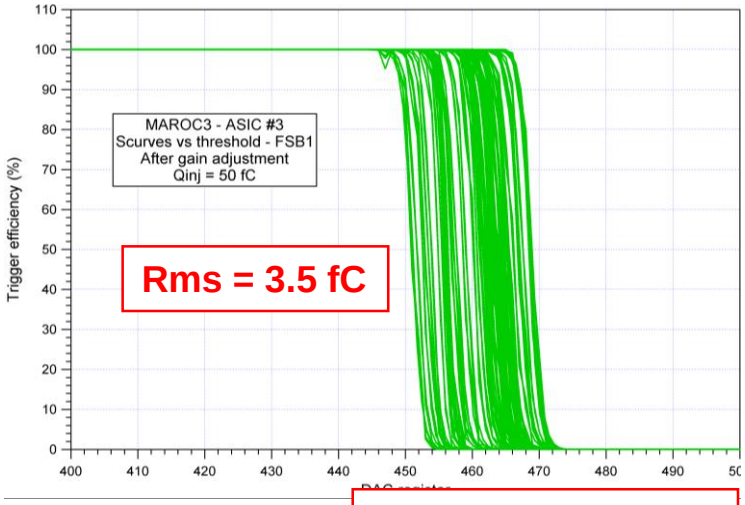
- Complete front-end chip for 64 channels multi-anode photomultipliers
  - 6bit-individual gain correction
  - Auto-trigger on 1/3 p.e. at 10 MHz
  - 12 bit charge output with internal ADC
  - SiGe 0.35 µm, 12 mm^2, Pd = 5 mW/ch



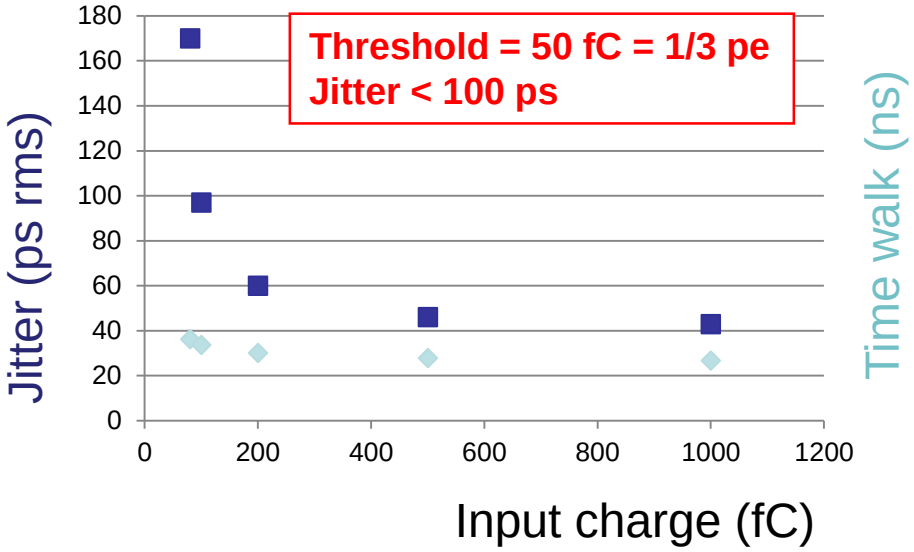


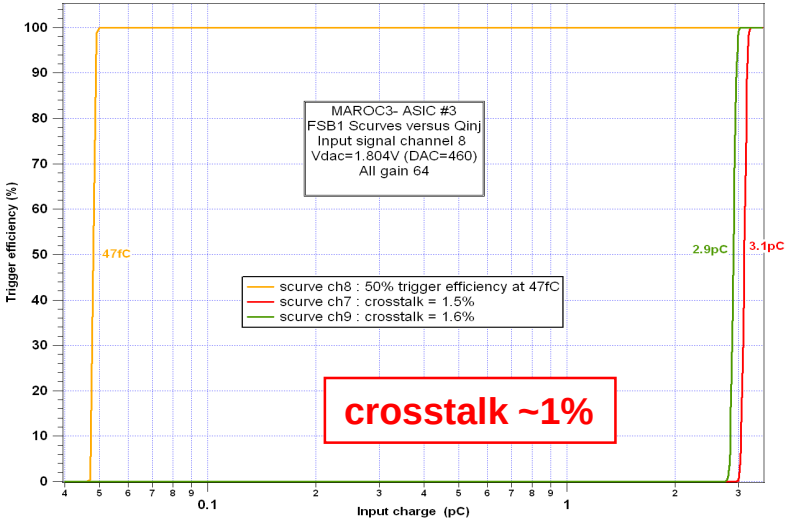


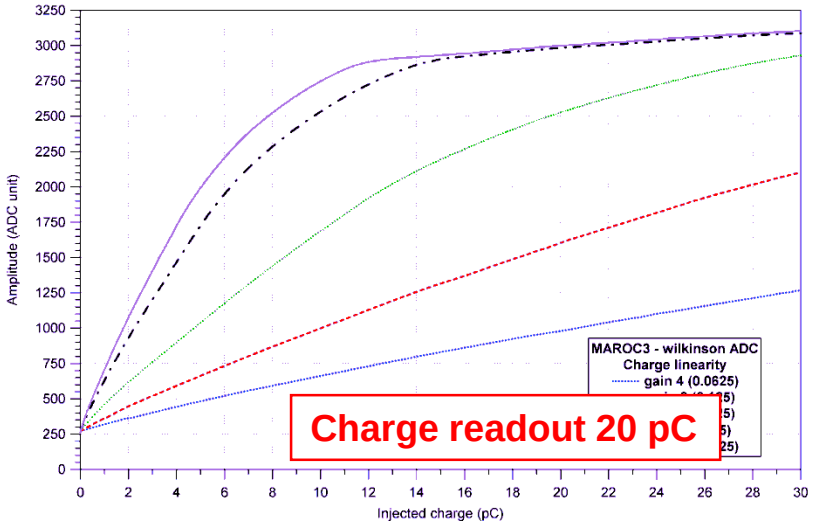
MAROC3 performance



Qin = 50 fC = 1/3 pe

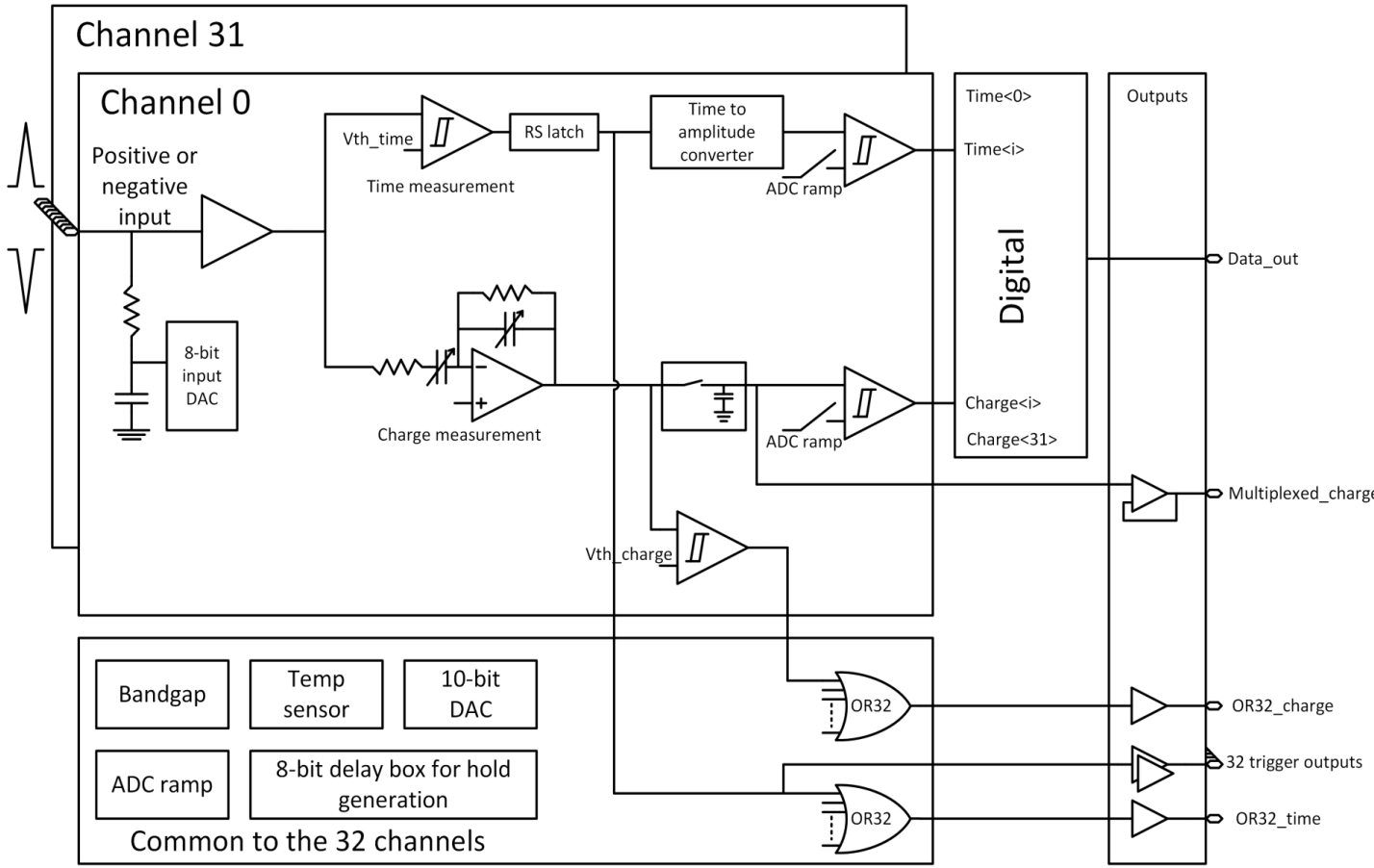


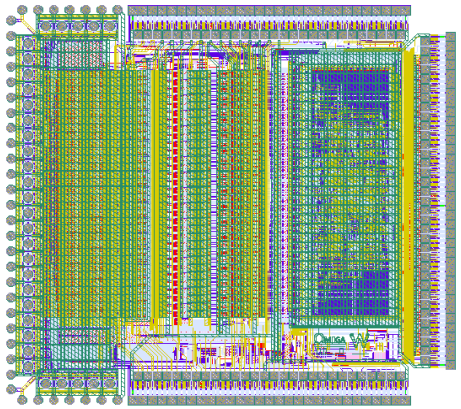




PETIROC2

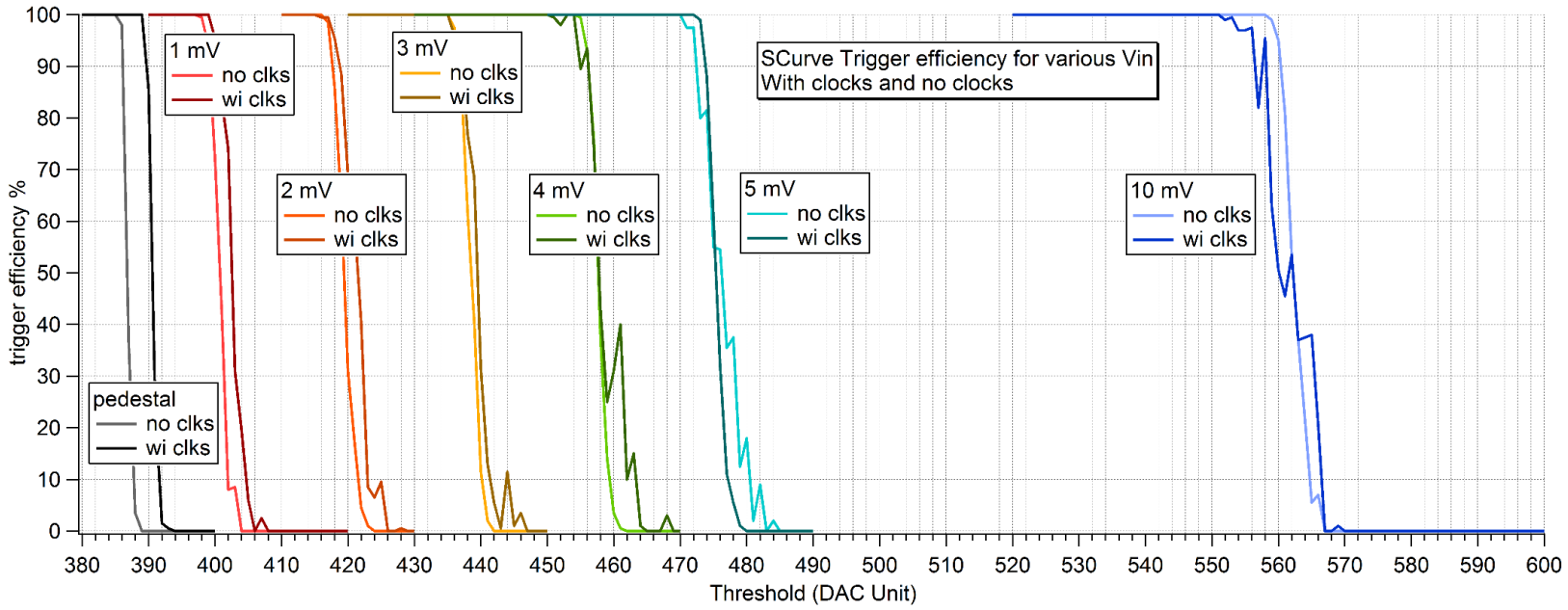
- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
- 32 trigger outputs and multiplexed data output
- Embedded 10-bit ADC and 50 ps TDC
- Dual threshold : first photons and energy

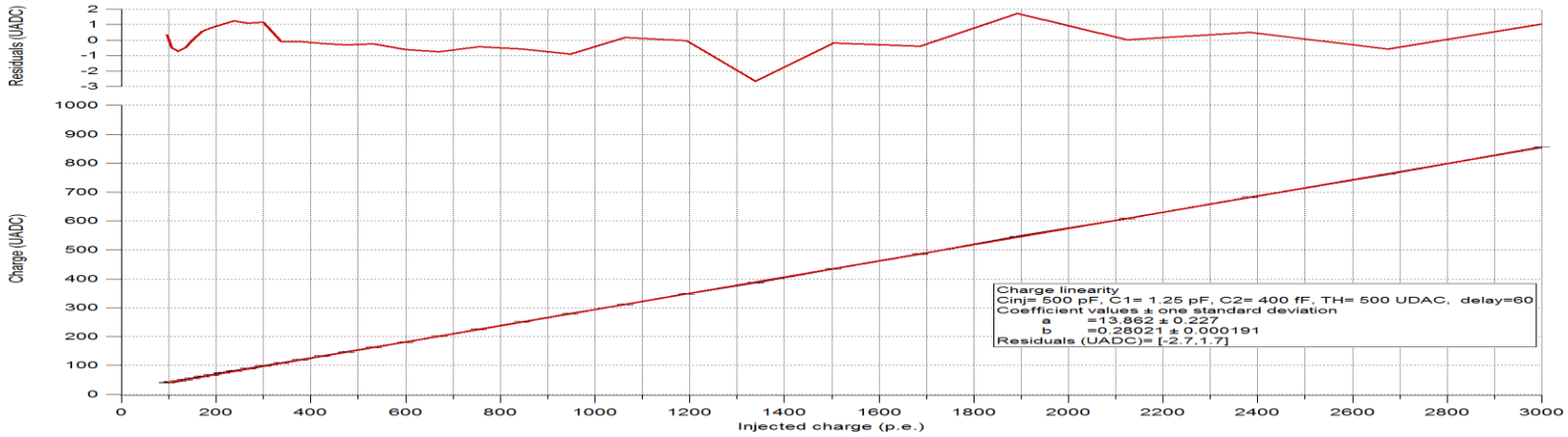




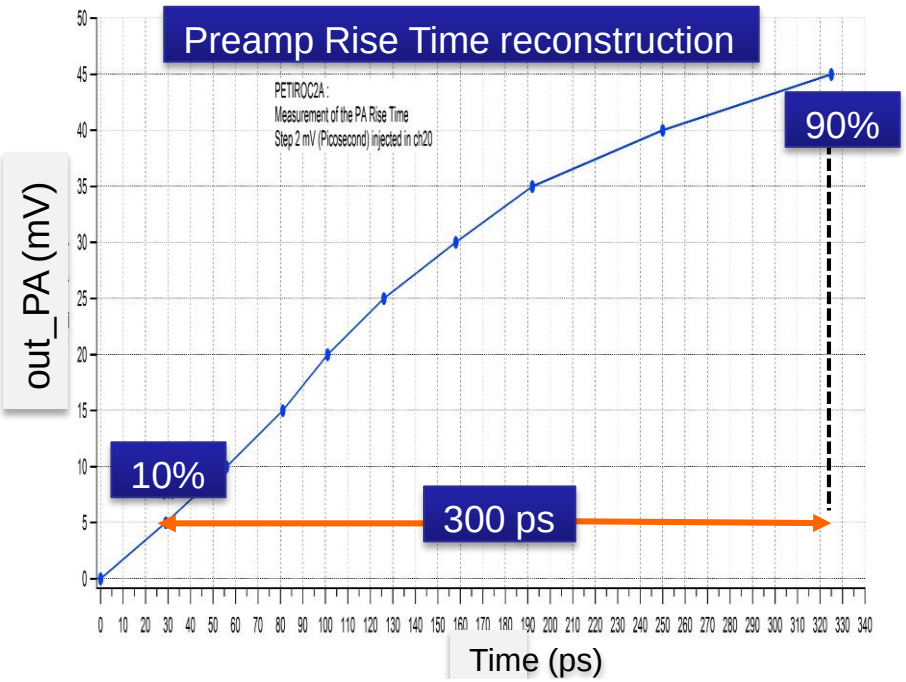
PETIROC2A : SCURVES with and w/o clock

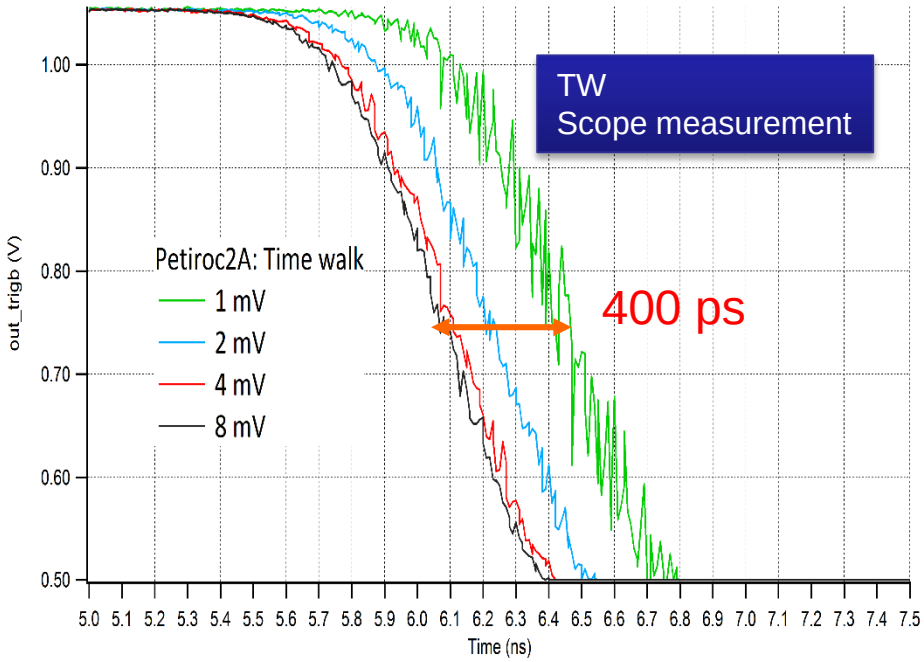
- Injection of a step (1mV, 2mV, 3mV, 4mV, 5mV and 10mV)

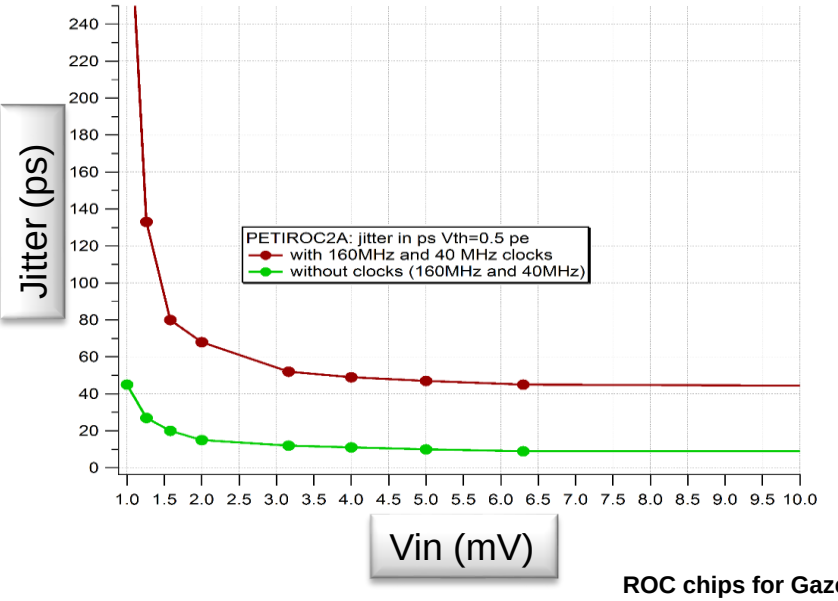


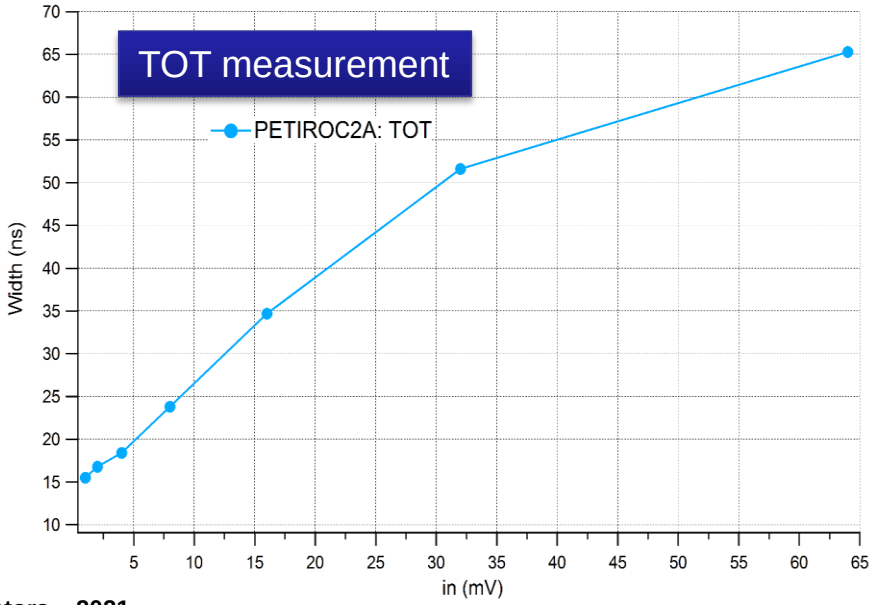


PETIROC2A: performance

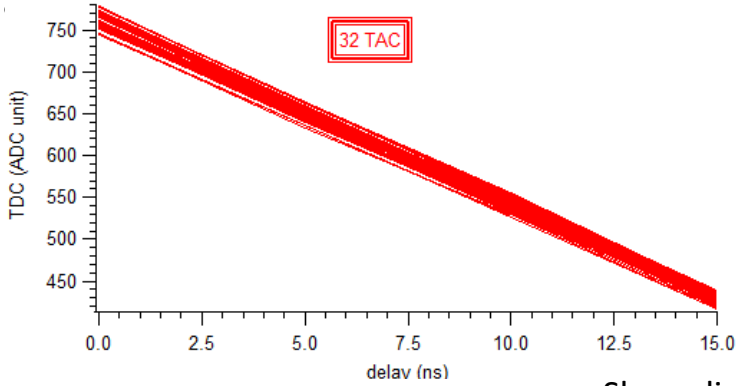




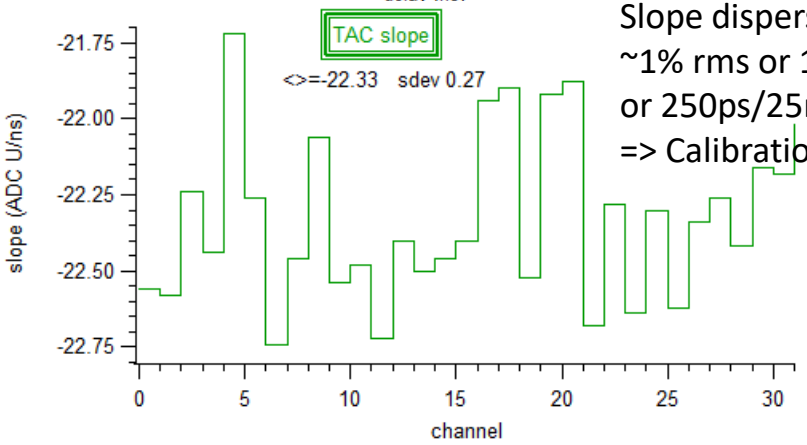




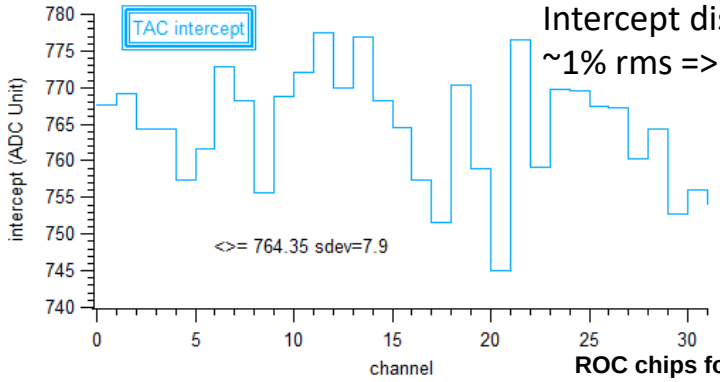
PETIROC2: TAC measurement



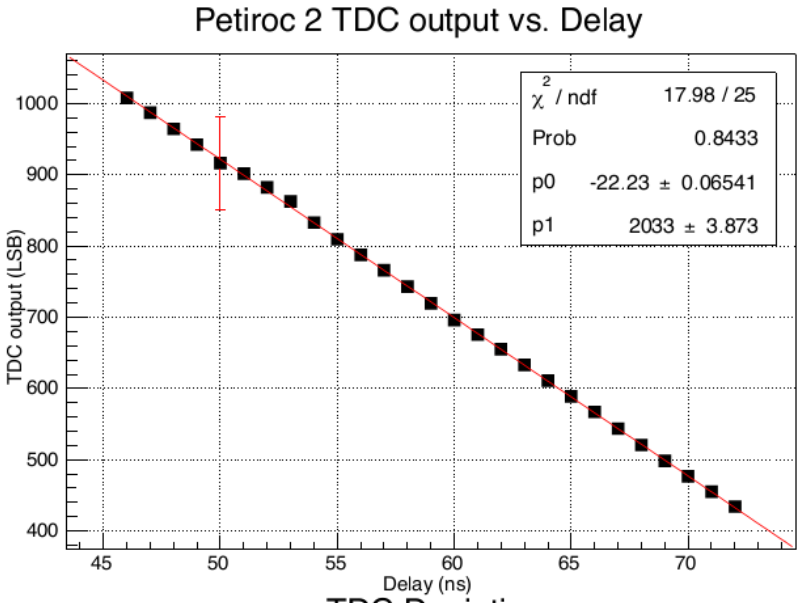
weeroc

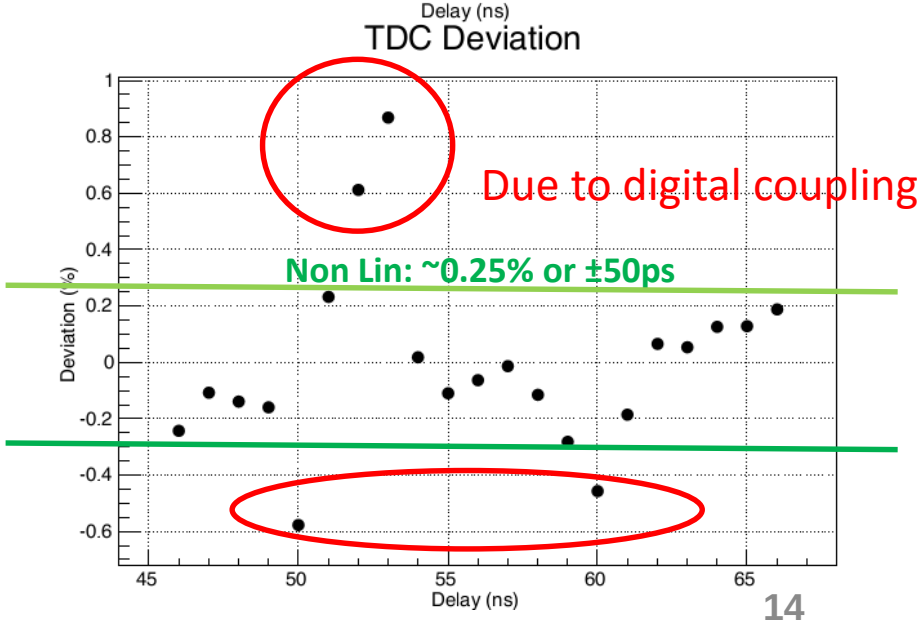


Slope dispersion:
~1% rms or 10ps/1ns
or 250ps/25ns
=> Calibration



Intercept dispersion:
~1% rms => Calibration



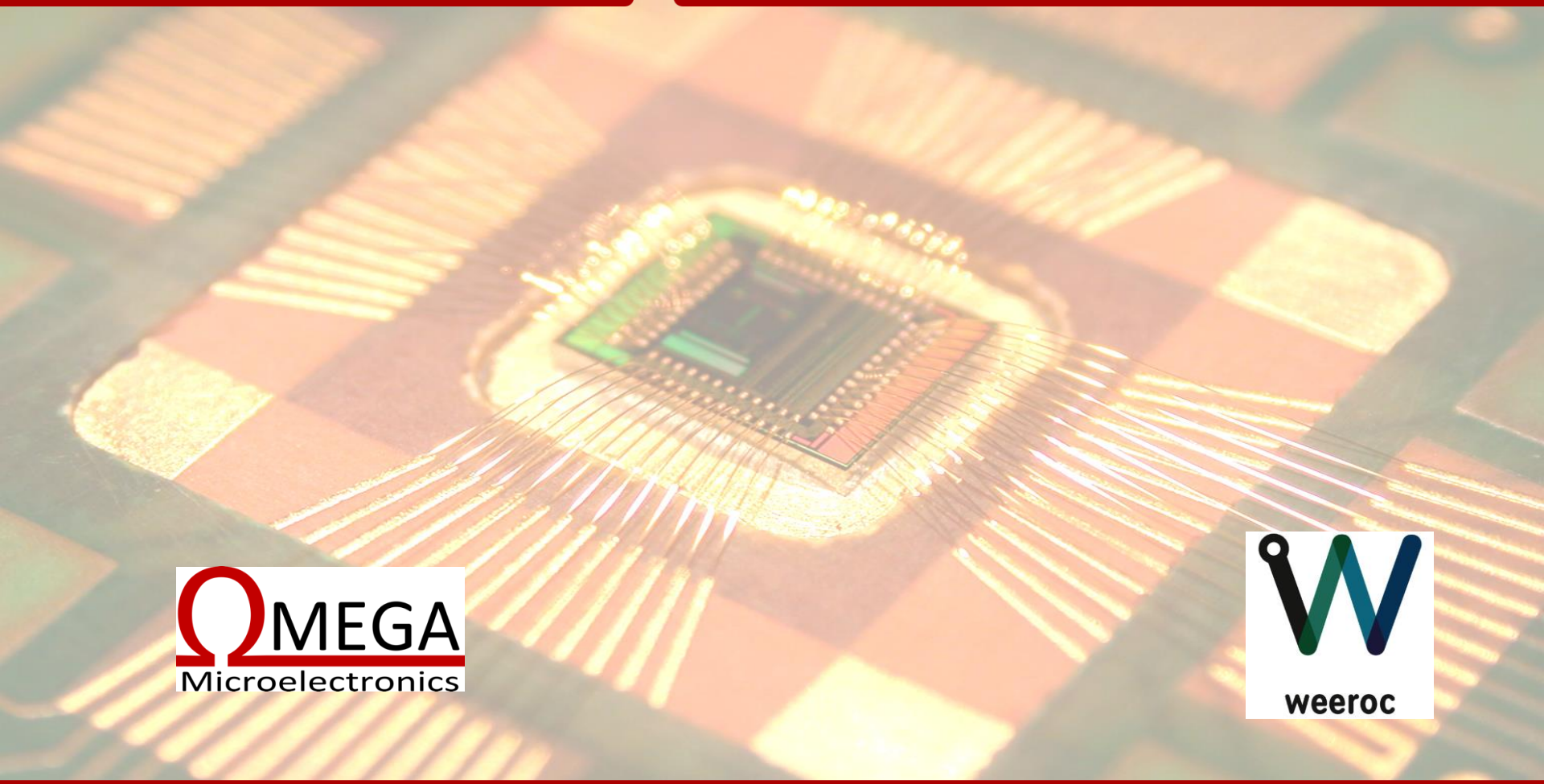


SUMMARY

http://omega.in2p3.fr/ http://www.weeroc.com/ Omega

Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	50 fC - 100 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

Omega



Organization for Micro-Electronics desiGn and Applications

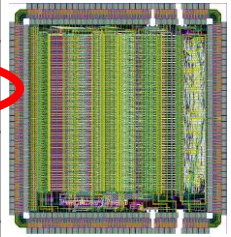
OMEGA ROC chips

- Use of Silicon Germanium AMS 0.35 µm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

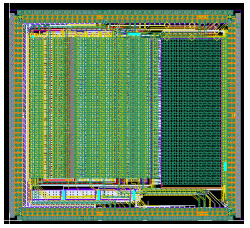
Chip	detector	ch	DR (C)
MAROC	PMT	64	-2f-50p
SPIROC	SiPM	36	10f 200p
SKIROC	Si	64	0.3f 10p
HARDROC	RPC	64	-2f-50p
PARISROC	PM	16	-5f-50p
SPACIROC	PMT	64	-5f-15p
EASI/CITIROC	SiPM	32	10f 200p
MICROROC	µMegas	64	-0.2f-0.5p
PETIROC	SiPM	32	50f 300p
TRIROC	SiPM	64	50f 300p

http://omega.in2p3.fr

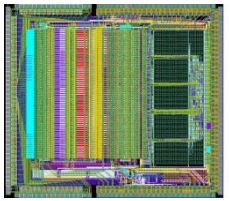
MAROC3



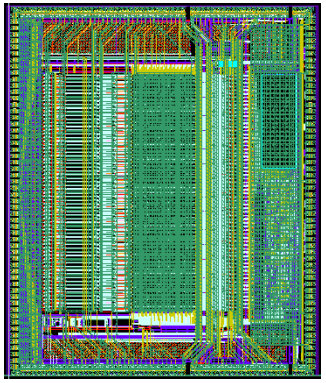
HARDROC2



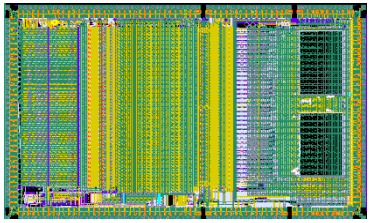
MICROROC1



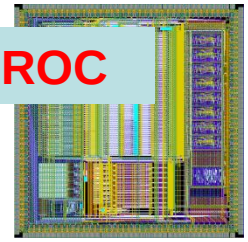
SKIROC2



SPIROC2

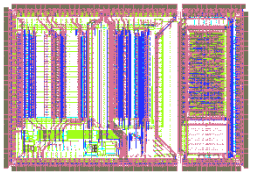


SPACIROC



GEMROC

PARISROC2



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Example of prices, prototyping

CNRS – INPG – UJF

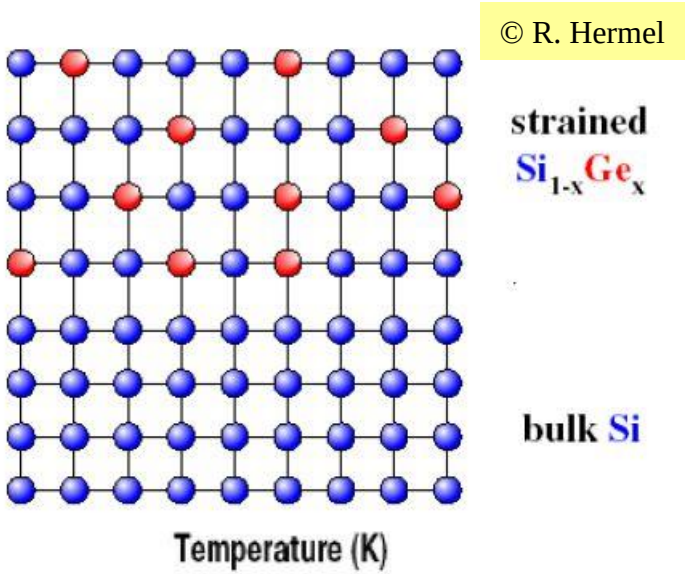
CMOS	.35 µ	AMS	650 €/mm²
CMOS opto	.35 µ	AMS	810 €/mm²
CMOS HV	.35 µ	AMS	1000 €/mm²
CMOS	130nm	ST	2200 €/mm²
CMOS	65 nm	ST	7500 €/mm²
CMOS	40 nm	ST	15000 €/mm²
SiGe BiCMOS	.35 µ	AMS	890 €/mm²
SiGe:C BiCMOS	130nm	ST	3500 €/mm²
SOI	130nm	ST	4000 €/mm²
SOI	65nm	ST	9500 €/mm²
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm²

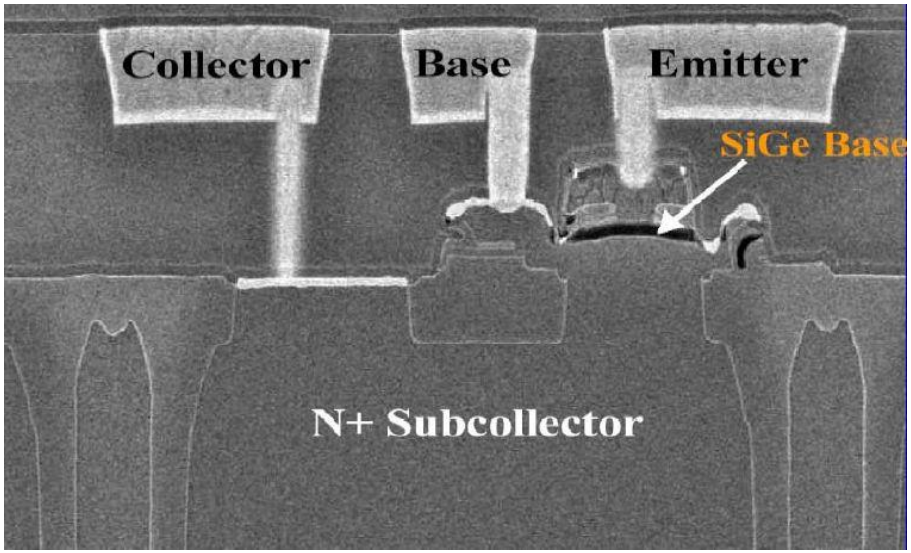
CMP annual users meeting, January 20th 2011, PARIS

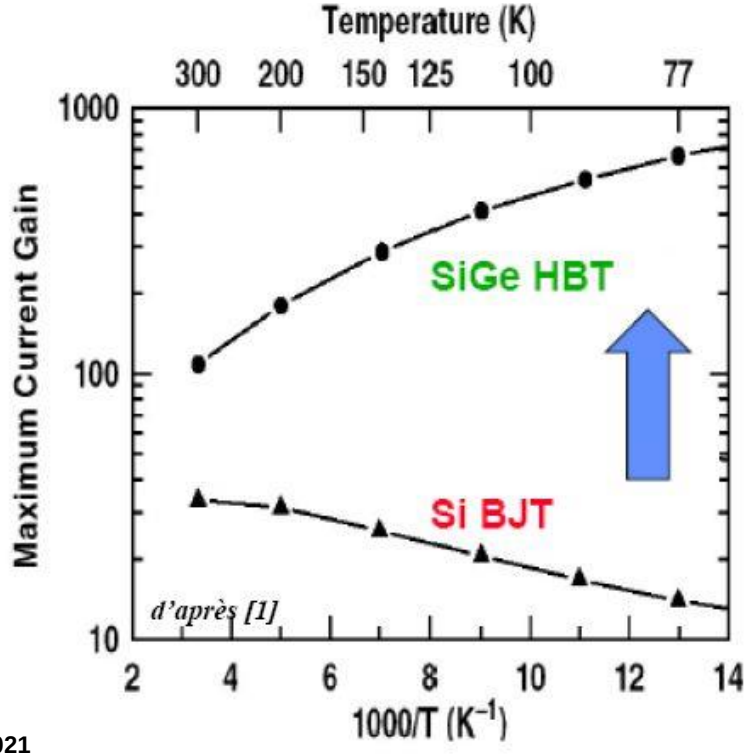
http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

SiGe technology

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-s

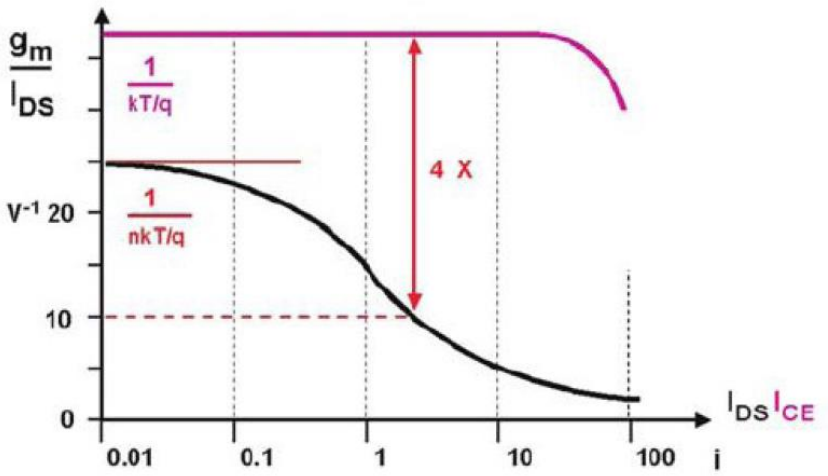


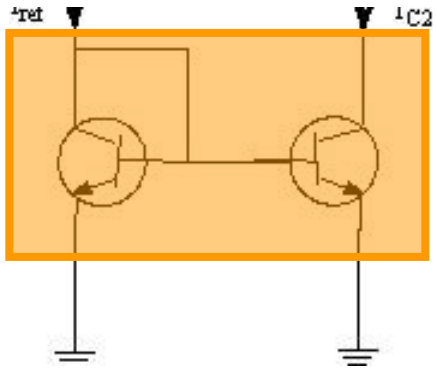


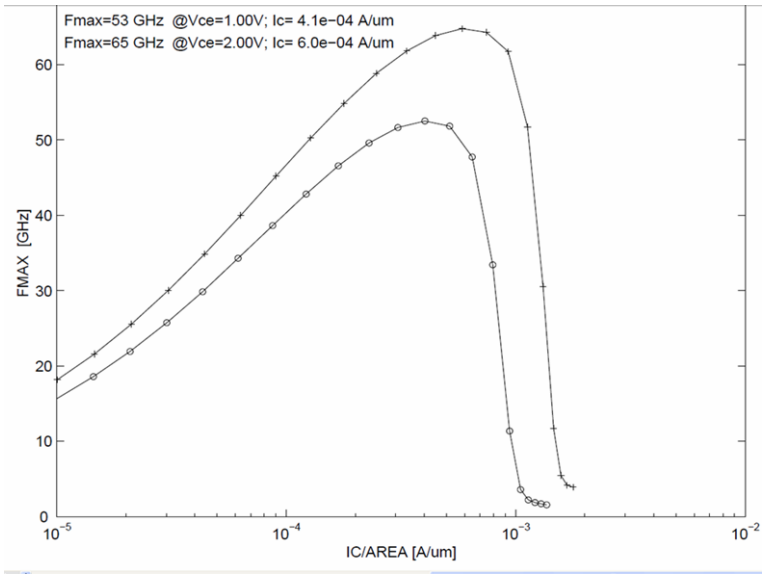


Power and speed with SiGe

- BJT : best g_m /I ratio $(1/U_T)$
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE}=V_T Ln(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T



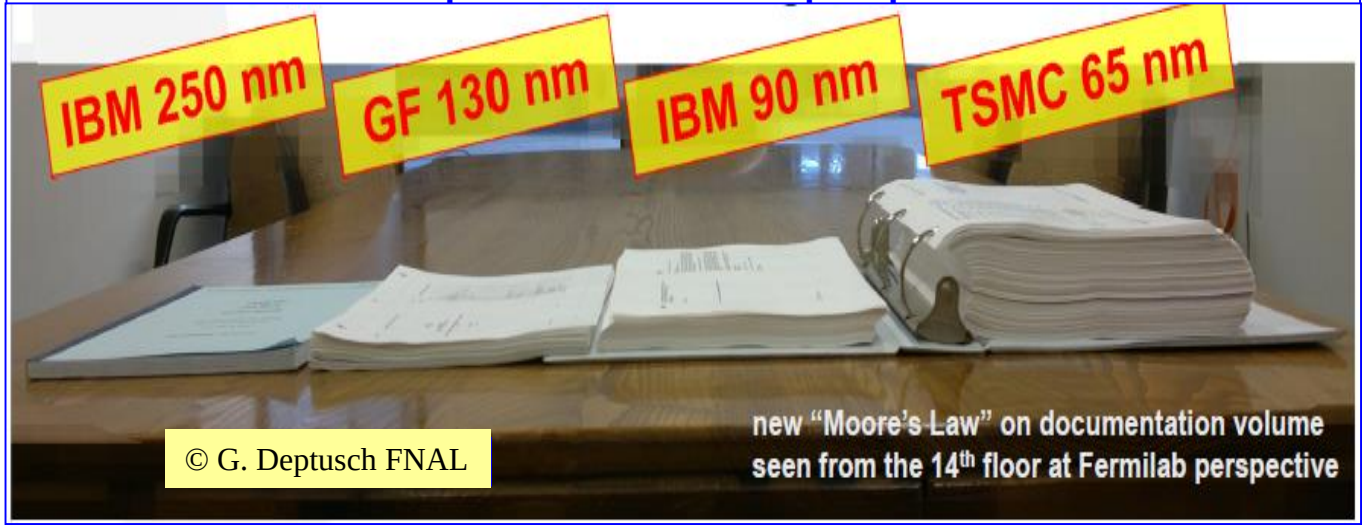




Evolution of technologies in practice

- Performant design is at transistor level
- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex

10 ans d'évolution des spécifications techniques pour la réalisation d' ASIC



Design Groups – Current Status

© G.L. de Geronimo (BNL) TIPP2014

design groups ≈ 30-40

active designs ≈ 30-40

... NOvA APV25 ... MAPS POM
3D FSSR2 ASDQ PACIFIC ICECAL
FE-I5 CBC LBNE VMM CLARO MAROC3
KPIX nEXO LAPAS ASDCDC SAMPA
BEAN QIE ABC ... SAO3 VELOPIX
CLIC TARGET ISR3B SALT ...

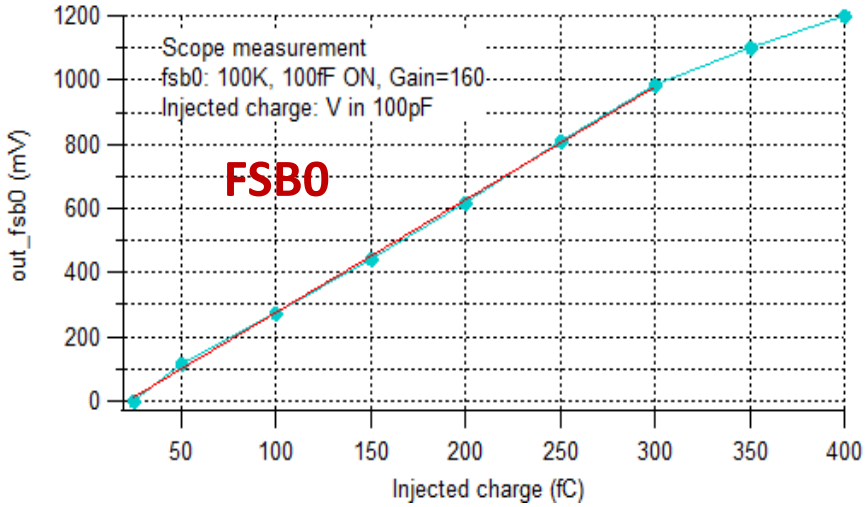
Average one design per group

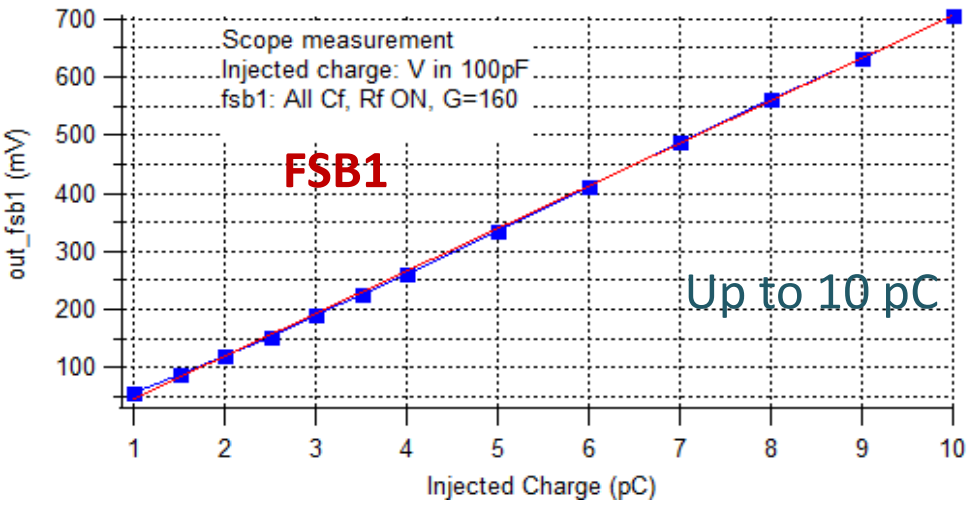
- institutions leading collaborative efforts
- institutions performing R&D on technologies

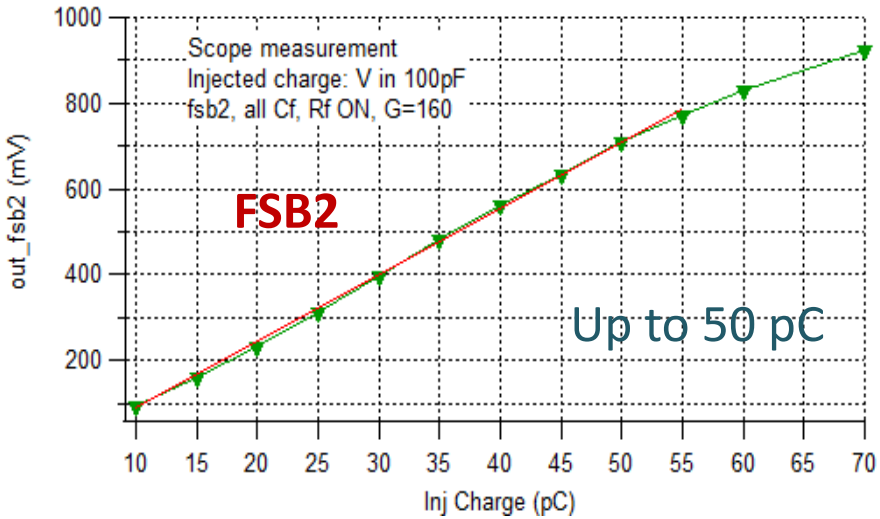
One FE-ASIC design currently requires
2-4 full-time designers and 2-4 years
average, from concept to ready-for-production

HR3: Analog linearity

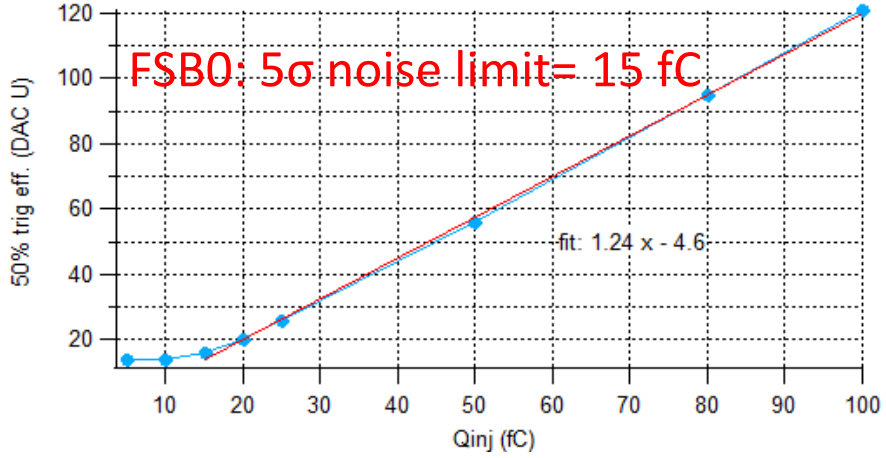
Fast shaper outputs (mV) vs Qinj (fC)







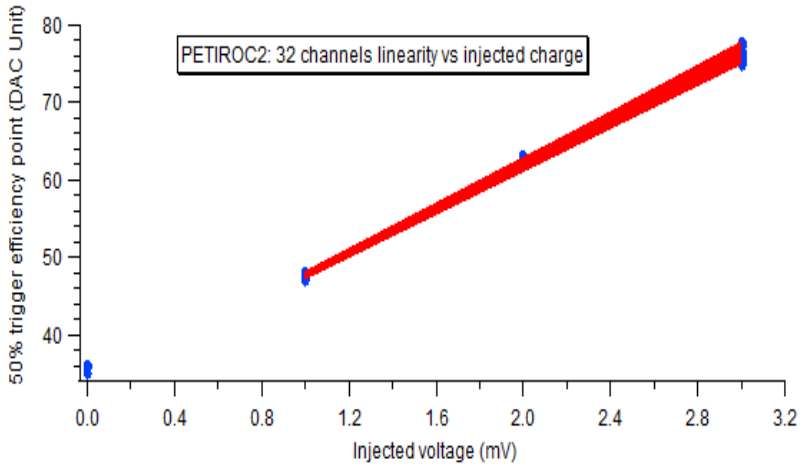
50% trig. Eff. (DAC units) vs Qinj (fC)

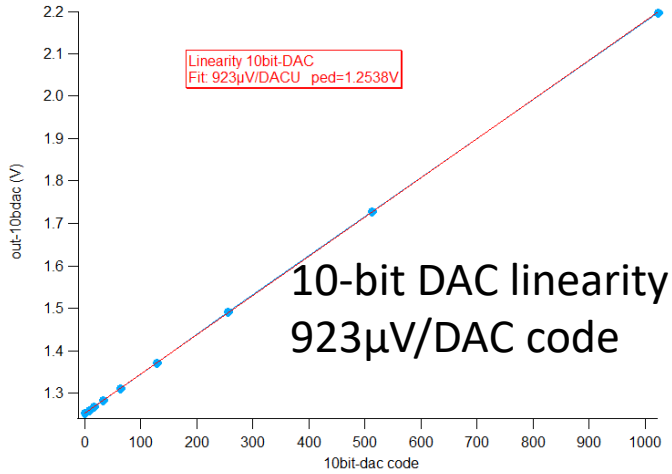


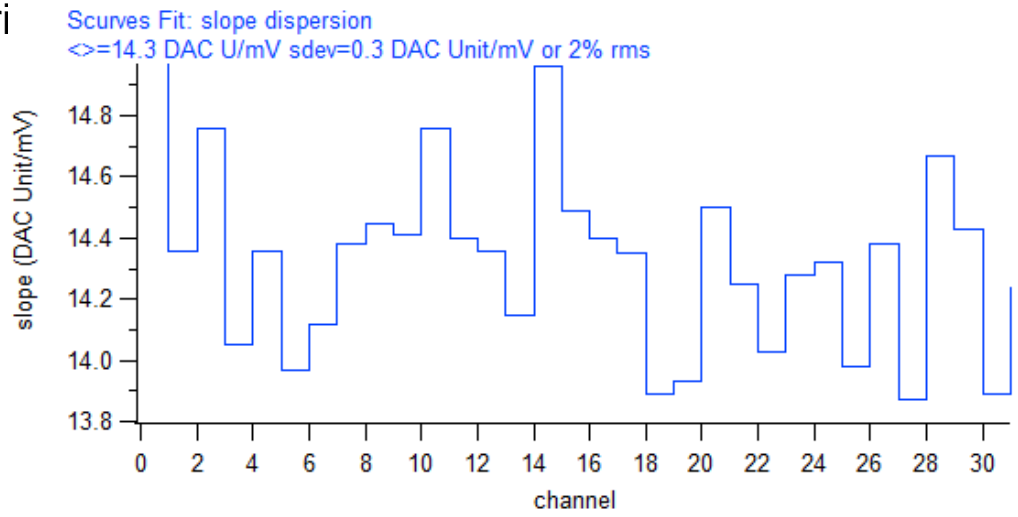
Dynamic range: 15fC - 50 pC

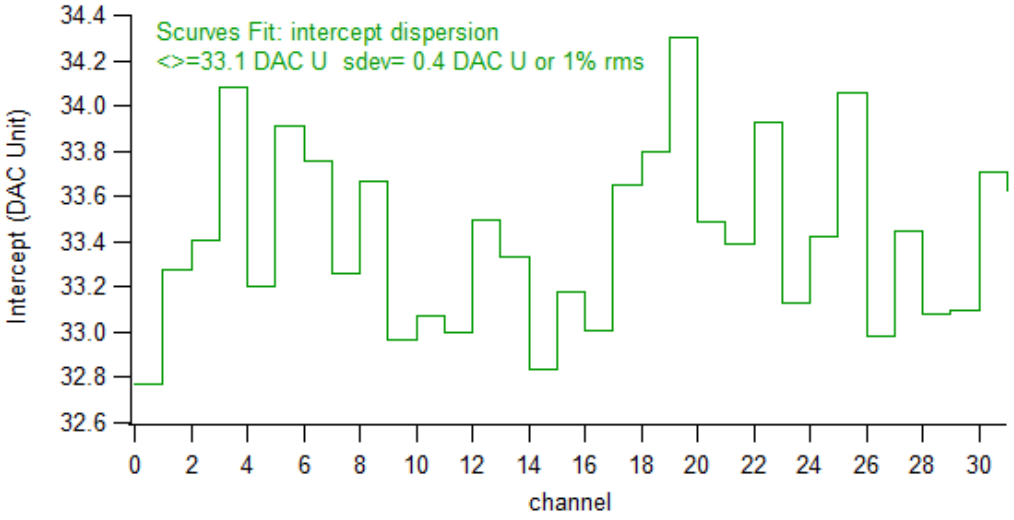
PETIROC2: efficiency uniformity

- Trigger efficiency measurements: Lineari
- One 10-bit DAC Unit= 923 µV



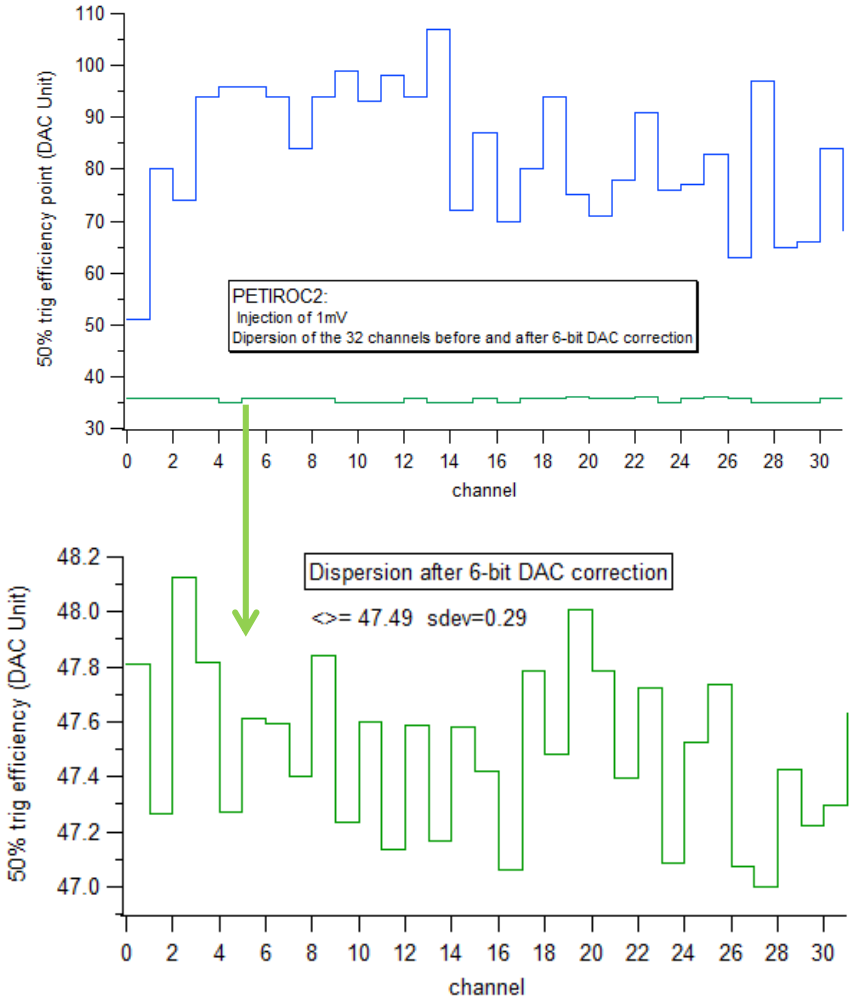


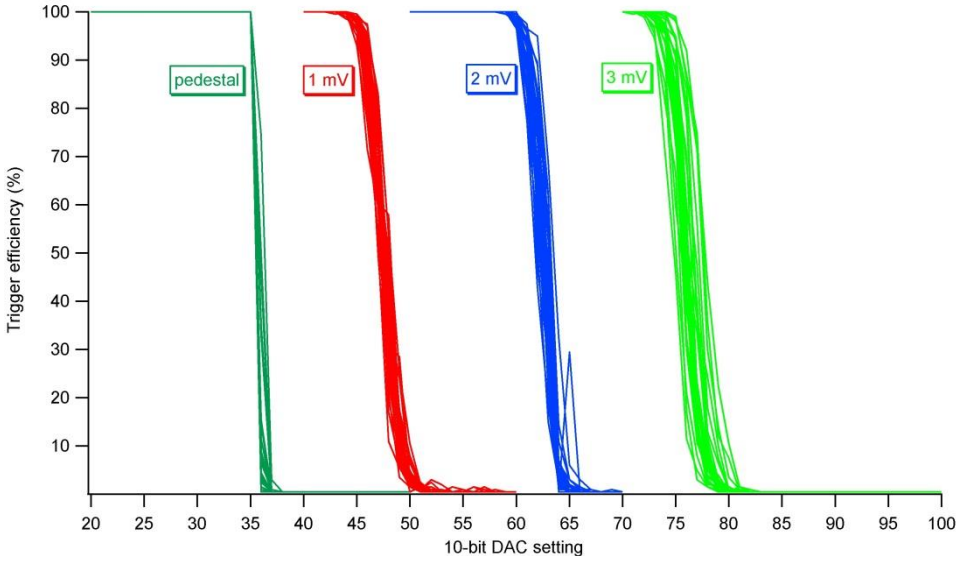


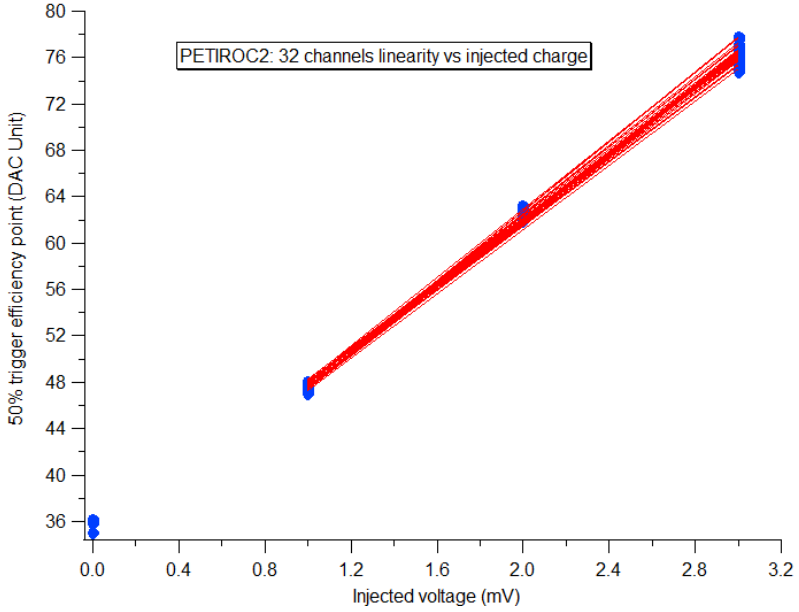


PETIROC2: « S-curves »

- Trigger efficiency measurements:





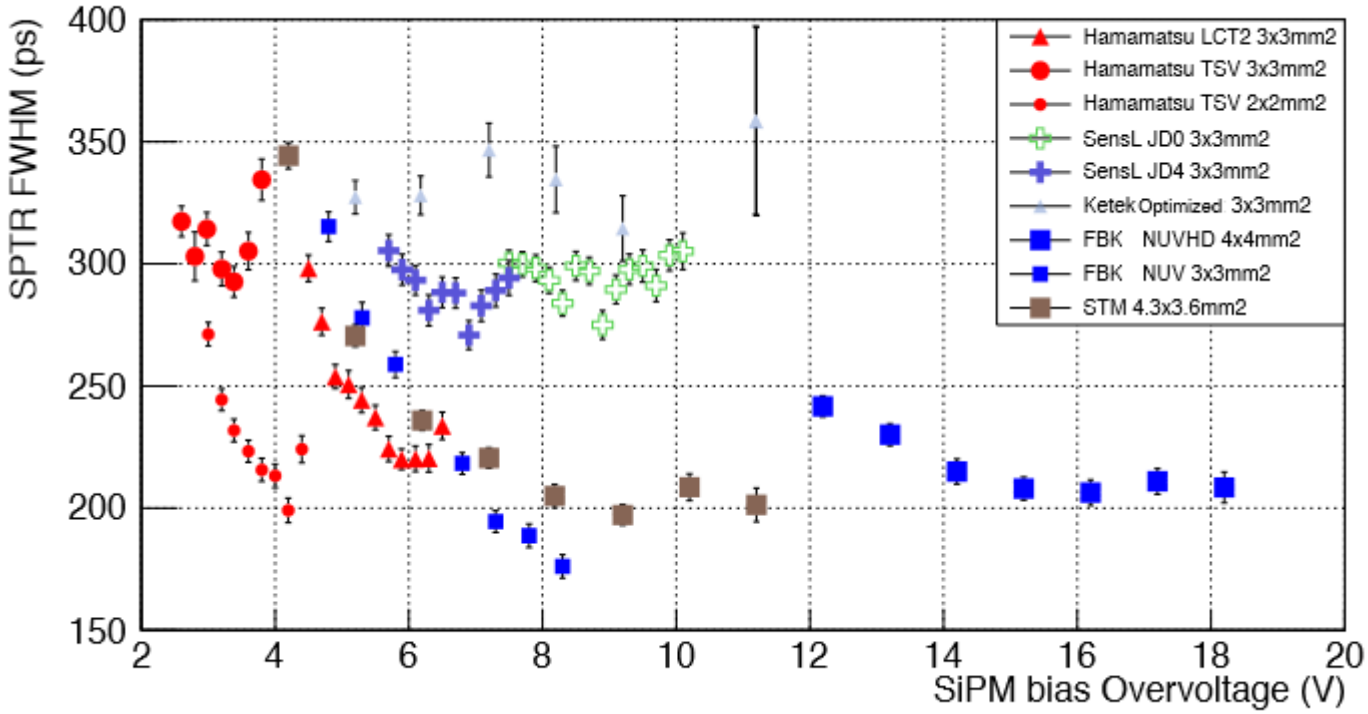


- SPTR
  - FWHM ~200 ps
  - Rms ~ 80 ps

Single photon time resolution of state of the art SiPMs

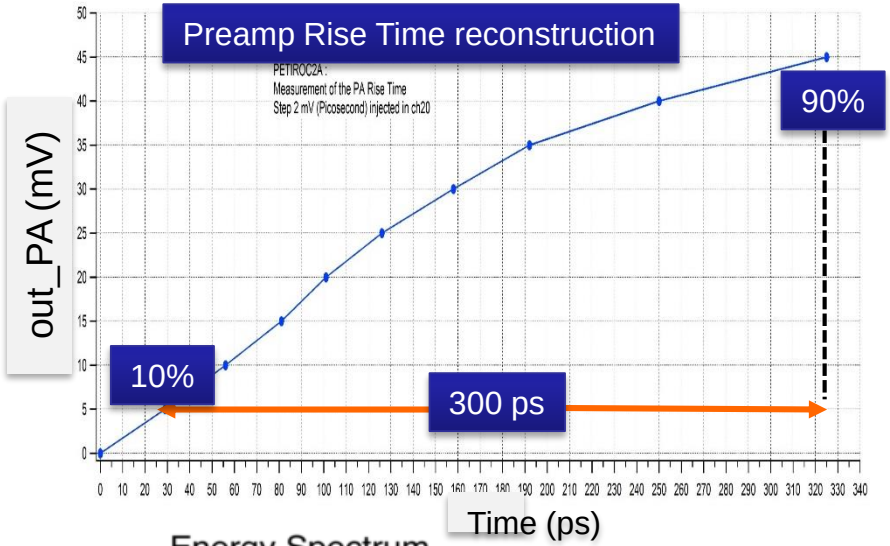
M.V. Nemallapudi,[1] S. Gundacker, P. Lecoq and E. Auffray

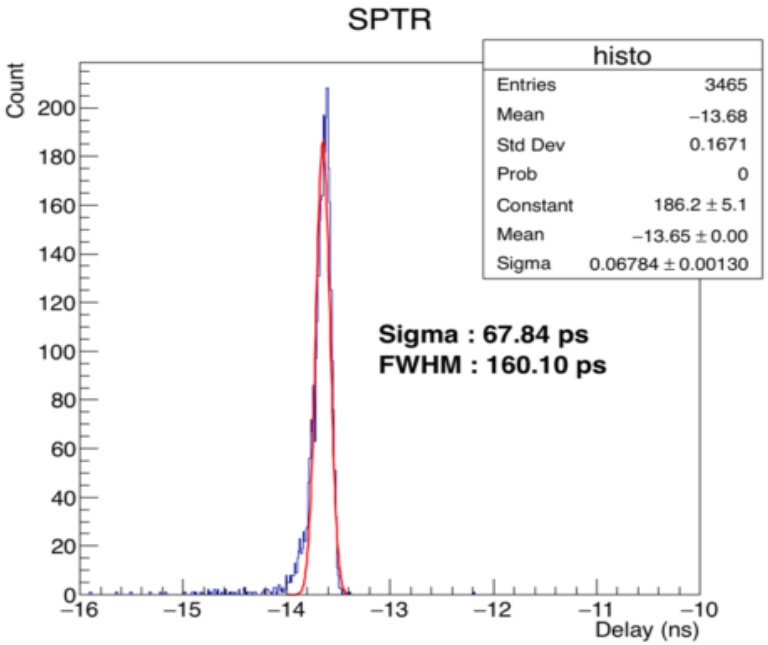
CERN,
23 Rue de Meyrin, Geneva, 1211-CH

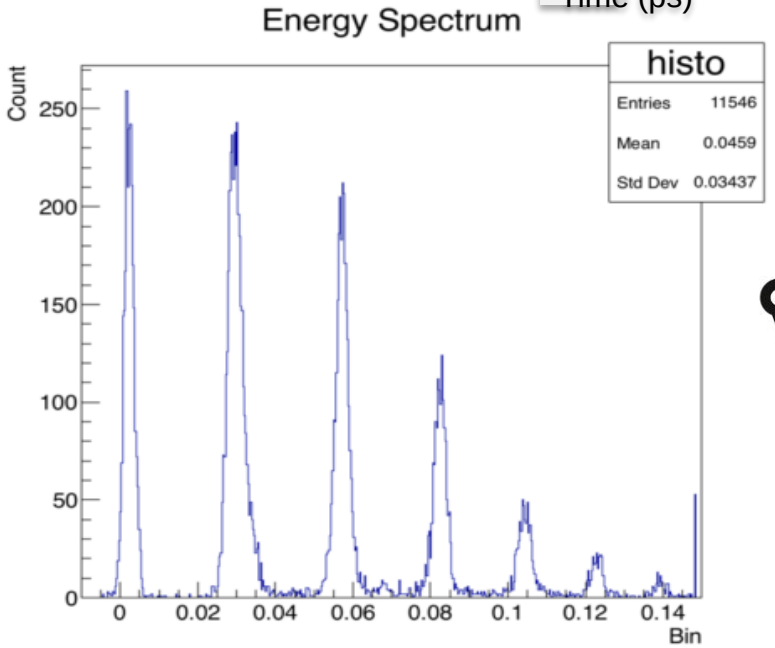


Going to lower SPTR

- Expect ~ 20 ps/pe
- NINO risetime ~1 ns
- Test with PETIROC2 (tr = 300 ps)
  - SPTR = 67 ps rms (180 ps FWHM)
- Possible effect of stray inductance
- Further studies in FAST framework







weeroc

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