Société Française de Physique

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MACHINE LEARNING FOR REAL-TIME PROCESSING OF ATLAS LIQUID ARGON CALORIMETER SIGNALS WITH FPGAS

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The Phase-II upgrade of the Large Hadron Collider (LHC) will increase its instantaneous luminosity by a factor of around 10 leading to the High Luminosity LHC (HL-LHC). At the HL-LHC, the number of proton-proton collisions in one bunch crossing, also known as pileup, increases significantly, putting more stringent requirements on the LHC detectors electronics and real-time data processing capabilities. The ATLAS Liquid Argon (LAr) calorimeter measures the energy of particles produced in LHC collisions and identify interesting events. The computation of the deposited energy is performed in real-time using dedicated data acquisition electronic boards based on FPGAs. FPGAs are chosen for their capacity to treat large amount of data with very low latency. The computation of the deposited energy is currently done using optimal filtering algorithms that assume a nominal pulse shape of the electronic signal. These filter algorithms are adapted to the ideal situation with very limited pileup and no timing overlap of the electronic pulses in the detector.

However, with the increased luminosity and pileup, the performance of the filter algorithms decreases significantly and no further extension nor tuning of these algorithms could recover the lost performance. The back-end electronic boards for the Phase-II upgrade of the LAr calorimeter will use the next high-end generation of INTEL FPGAs with increased processing power and memory. This is a unique opportunity to develop the necessary tools, enabling the use of more complex algorithms on these boards.

Making possible the artificial intelligence implementation in this phase. We developed neural networks (NNs) algorithms based on CNN (Conv-3 and 4) and RNN (Vanila-RNN and LSTM) with significant performance improvements. Especially for overlapping pulses, NNs outperform optimal filtering algorithms.

Also, the implementation were done in VHDL and Quartus HLS code. The implementation results on Stratix 10 INTEL FPGAs, including the resource usage, the latency, and operation frequency can be seen in the table represented in the poster, also we did studies about time multiplexing to reduce resource usage. Because multiplexing is used as strategy to enables one network instance to handle multiple calorimeter cells.

Further optimisation of resource usage and execution frequency are ongoing, as well as hardware tests on Stratix-10 FPGAs.

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