DIRAC2 2009 Testbeam Preliminary Results

R. Gaglione

Laboratoire d'Annecy-le-Vieux de Physique des Particules,
Université de Savoie, CNRS/IN2P3
FRANCE

November 17th, 2009

Outline

Outline

Outline

Introduction

Testbeam setup summary:

- 4 8×8 cm^2 DIRAC2 chambers (blue table);
- 3 PMTs, with $\simeq 8 \times 6$ cm^2 coinc $\rightarrow$ 3500 triggers/spill (red table);
- Labview acquisition software $\rightarrow$ 450 triggers/spill;
- Framework for quick analysis;

Events sequence

- 30 oct: installation, firsts data ! (this part)
- 31 oct: same setup, no more data... (see second part)
- 2 oct: only one chamber repaired, lot of interresting data to be analysed...

Data

30 oct: the configuration of the chip is "LAPP defaults"! No optimisation at all!

- 2 files: acq_30102009_2102_1.root and acq_30102009_2107_1.root → 37450 events;
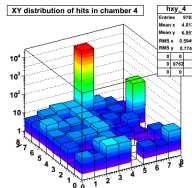- more or less the same setup (lowest threshold has been reduced in one chamber);
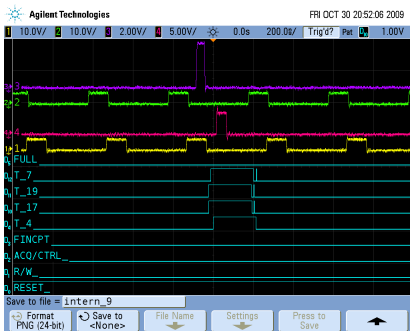
Outline

Setup

Channels 11 and 57 are masked in hardware (unable to trig) for all boards.

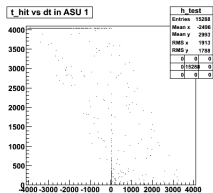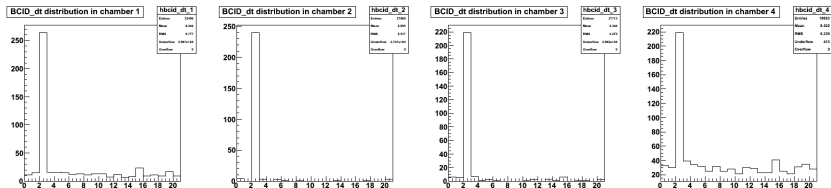| Chamber#	1	2	3	4
DIF#	7	19	17	4
low thr	7	14	14/13	7

Cut on dt>10:
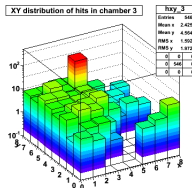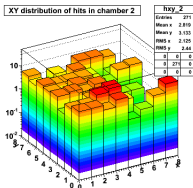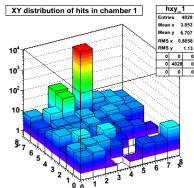
Noise Analysis

- Channels 11 and 57 are removed in analysis (maybe not necessary !);
- Remove bcid_hit=4095;
- Remove channel 32 on chamber 2 and 3;
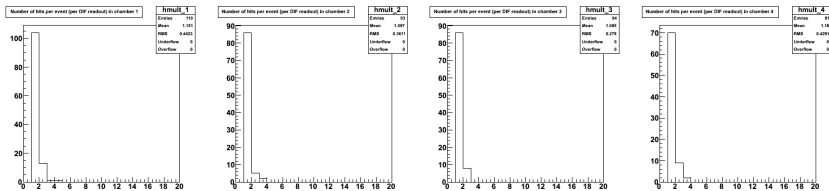- Cut on dt=2;

Data quality

t_hit *versus* dt:
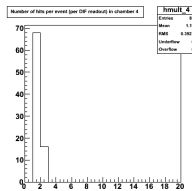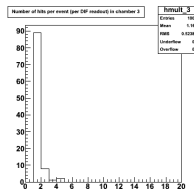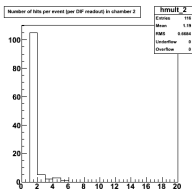

Only with cut bcid_hit≠4095:

Very clean as it is!
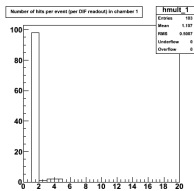
Run 31102009_2102:

Run 31102009_2107:
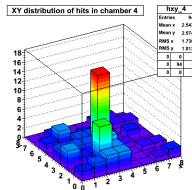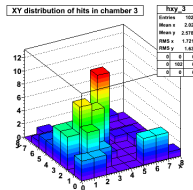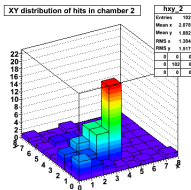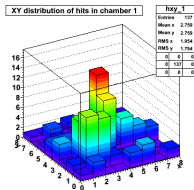
Run 31102009_2102:

Run 31102009_2107:

TO BE DONE !

Outline
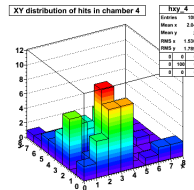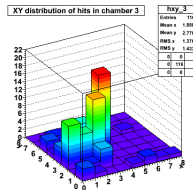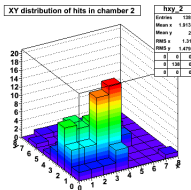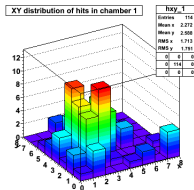
Very useful tool, but:

- 1 event $=$ 1 readout of all channel of all DIFs will be nice ;)
- sort event versus abs bcid will be nice too (Jean is working on) ;
- Wrong bcid abs (Laurent is working on) ;
- Still some error message on reconstruction;
- Question: on "bad" event, is the whole physical event skipped or just current DIF readout ?

Outline

Outline

History

- 30 oct: first data to check beam and trigger quality with DIRAC stack "out of the box";
- 31 oct: unable to see coincidence on the 4 chambers, very low efficiency;
- 1 nov: electronic check: wrong DC point at the input of the chamber 4 and 3... all chambers are damaged !
- 2 nov: one chip has been exchanged with the only one spare;
- 5 nov: beam profile versus time, input voltage measurements.

Outline

DC input voltages

The inputs of the chip must be at 580+/-15 mV, and we got a large spread from few mV to 3.5 V.
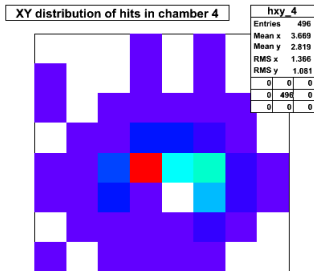$\rightarrow$ New calibration of this board to check each channel:

```
X  X  X  X   X   X  X  X
X  X  X  X   X   X  X  X
X  X  X  X   X   X  X  X
X  X  X  X   X   X  X  X
X  X  X  X   X   O  O  O
X  X  X  X   X   O  O  O
X  X  X  X   X   O  O  O
X  X  X  X  XO   O  O  O
```
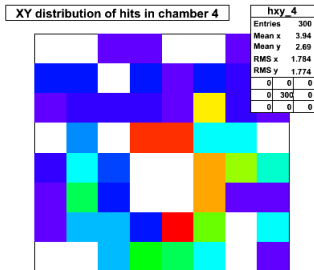
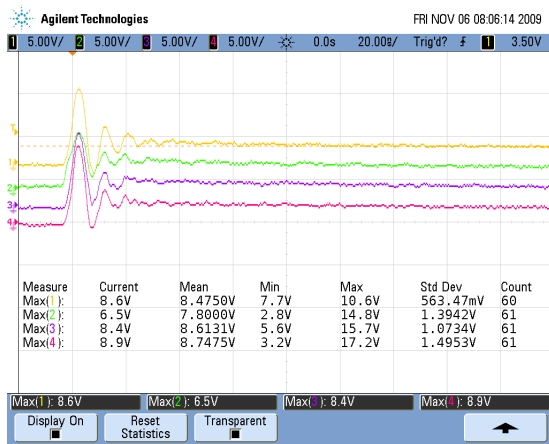Need to check other boards to verify the pattern.

Run 02112009_1717:

Run 02112009_1802:

Voltage monitoring

The maximum voltage for AMS C35B4 is 5.5 V and the gate oxyde breakdown voltage is 8 V...

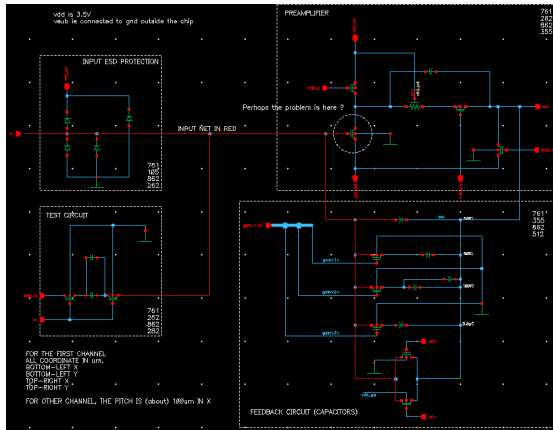With a $800\times$ magnification: nothing to see. . .

. . . to SEM inspection !

SERMA technologies will inspect the input net of the chip to check for defects in polysilicon/metalizations.
The result is expected in about 2 weeks.

Outline

Conclusion

Good point: DIRAC stack has been working "as it is" without any optimisations (very good work of all the team BEFORE test beam);

To do now:

- Repair the stack for cosmics;
- Prepare new chambers with stronger protections;
- Protection testboard !
- Diodes engineering.