Selective Summary of ECFA Detector R&D Roadmap Symposium of Task Force 3 Solid State Detectors on 23/4/2021

A. HABIB

Disclaimer

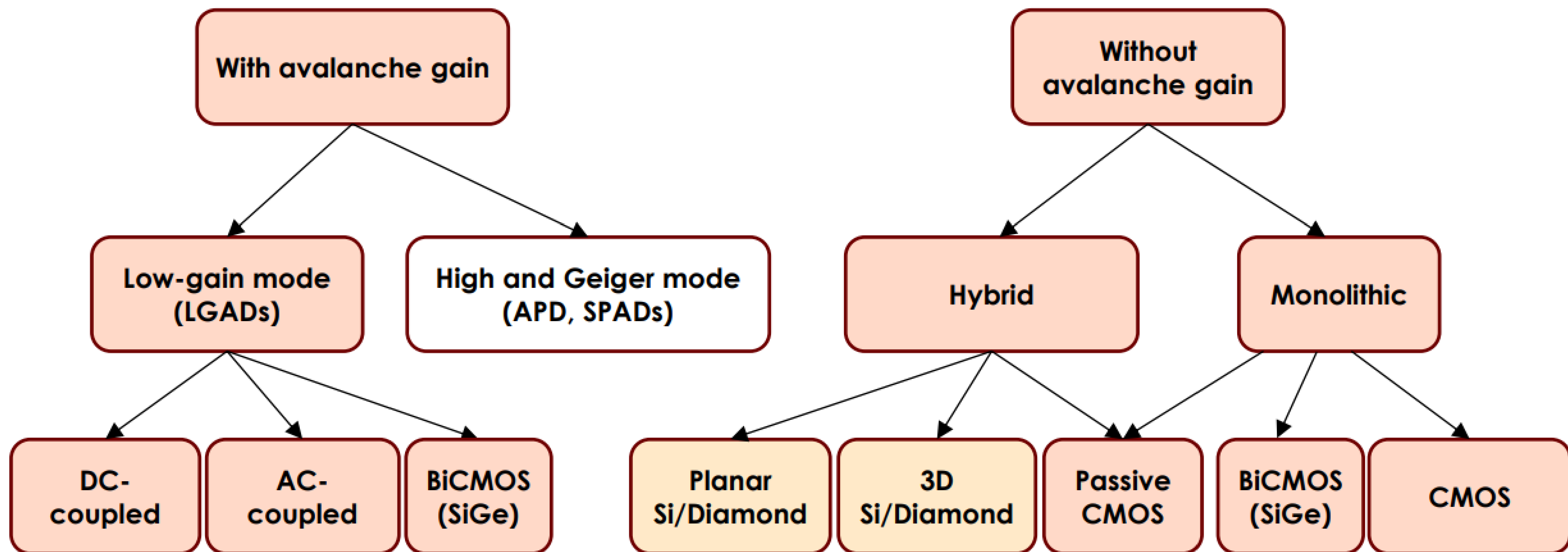
- All of the slides of this presentation are taken from the original presentations that can be found here: https://indico.cern.ch/event/999816/

- This summary is selective and subjective and does not reflect all of the presentations at the symposium.

Presentation plan

- Towards more density
- Towards faster sensors
- Towards bigger sensors
- Conslusion

Solid state detectors for future (4D) trackers



Presentation plan

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Advanced pixel detectors and readout microelectronics

Particle tracking at LHC- Phase II:

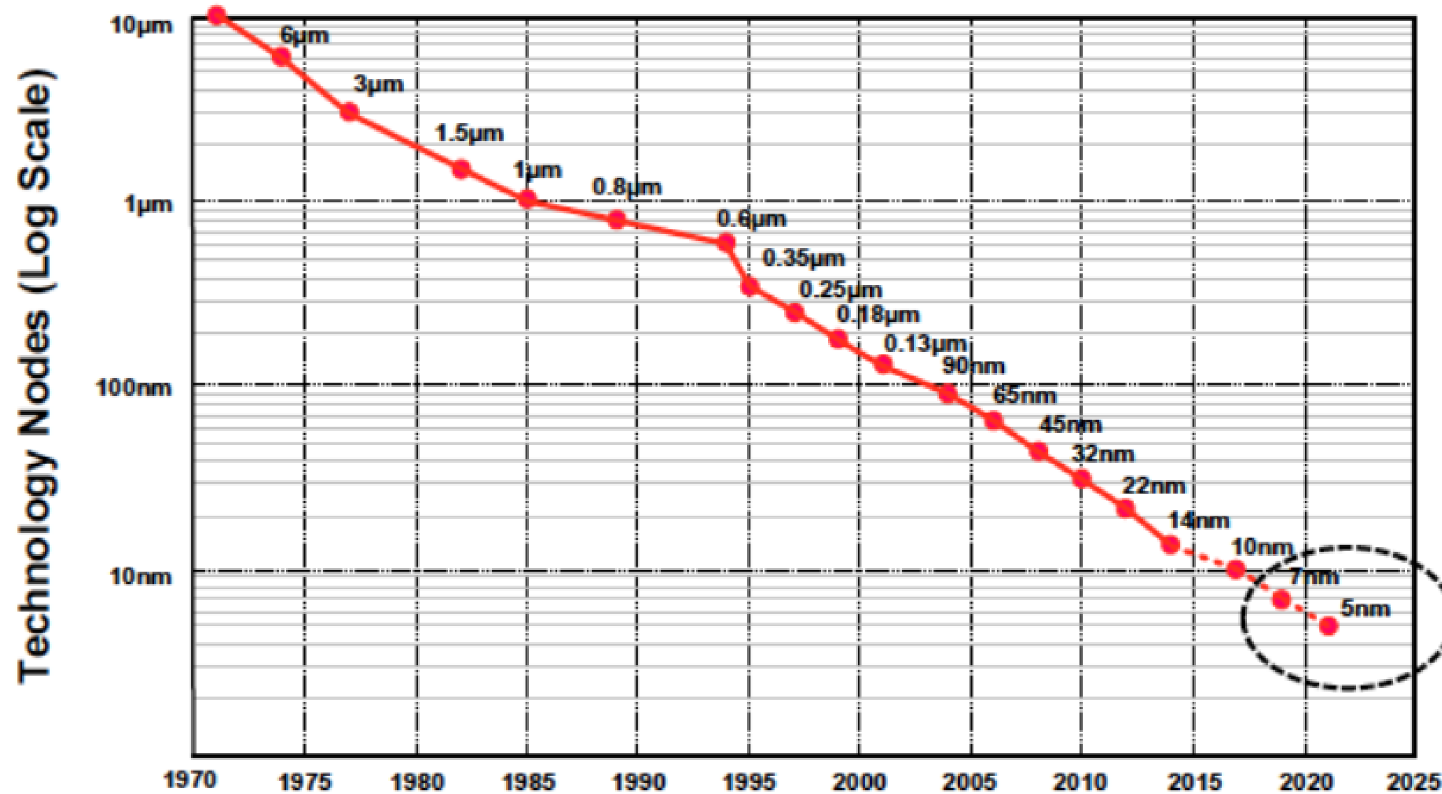
- Very high hit rates (3 GHz/cm^2), need of an intelligent pixel-level data processing
- Small detector signals require operating at low threshold (< 1000 electrons)
- Very high radiation levels (1 Grad Total Ionizing Dose, 10^{16} $neutrons/cm^2$)
- Small pixel cells to increase resolution and reduce occupancy (~$50 \times 50 \mu m^2$)

➔ Large chips: > 2cm x 2cm, ½ - 1 Billion transistors

FCC-hh:

- **Radiation levels expected to increase in inner layers (25 mm):**
  up to 30 Grad and 10^{18} $neutrons/cm^2$
- **Smaller pixels (avoid in-pixel pileup)**
  (~25×50 μm^2) the need for higher logic density is not a function of pixel size, but of hit rate per unit area.
- **Huge data rates:**
  - Max hit rate 20 $Gb/s/cm^2$, will need 50-100 Gbps low-power, low-material data links

Scaling of microelectronic processes



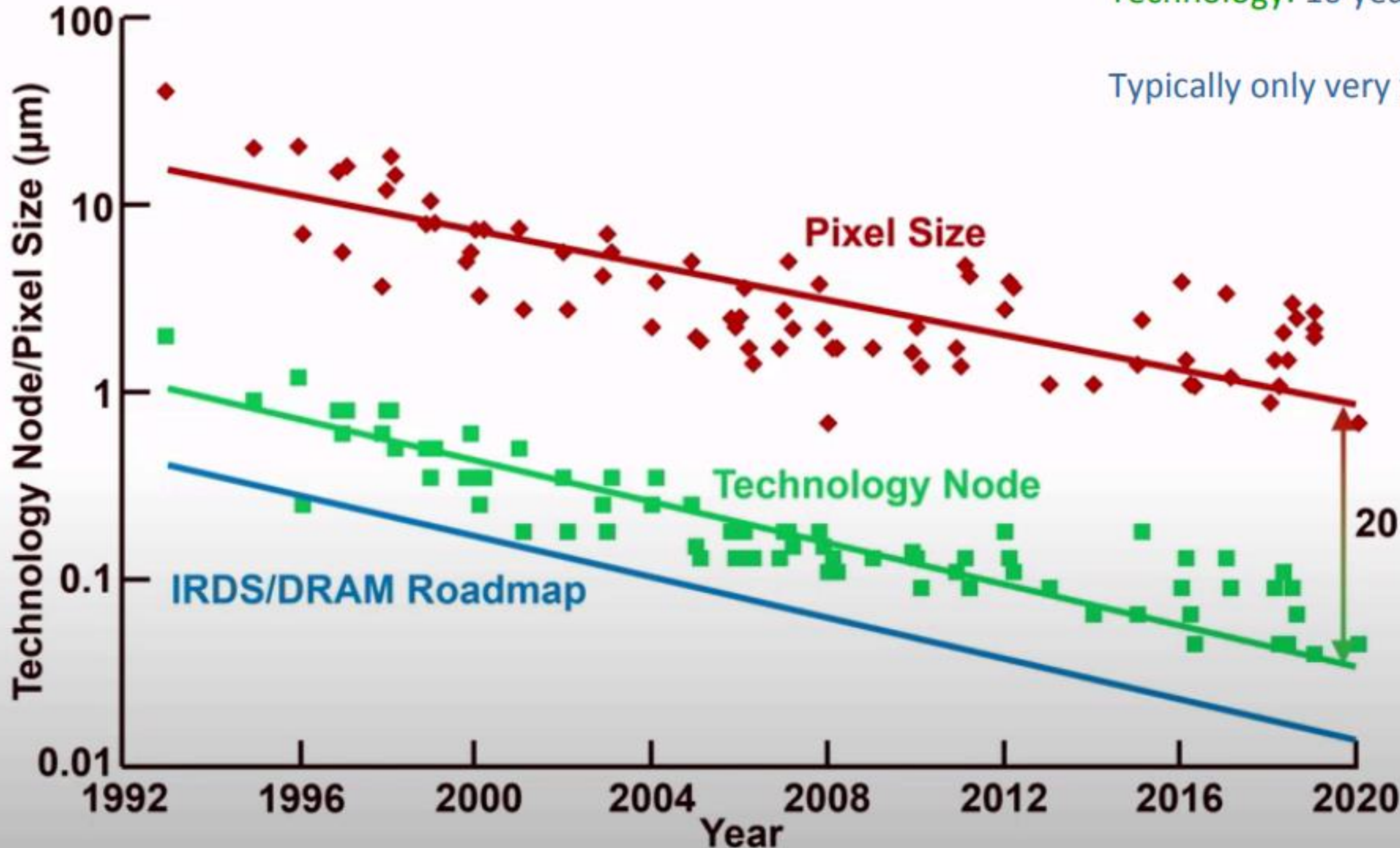
Source: Semiconductor device fabrication https://en.wikipedia.org/wiki/Semiconductor_device_fabrication

The meaning of scaling

Scaling is about density (not, or not only about the gate length of transistors) ⇒ more speed, more power/energy efficiency

For recent CMOS nodes, "7 nm", "5 nm" are not related to a feature size: they give an indication of the achievable density of transistors

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

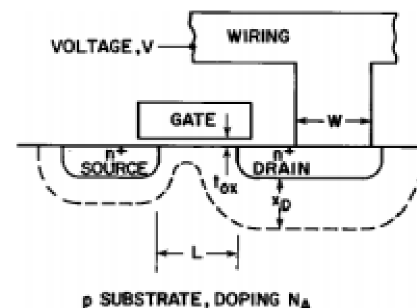
Typically only very few (1-4) transistors per pixel

Albert Theuwissen, ISSCC 2021

The old ways of CMOS scaling

- **Shrinking of gate length** leads to an increase in speed and circuit density. To avoid short-channel effects, drain and source depletion regions are made correspondingly smaller by **increasing substrate doping concentration** and decreasing reverse bias (**reduction of the supply voltage**)
- Increasing substrate doping increases the device threshold voltage: this is overcome by **decreasing the gate oxide thickness**.
- Classical scaling ended because of gate oxide thickness limits: in very thin oxides, direct tunneling of carriers leads to a large gate leakage current.

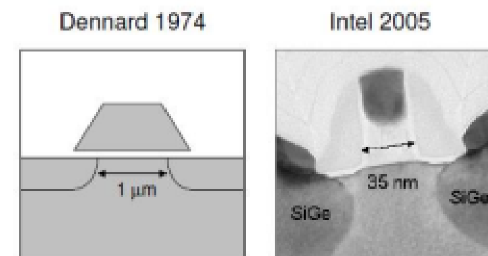
Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/κ
Doping concentration *Na*	κ
Voltage *V*	1/κ
Current *I*	1/κ
Capacitance *εA/t*	1/κ
Delay time/circuit *VC/I*	1/κ
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1



R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling was first described in 1974

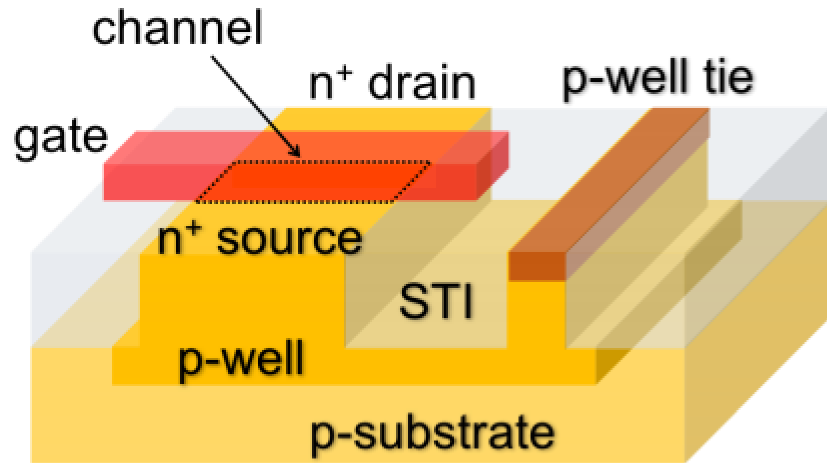
30 Years of MOSFET Scaling

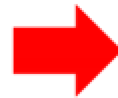


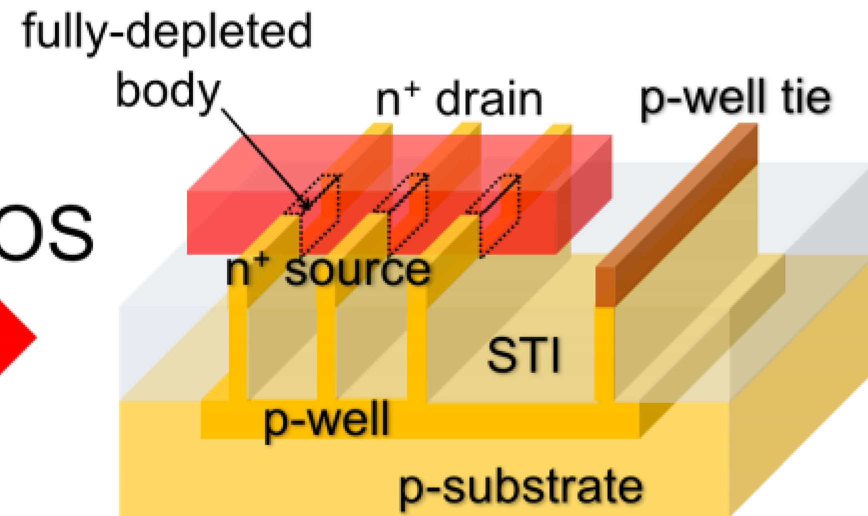
	Dennard 1974	Intel 2005
Gate Length:	1.0 µm	35 nm
Gate Oxide Thickness:	35 nm	1.2 nm
Operating Voltage:	4.0 V	1.2 V

Modern CMOS scaling is as much about material and structure innovation as dimensional scaling

Below 28 nm, FinFET





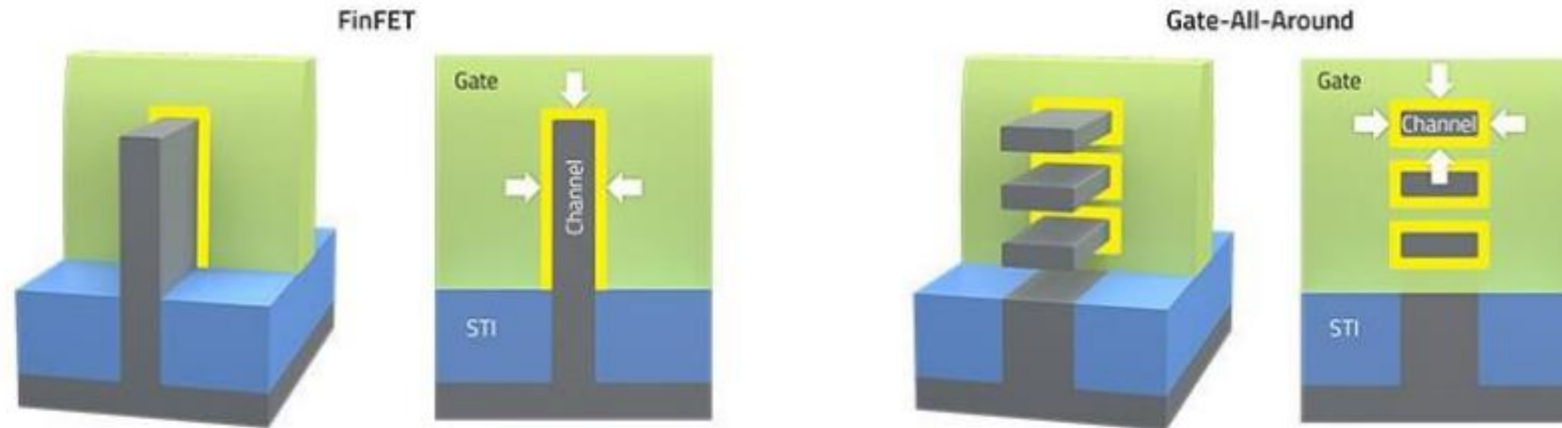


Three-dimensional, Gate-All-Around vertically stacked transistors

At reduced gate length, even the FinFET fails to provide enough electrostatic control of the channel. The scaling of the size of standard cells requires using single-fin devices, which cannot provide enough drive current

GAA = Gate All Aroud

In GAA transistors, the channel is divided into separate horizontal sheets. As the gate now fully wraps around the channels, superior channel control is obtained compared to FinFET
The sheet-to-sheet spacing, analogous to fin pitch, is determined not by lithography but tightly controlled epitaxial processes.



Improved gate control was developed in FinFET to decrease leakage current, reduce short channel effects (which also may lead to higher gain) and process-induced variability

The improved electrostatics of GAA transistors can help in increasing the gain

Tolerance to high Total Ionizing Dose of nanoscale CMOS

In RD53, the extensive characterization of the LP 65 nm CMOS technology led to the definition of analog design guidelines to prevent degradation of transconductance and excessive threshold voltage shift
($W_p \geq 300$nm $L_p \geq 120$nm $L_n \geq 120$nm)

Can similar criteria be defined for 28 nm CMOS, for FinFET and GAA processes?
What is the noise behavior at extremely high TID?
Can a 28 nm CMOS chip (or, e.g., a 14 nm or a 5 nm one) work with acceptable performance at TID > 1 Grad?
(see the excellent and extensive work by CERN, Padova et al, to characterize radiation hardness of 28 nm CMOS at very high total ionizing dose)

A significant radiation-induced parasitic leakage current can be observed for bulk FinFETs due to charge trapping in isolation oxides, particularly for narrow-fin transistors

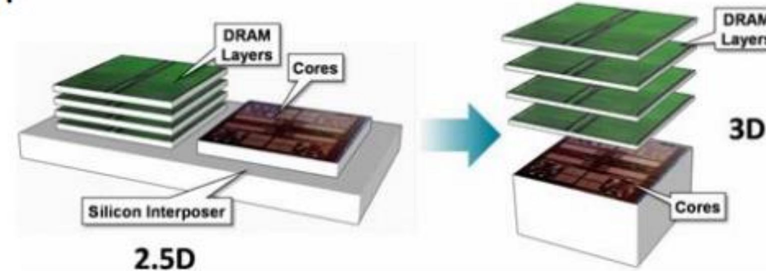
(D. Fleetwood, Evolution of Total Ionizing Dose Effects in MOS Devices with Moore's Law Scaling, IEEE TNS, 2017)

3D integration as a tool to advance the state of the art of pixel sensors

- **The increase of functional density can be achieved by stacking layers of electronics, vertically interconnected by Through-Silicon Vias (TSV)**

  ⇒ interconnect delays can be reduced

  ⇒ each layer can be optimized for a dedicated function (sensing analog processing, DSP, memory, optical data transmission `



- For our pixel sensors, 3D integration could be leveraged to shrink pixel size and pitch, increase pixel-level electronic functions, reduce dead areas, decrease amount of material by aggressive thinning

Examples:

M. Kwon et al., A Low-Power 65/14nm Stacked CMOS Image Sensor", Samsung, ISCAS 2020

"Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology" H. Tsugawa et al. Sony, 2017 IEEE IEDM

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

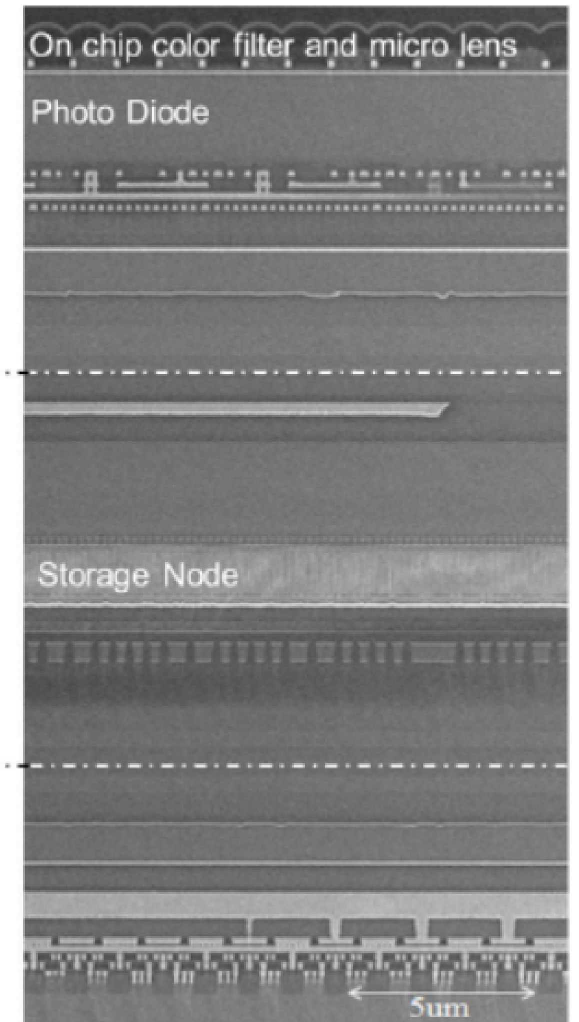
… and now CMOS MAPS make their way in High Energy Physics !

Hybrid still in majority in presently installed systems

Top part
(BI-CIS process technology)

Middle part
(DRAM process technology)

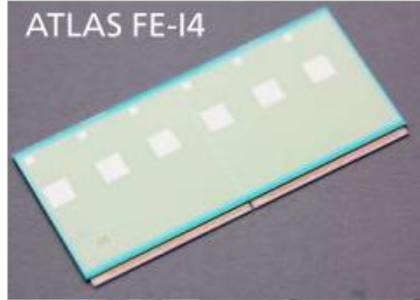
Bottom part
(Logic process technology)

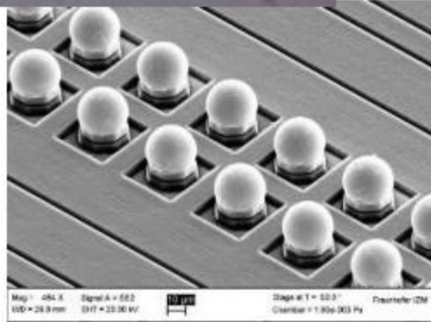


Sony, ISSCC 2017

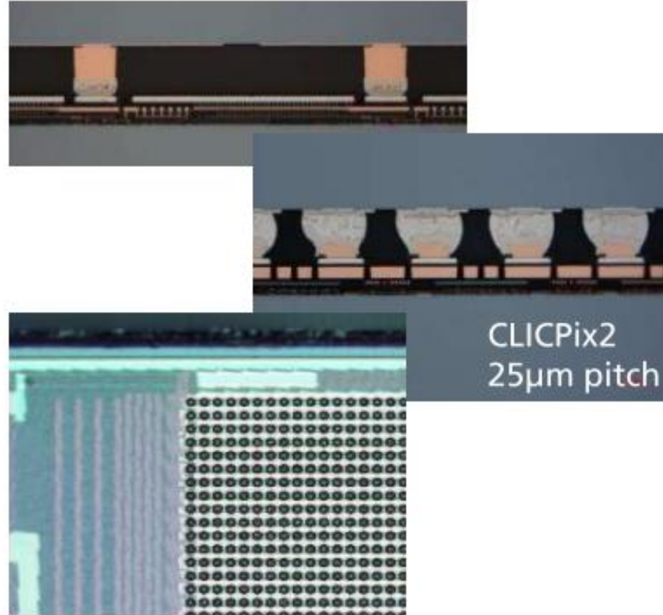
New technologies (TSV's, microbumps, wafer stacking…) make the distinction more vague.

Flip Chip Assembly Key Parameter: Interconnection Pitch

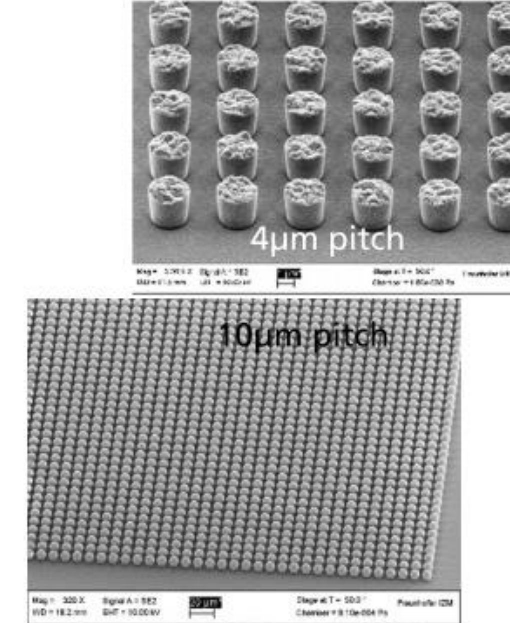




Fine pitch bumping:
Pitch 100…50µm
Bump size: 50…25µm
Material: Solder bumps, pillar bumps with solder cap



µ-bumping:
Pitch 50…20µm
Bump size: 25…12µm
Material: Solder bumps, pillar bumps



Sub-10µ-pitch:
Pitch 10…2 µm
Bump size: 6…1µm
Material: pillar bumps, metal pins

Reduction of pixel pitch – more challenging assembly process

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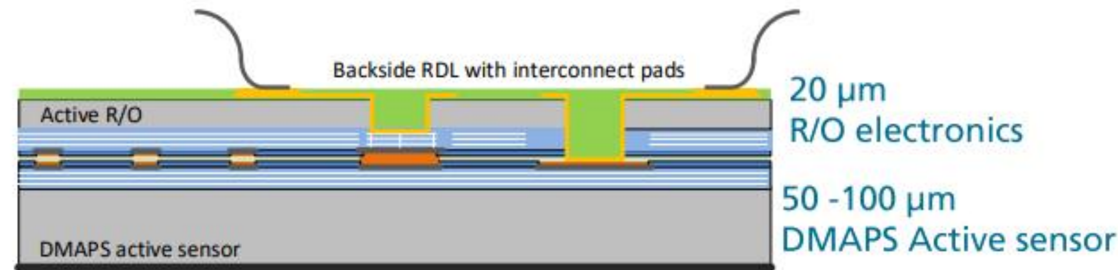
Ultra Thin Hybrid Pixel Detectors

- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer with backside via last interconnection
- Bonding layer with metal-metal or capacitively coupled contacts
- Thin DMAPS sensor with contact pads and backside processing

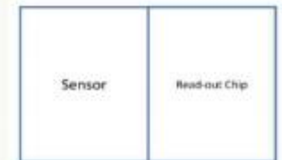


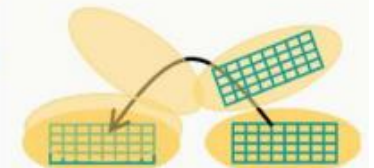
20 µm
R/O electronics

50 -100 µm
DMAPS Active sensor

Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:

- Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
- Use either TimePix3 chip wafers (130 nm on 200 mm wafers) or own FE development on the same wafer as the sensor
- Develop and optimize hybridization process including thinning and interconnection from chip's backside
- Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics (long term, not with AIDAinnova)





Task 6.4: Wafer to wafer bonding technique

Slides: F. Huegging (Bonn), I. Gregor (DESY&Bonn), T. Fritzsch (IZM)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

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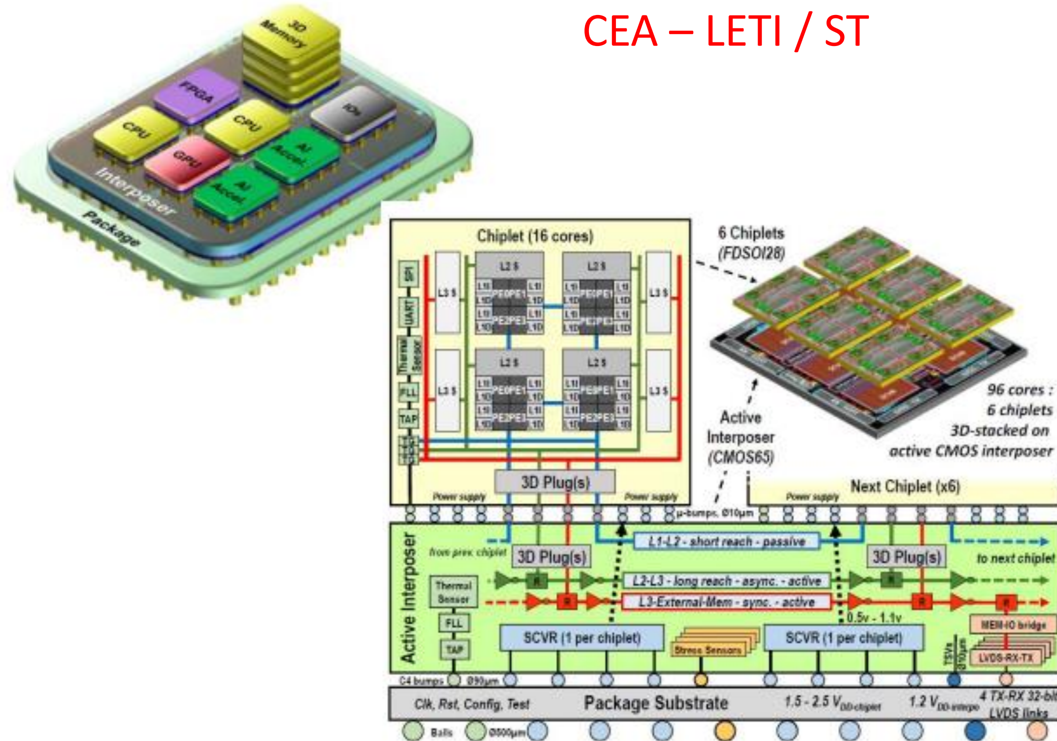
Industry Technology Trend: Processor Chiplet Assembly on Active Interposer



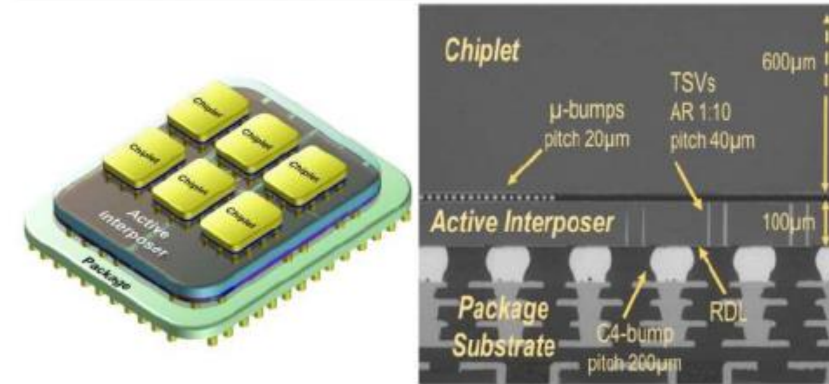


Fig. 5. INTACT : from concept to 3D-cross section

TABLE I: INTACT MAIN CIRCUIT FEATURES AND 3D TECHNOLOGY DETAILS

Chiplet technology	FDSOI 28nm, 10 metals, 0.5V-1.3V+adaptive biasing
Chiplet area	4.0 mm x 5.6 mm = 22.4 mm²
Chiplet complexity	395 Million transistors, 18 transistors/µm² density
Interposer tech.	CMOS 65nm bulk, 7 metals, MIM option, 1.2V
Interposer area	13.05 mm x 15.16 mm = 197.8 mm²
Interposer complexity	15 Million transistors, 0.08 transistors/µm² density
3D technology	Face2Face, Die2Die assembly onto active interposer
µ-bump technology	Ø10µm, pitch 20µm
#µ-bumps	150 000 (20k signals + 120k powers + 10k dummies)
Inter-chiplet distance	800µm
TSV technology	TSV middle, Ø10µm, height 100µm, pitch 40µm
#TSV	14 000 TSV (2 000 signals + 12 000 power supply)
Backside RDL	10µm width, 20µm pitch
C4-bumps	Ø90µm, pitch 200µm, 4,600 bumps
Flipchip package	BGA 39 x 39, 40mm x 40mm, 10 layers
Balls	Ø500µm, pitch 1mm, 1 517 balls

Pascal Vivet, Eric Guthmuller, Yvain Thonnart, Gaël Pillonnet, Cesar Fuguet, et al.. IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management. IEEE Journal of Solid-State Circuits, Institute of Electrical and Electronics Engineers, 2020, pp.1-1. 10.1109/JSSC.2020.3036341 . hal-03072959

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Presentation plan

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- Towards bigger sensors
- Conslusion

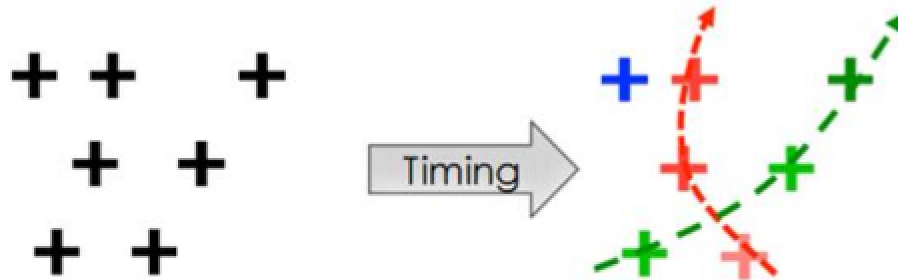
4D tracking

Benefits of more distant future full 4D tracking (each hit has precise 4D stamp):

- much better/simpler pattern recognition, ghost rate reduction
- better and faster tracks/physics reconstruction, better tracking algorithms
- less CPU power (improved cost and energy efficiency)
- effectively more luminosity

Near future: timing layer(s) – assigning the time stamp to the track

- Smaller spatial, but very good timing resolution (different technologies, harder integration)



Facilities/experiments mainly expressing the interests:

- Beam monitors
- Future HL/HE/Hadron colliders also ee machines and rare decay experiments
  - Tracking
  - Calorimetry
- Outside HEP:
  - Medical imaging
  - Therapy beam monitoring

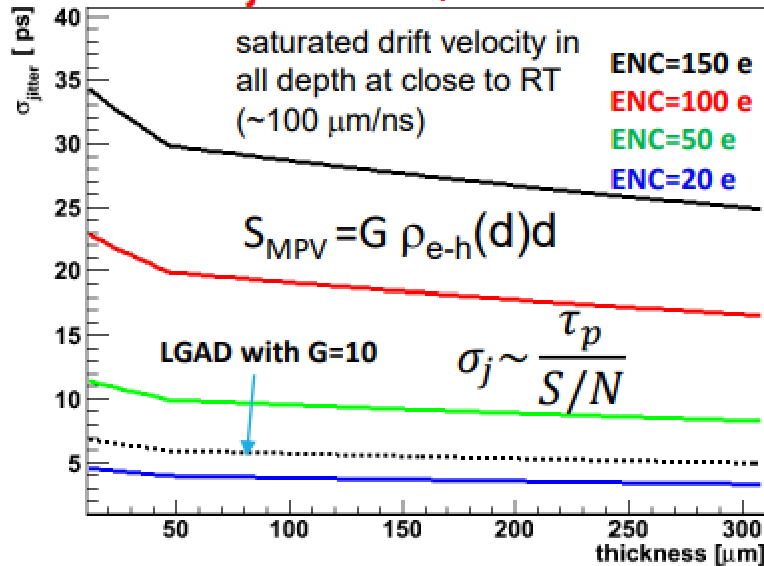
much easier tracking with “time compatible” points only
4D means going from now few ns (tens ns) to few tens ps – 2-3 orders of magnitude better, while retaining the superb spatial resolution

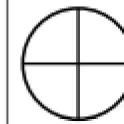
Limits for planar sensors

*NA62, NIM A958 (2020) 162127
**ATLAS HGTD TDR

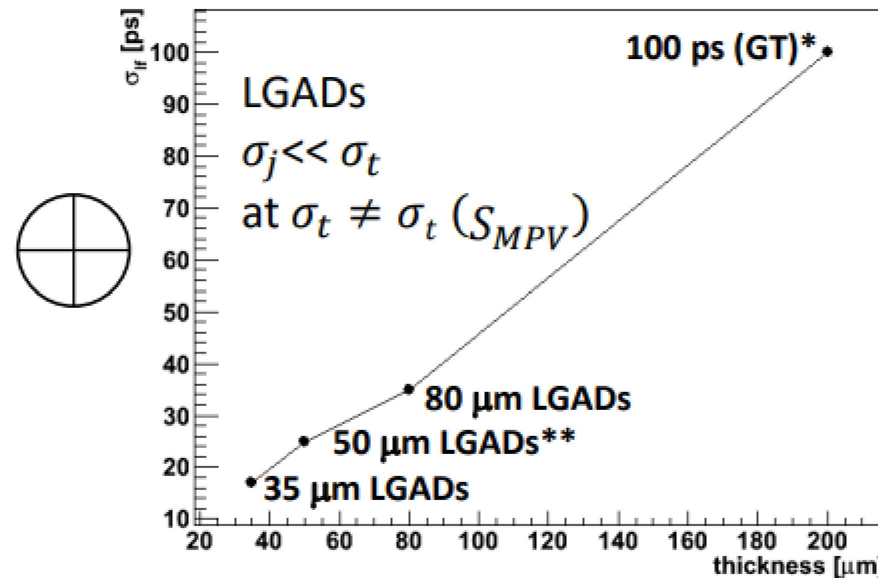
Planar sensors: NA62 giga-tracker (200 μm, p-n, TDCPix, 300x300 μm²)*: σ_j~80 ps, σ_{wf}~ 80 ps , σ_{lf}~ 100 ps : σ_j~140 ps
This represents roughly the limits achievable with conventional planar detectors of that thickness.

σ_j - Jitter (τ_p= $t_{collection}$)





σ_{lf} - Landau fluctuations



Wf: weighting field

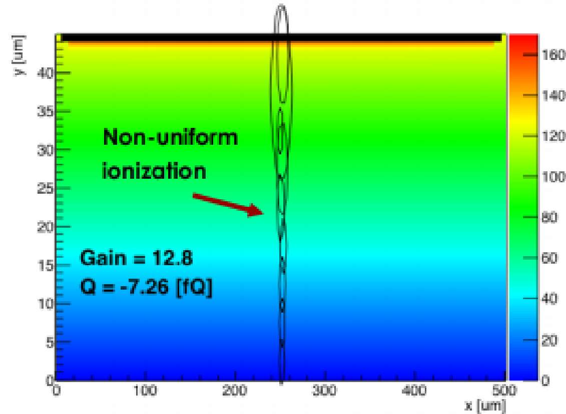
σ_{wf} (segmentation pitch/thickness) ≈ **~10 ps** is (almost?) impossible in Si planar technology

LGADs (planar sensors with gain) seem to be ideal solution to reach superb resolution for large pixels/pads
- large capacitance (noise) can be offset by gain -> good S/N (with discrete electronics 80-100)
- σ_{wf} ~ 0
- Inter-pad no gain region is not critical (IP/cell size ~ 0)

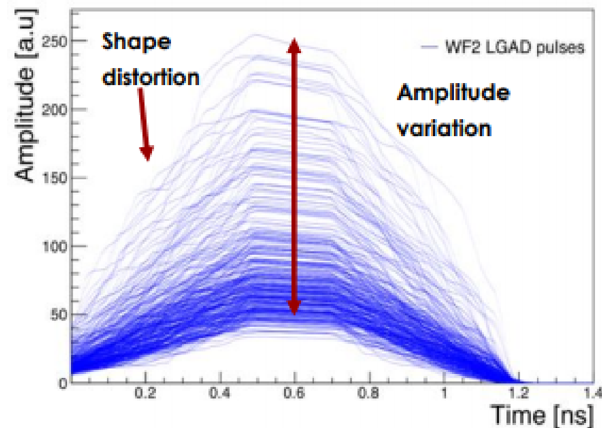
Main LGAD limitations:
- Radiation hardness (currently $\Phi_{eq}<3\cdot10^{15}$cm^{-2})
- Fill factor for small pixels

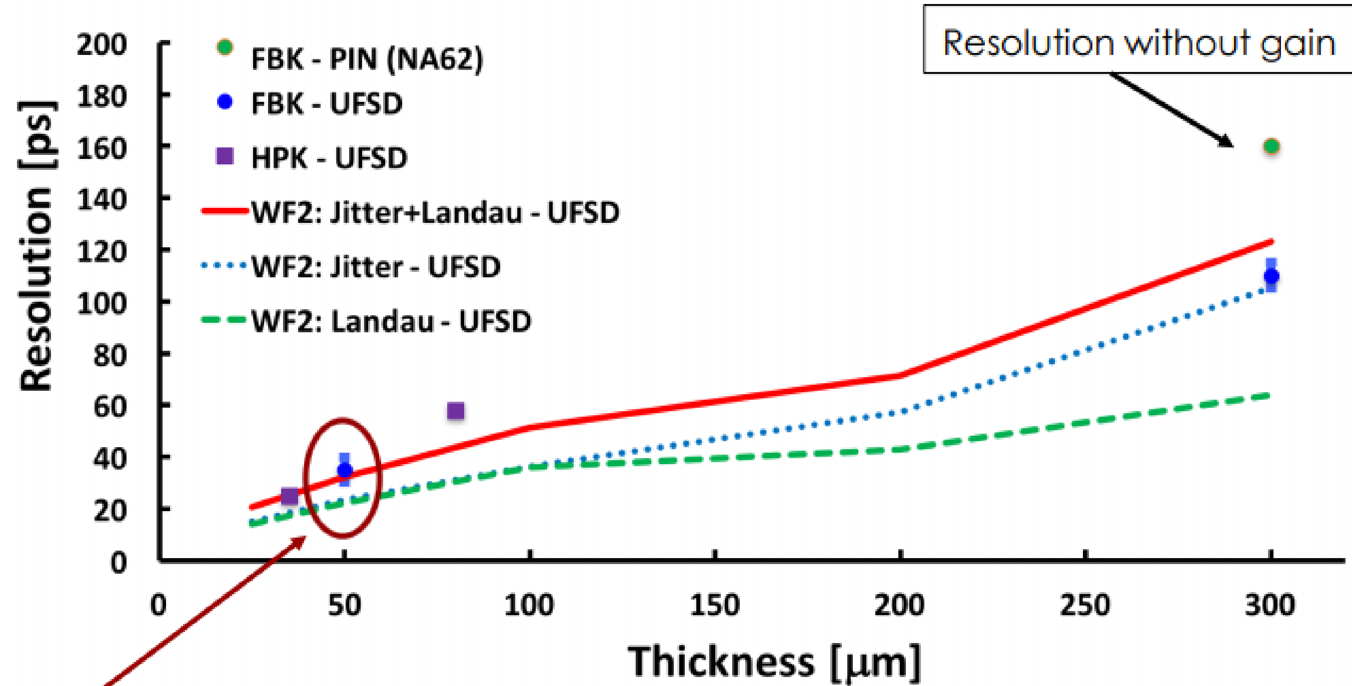
Summary of LGAD temporal resolution

Physical limit:
non uniform signal shape



Simulation of signals in 50-um RSD





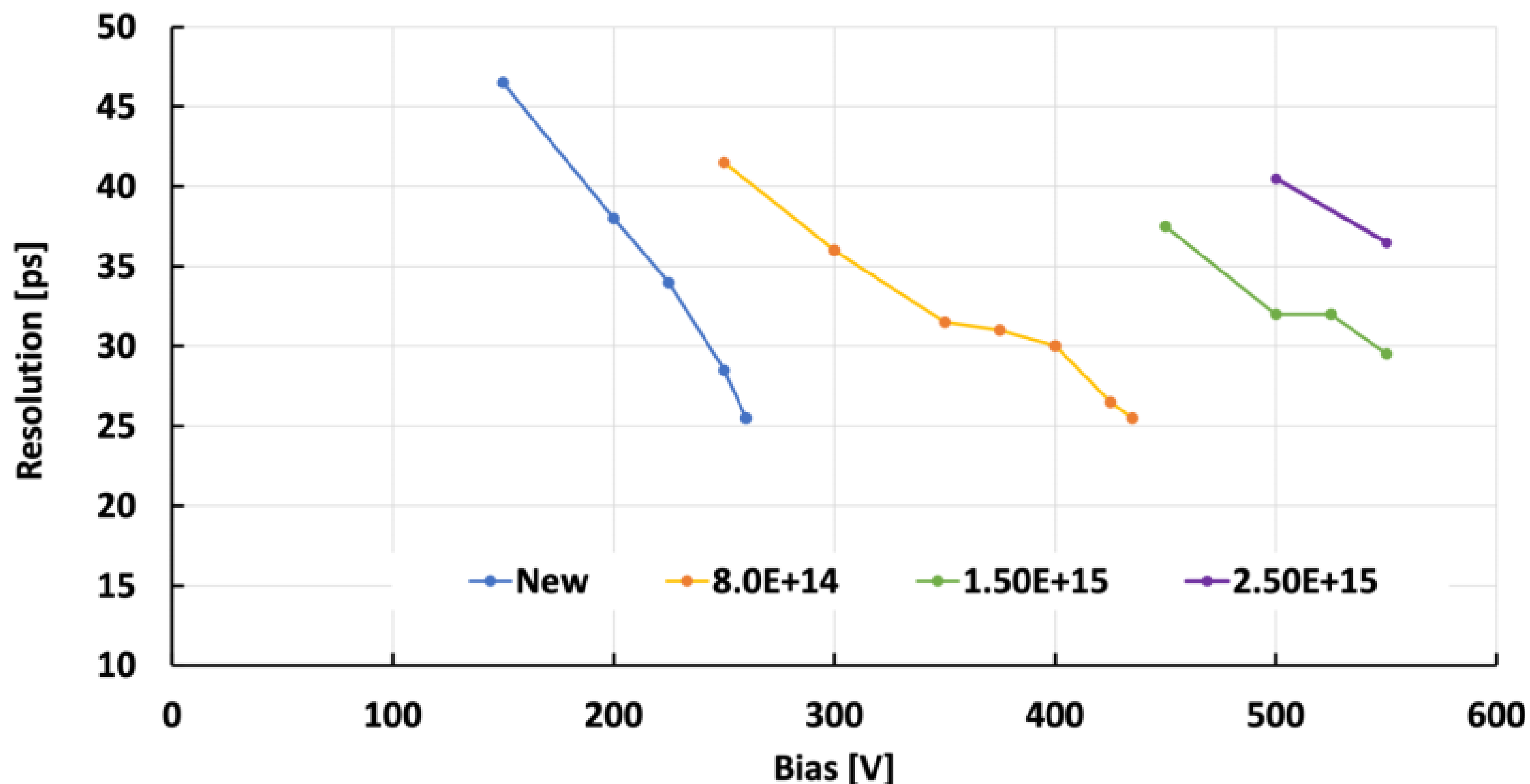
There are now hundreds of measurements on 45-55 µm-thick UFSDs

➔ Current sensor choice for the ATLAS and CMS timing layers

LGAD radiation hardness

Evolution with radiation of the biasing working point for a 45-micron thick LGAD with a carbonated gain layer

Increase bias to compensate for gain implant doping deactivation.



Present LGAD designs provide large signals and low noise up to 2.5E15 n/cm2

Depleted MAPS - planar

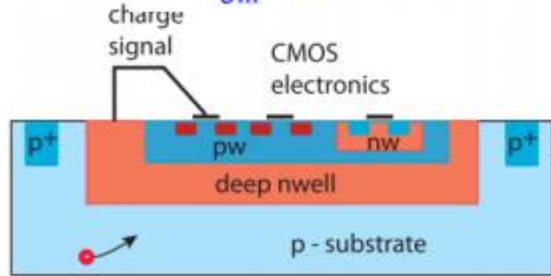
JSI Ljubljana Slovenia

Depleted MAPS/HVCMOS offer an alternative to hybrid sensors as timing detectors – aiming for better S/N

$\tau \propto \frac{C}{g_m}$, $ENC_{thermal} \propto \frac{kTC}{g_m}$ compensated by power (g_m)

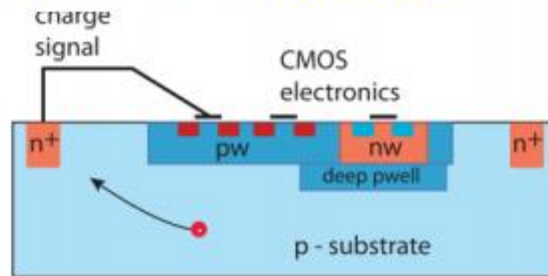
(*there are several talks on D-MAPS and CMOS D-L. Pohl, W. Snoeys, P. Riedler*)

taken from N. Wermes



- Large electrode: $C \approx 300\,\mathrm{fF}$
- Strong drift field, short drift paths, large depletion depth
- Higher power, slower
- Threshold $\sim 2000\,\mathrm{e}^-$

σ_{wf} - small, σ_j, σ_{lf} - large



- Small electrode: $C \approx 3\,\mathrm{fF}$
- Low analogue power
- Faster at given power
- Difficult lateral depletion, process modifications for radiation hardness
- Threshold $\sim 300\,\mathrm{e}^-$

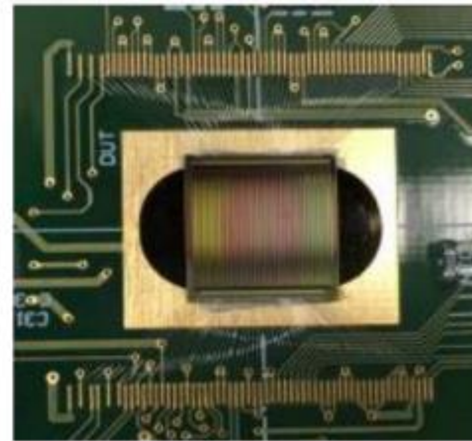
σ_{wf} - large, σ_j, σ_{lf} - small

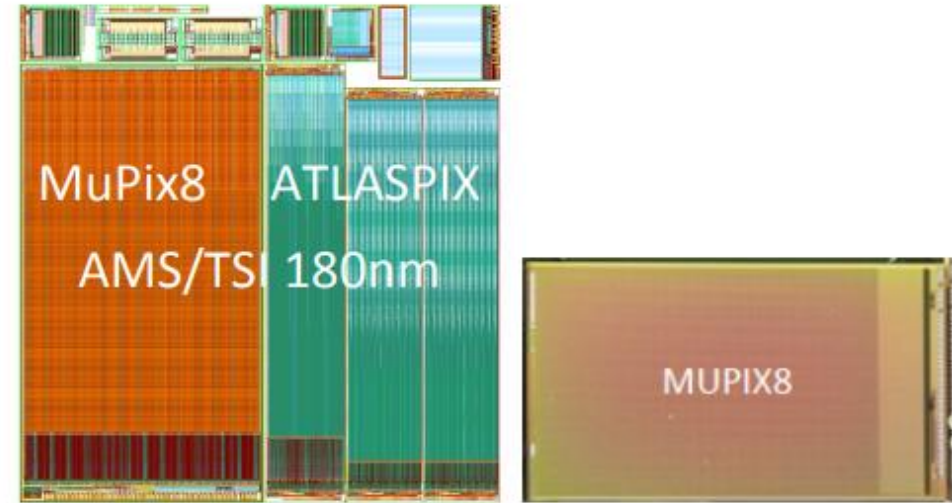
The limits set for the planar detector are still valid:
CACTUS D-MAPS *(Y. Degerlia et al. JINST 15 (2020) P06011)*

LFoundry-150 nm, high resistivity substrate
thickness=100 μm-> ~7500 e for m.i.p.
simulated channel noise ENC~ 300 e
τ_r~1 ns -> σ_j ~ 50 ps
σ_{wf}~0 (pixel of 1x1 mm^2)
σ_{lf}~50 ps

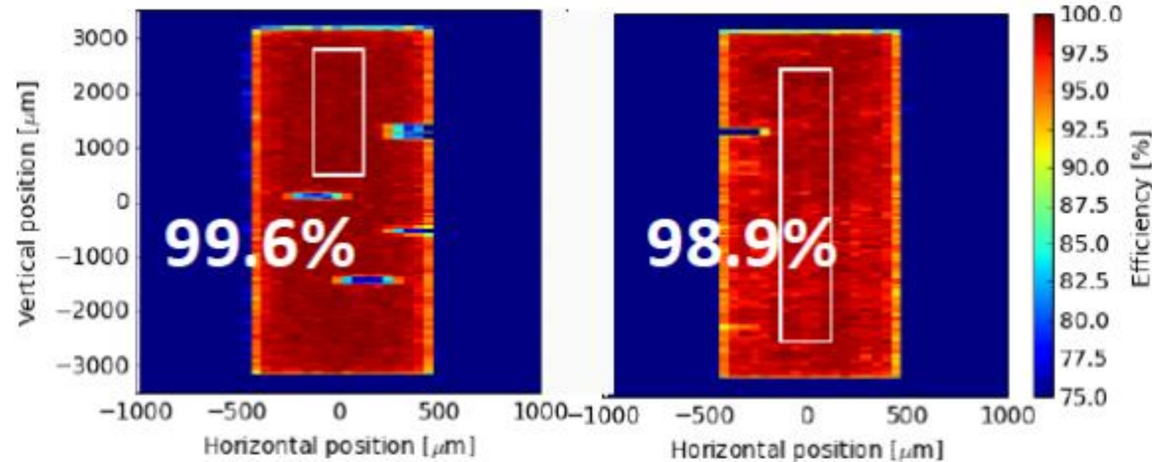
σ_t~70 ps -> also aimed by the designers (60 ps)

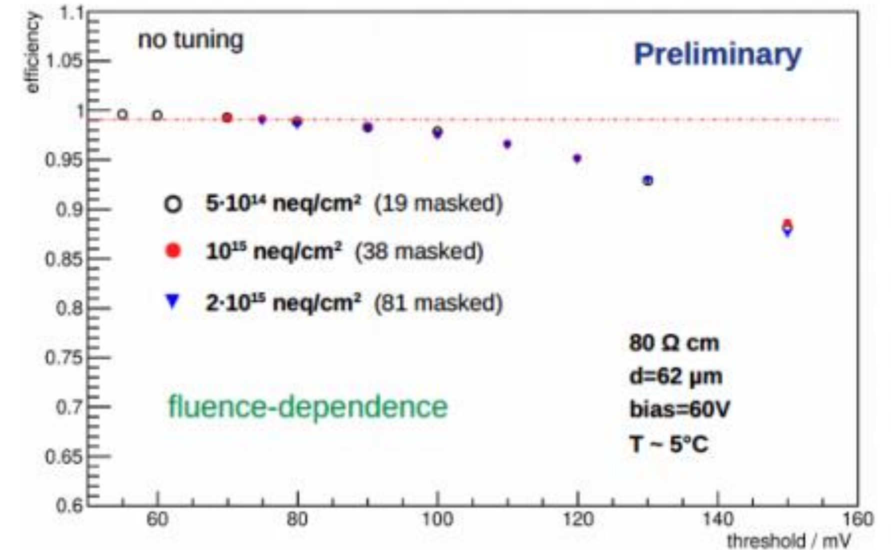
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)





Efficiency non-irradiated after 1.14 E15 n_{eq}/cm^2



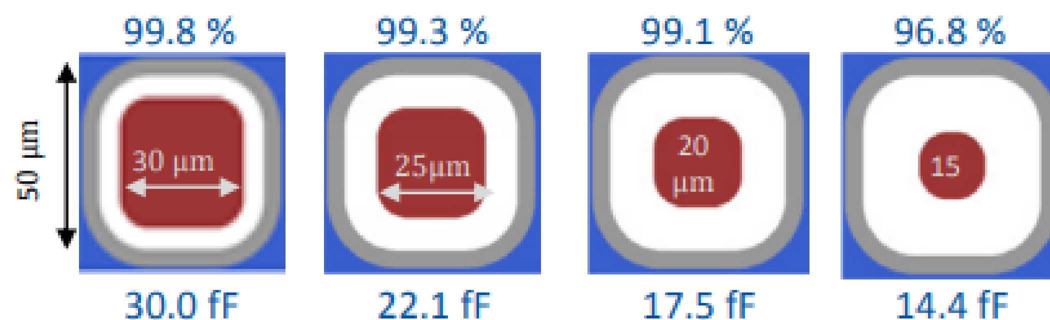


T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

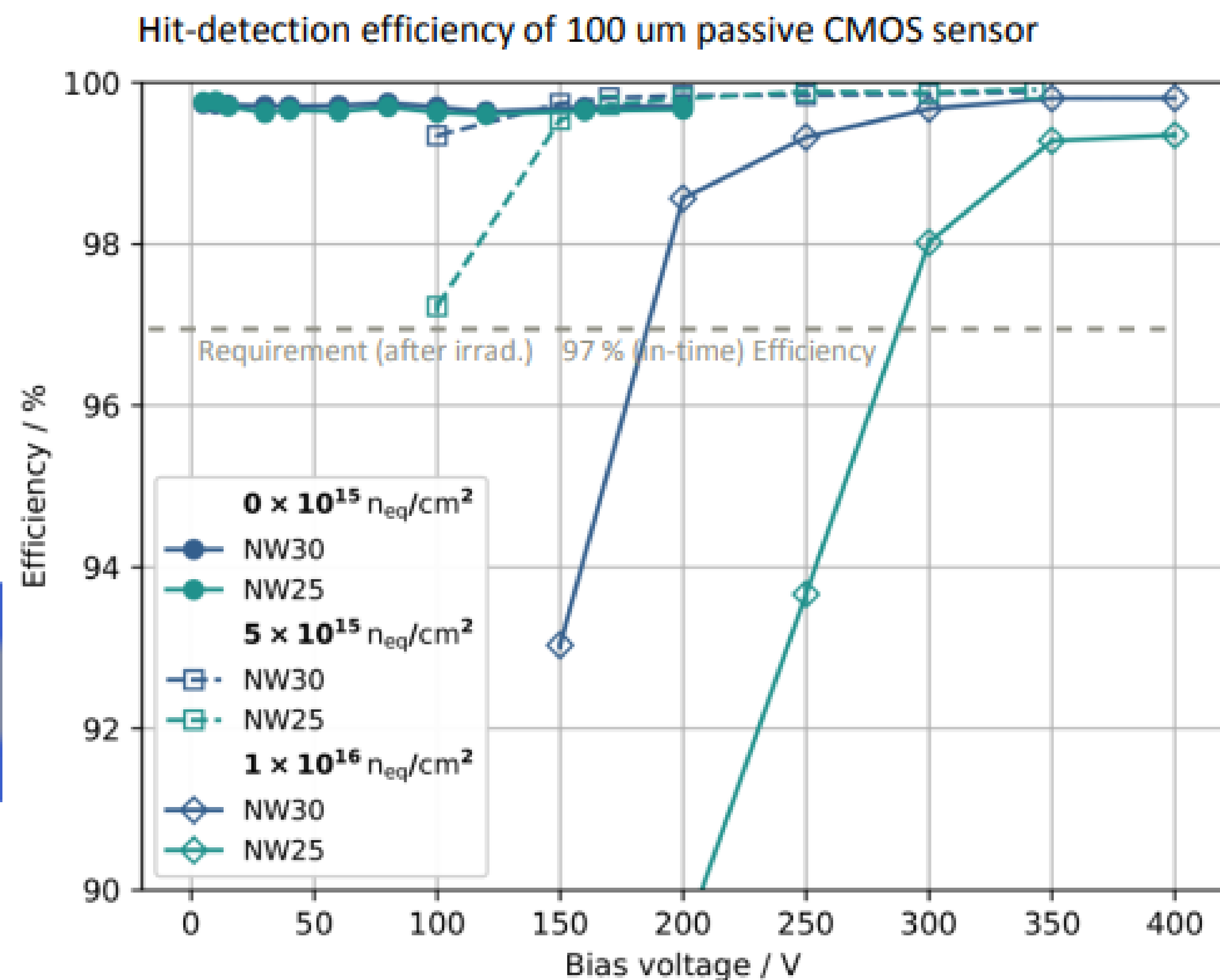
Courtesy I.Peric and A. Schoening

EFFICIENCY MEASUREMENT: PIXEL SENSOR

- R/O chip parameters:
  - Linear FE of RD53A
  - Threshold: ~1000 e
  - Noise occupancy: < 10^{-6}
- Before irradiation: > 99.5 % at 5 V only
- $5 \times 10^{15}\ n_{eq}/cm^2$: > 99 % efficiency (@ 100 V)
- $1 \times 10^{16}\ n_{eq}/cm^2$: > 99 % efficiency (@ 400 V)
- Mean efficiency and capacitance for different fill-factors @ 400 V:



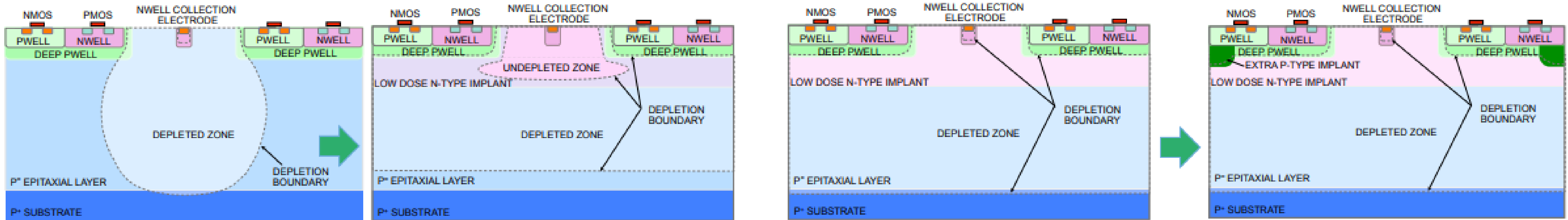
- Capacitance measurement in: https://doi.org/10.1088/1748-0221/16/01/P01029



Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness... and better efficiency, especially for thin sensors

Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field...



Standard, not fully depleted (ALPIDE)

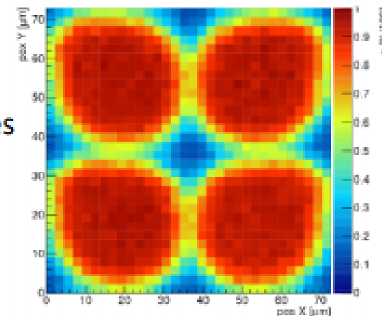
Not fully depleted at low reverse bias

Depletion at higher reverse bias (MALTA1, MONOPIX)

Further improvements by influencing the lateral field

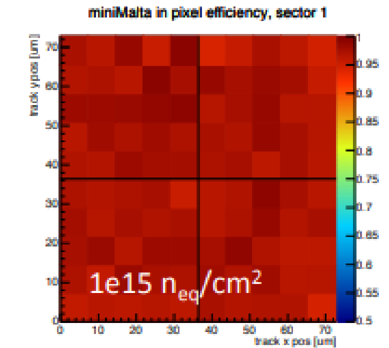
Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96
Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

Efficiency drop at pixel edges after irradiation for 36.4 x 36.4 μm^2 pixel needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987

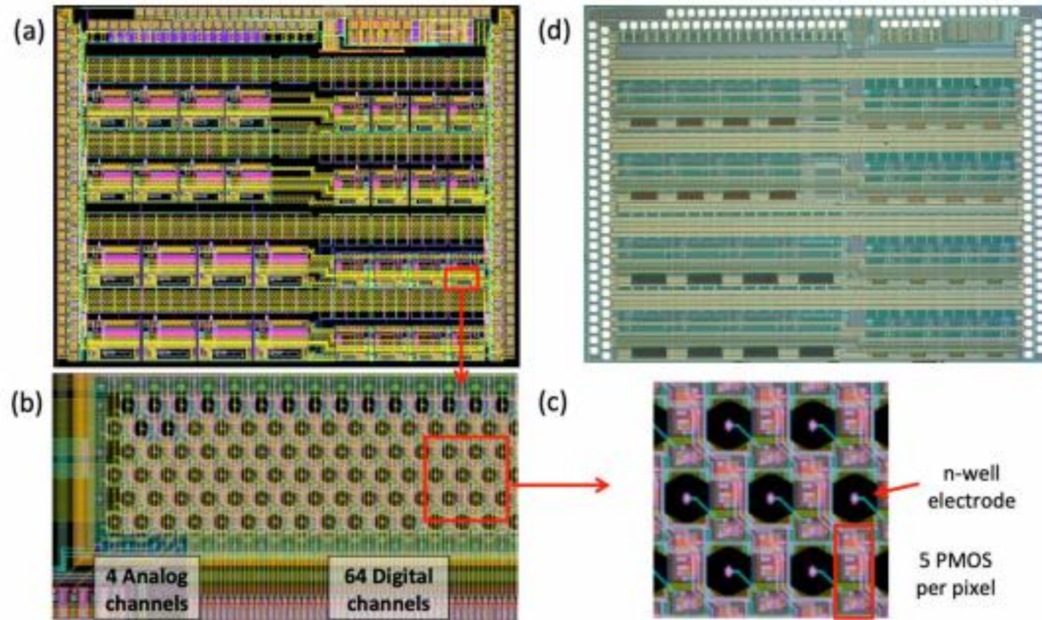


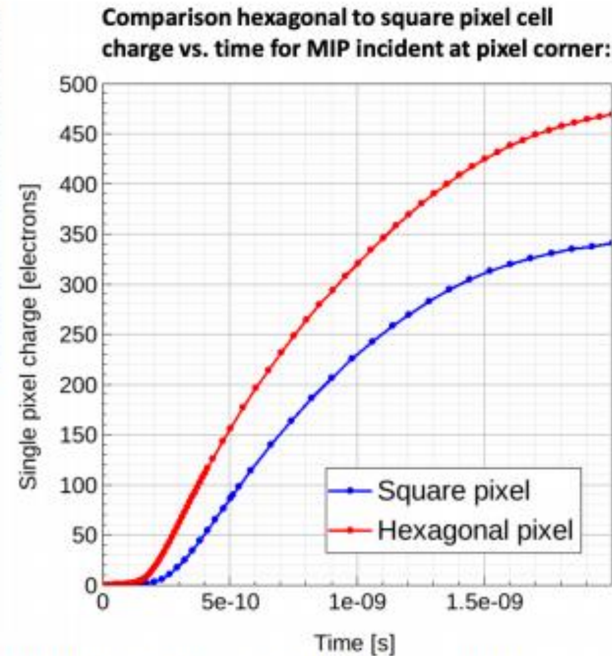
Other similar developments for fast charge collection and depletion:

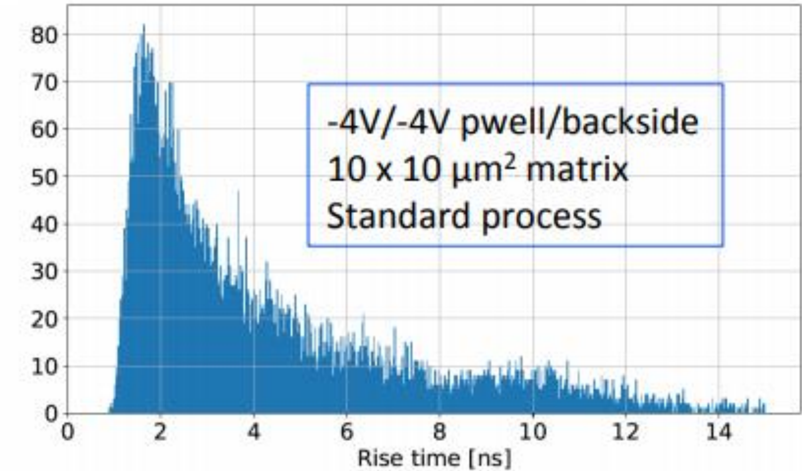
T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027...
S. Kawahito et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

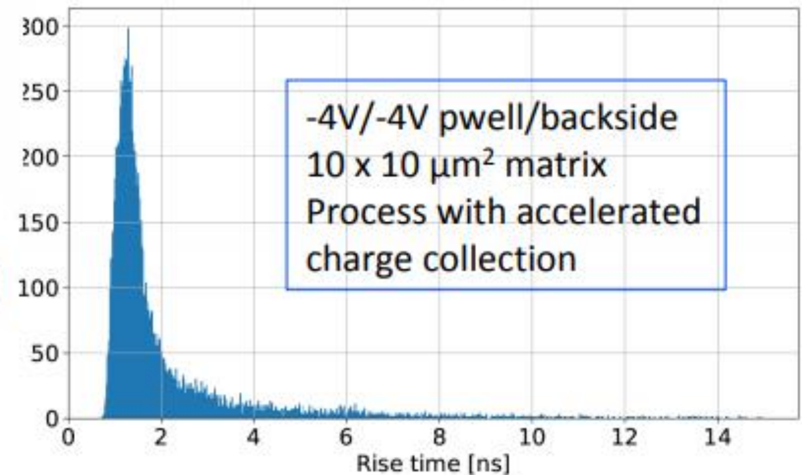
FASTPIX ATTRACT project: ^{90}Sr Risetime distributions

EP R&D









T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461 (ATTRACT: INFN, Ritsumeikan University and CERN)

E. Buschmann, D. Dannheim, K. Dort, M. Muenker

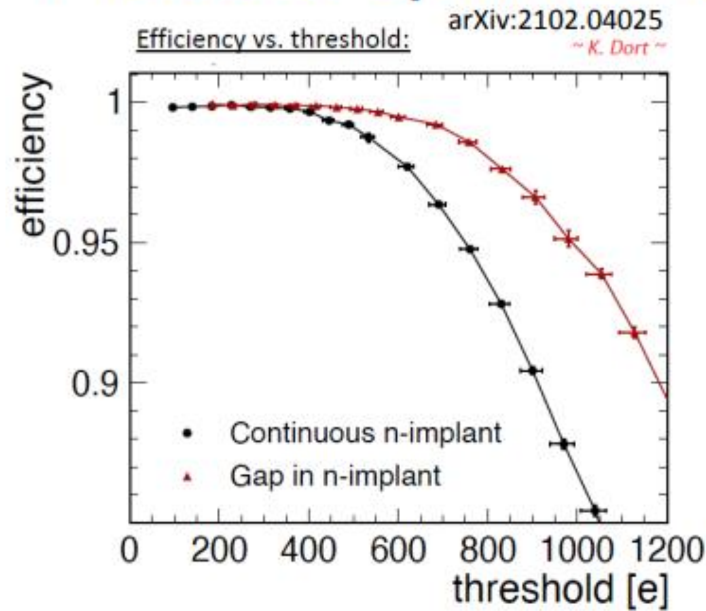
Direct relation between charge collection and process variant (TowerJazz 180nm)

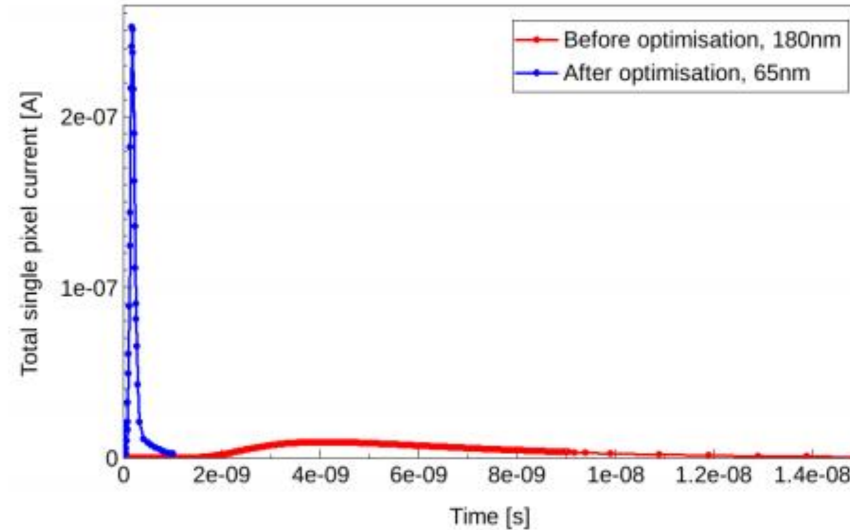
Significant impact even at very small pixel pitch

Hexagonal pixels

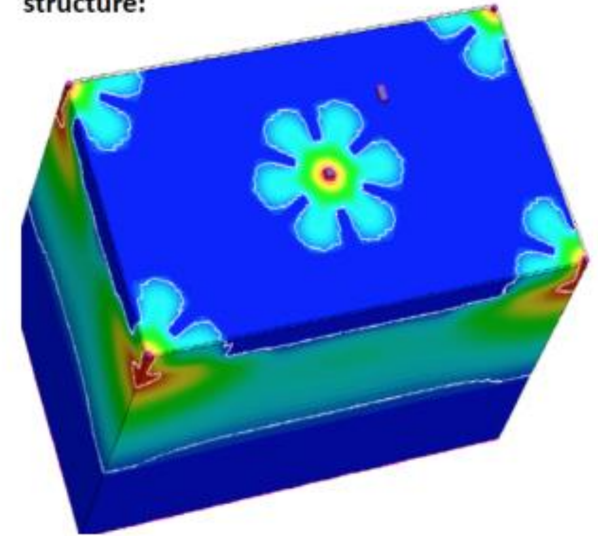
- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit to remain on Manhattan layout

Process optimizations for small collection electrode





Example of complex 3D TCAD structure:

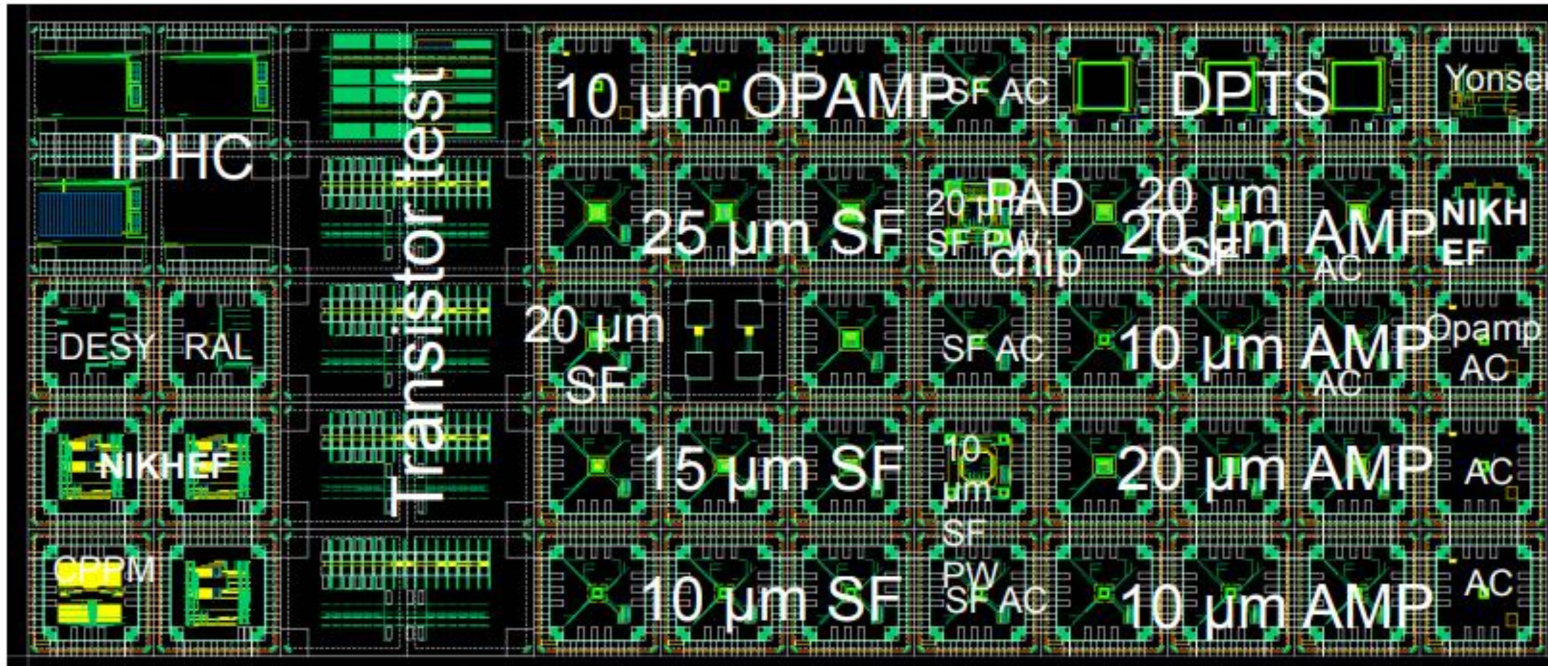


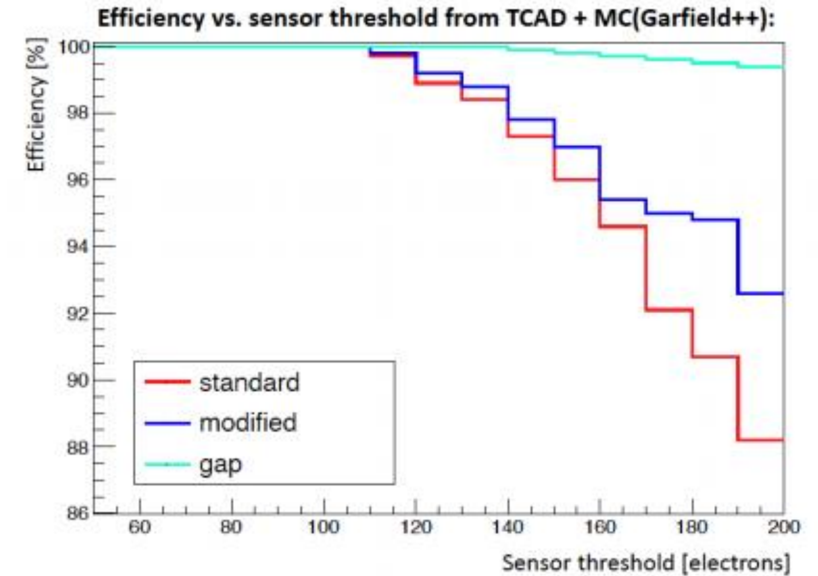
- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker's CERN EP detector seminar

EP-RD WP1.2 TPSCo 65 nm

EP R&D





Jan Hasenbichler

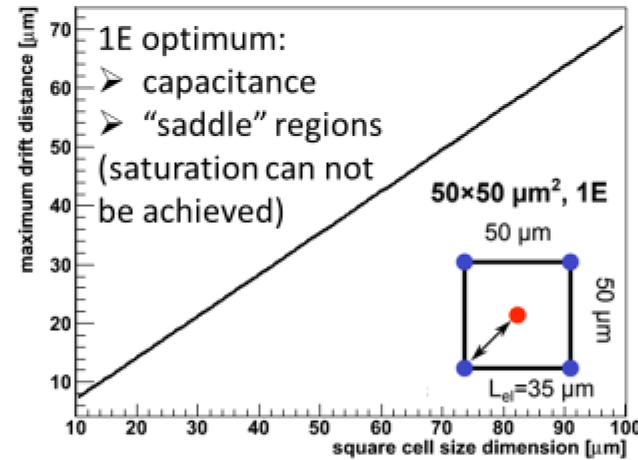
- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Significant effort from participating institutes, also financially
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- Converged with 4 splits of 3 wafers, back from foundry beginning of June
- Process modifications even more needed due to thinner epitaxial layer, hopefully in a similar position as on 180nm process

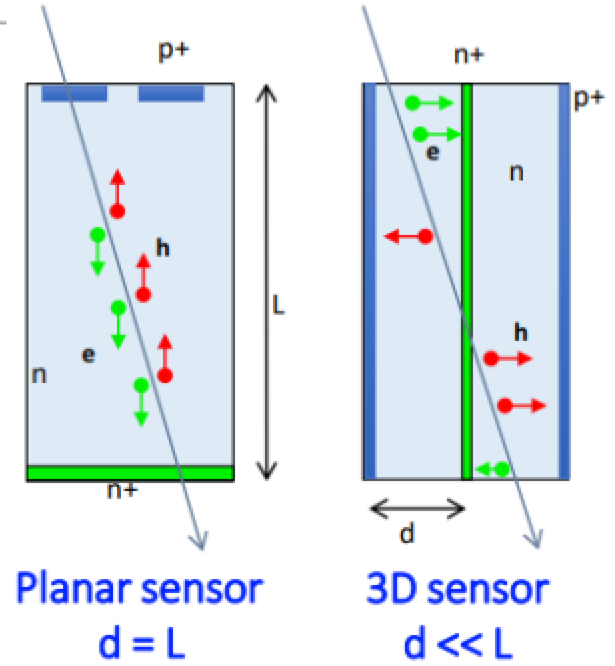
JSI
Ljubljana
Slovenia

3D detectors for timing applications

3D technology as timing detectors:

- They have fill factor ~100% (inclined tracks)
- The radiation tolerance of small cell size devices is large (for signal) and allows operation at higher bias voltages (next slide)

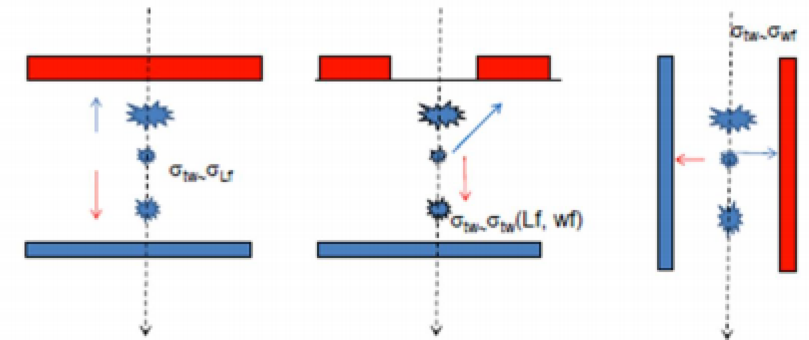




S. Parker et al, Nucl.Instrum.Meth.A 395 (1997) 328-343

But/However:

- 3D can be fast – ☺ short drift distance, but ☹saddle regions in the field
- the weighting field – hit position - will impact the signal ☹
- they can be thicker as Landau fluctuations play a minor role
- the capacitance will be much larger (hence noise and the jitter) particularly for thick sensors
- Lower operation voltages than for planar detectors (LGAD) and possibly lower current ($I_{LGAD}=G\cdot I_{gen}$) result in smaller power dissipation

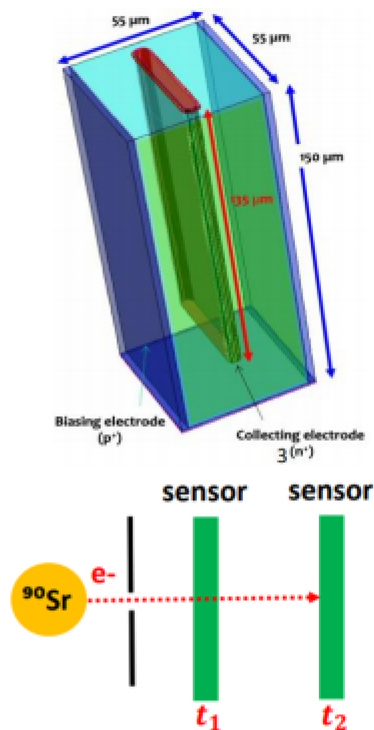


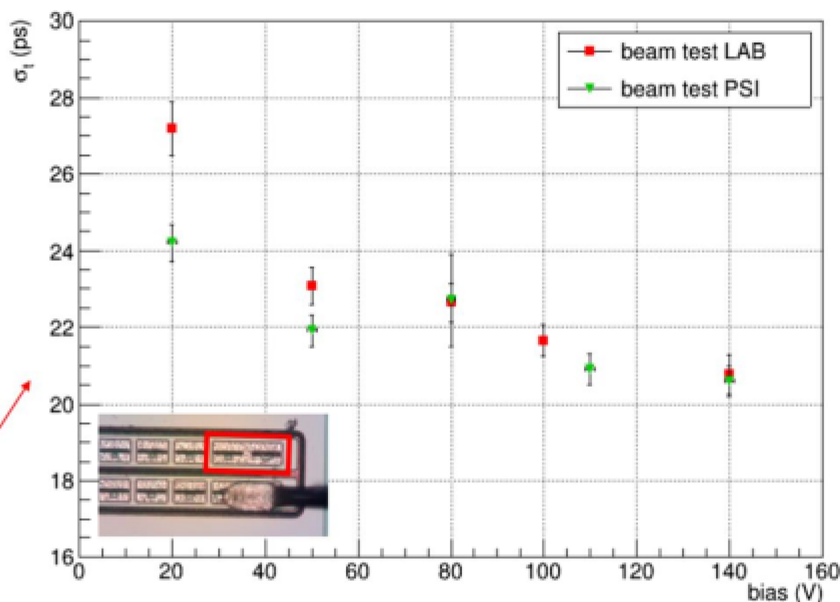
Trench - 3D detectors

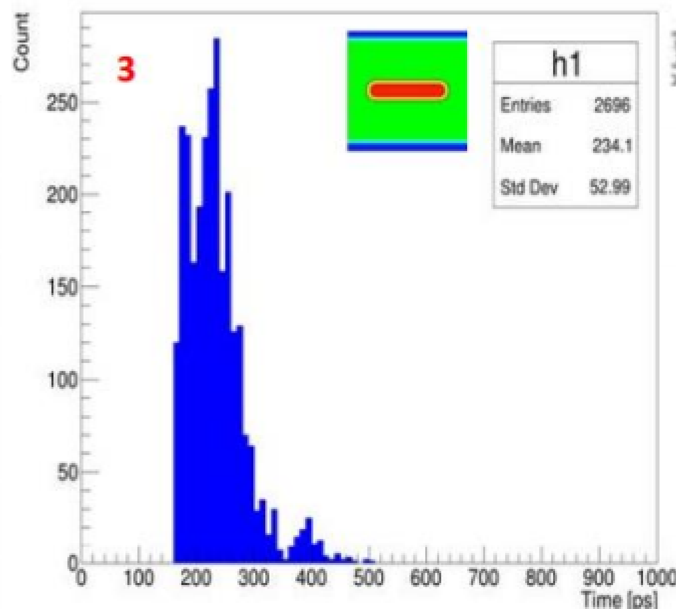
JSI Ljubljana Slovenia

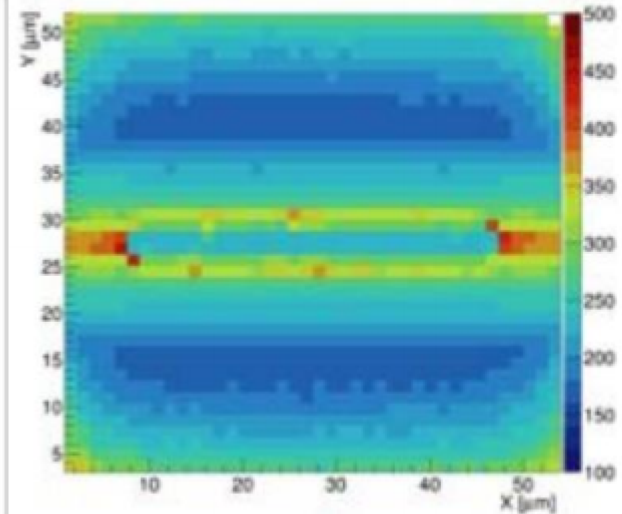
TimeSPOT

A. Lampis, 16th TRENTO workshop, 2021
M. Garau, 16th TRENTO workshop, 2021









The time resolution was found to be dominated by FE electronics σ_j ~18 ps

The σ_{wf} (intrinsic time resolution) of was found to be ~14-15 ps with accurate analysis **~10 ps.**

The tails in distribution due to low field regions in the space between the pads.

The reduction cell size may not improve the time resolution σ_t as the σ_{wf} may not be the limiting factor to the total time resolution.

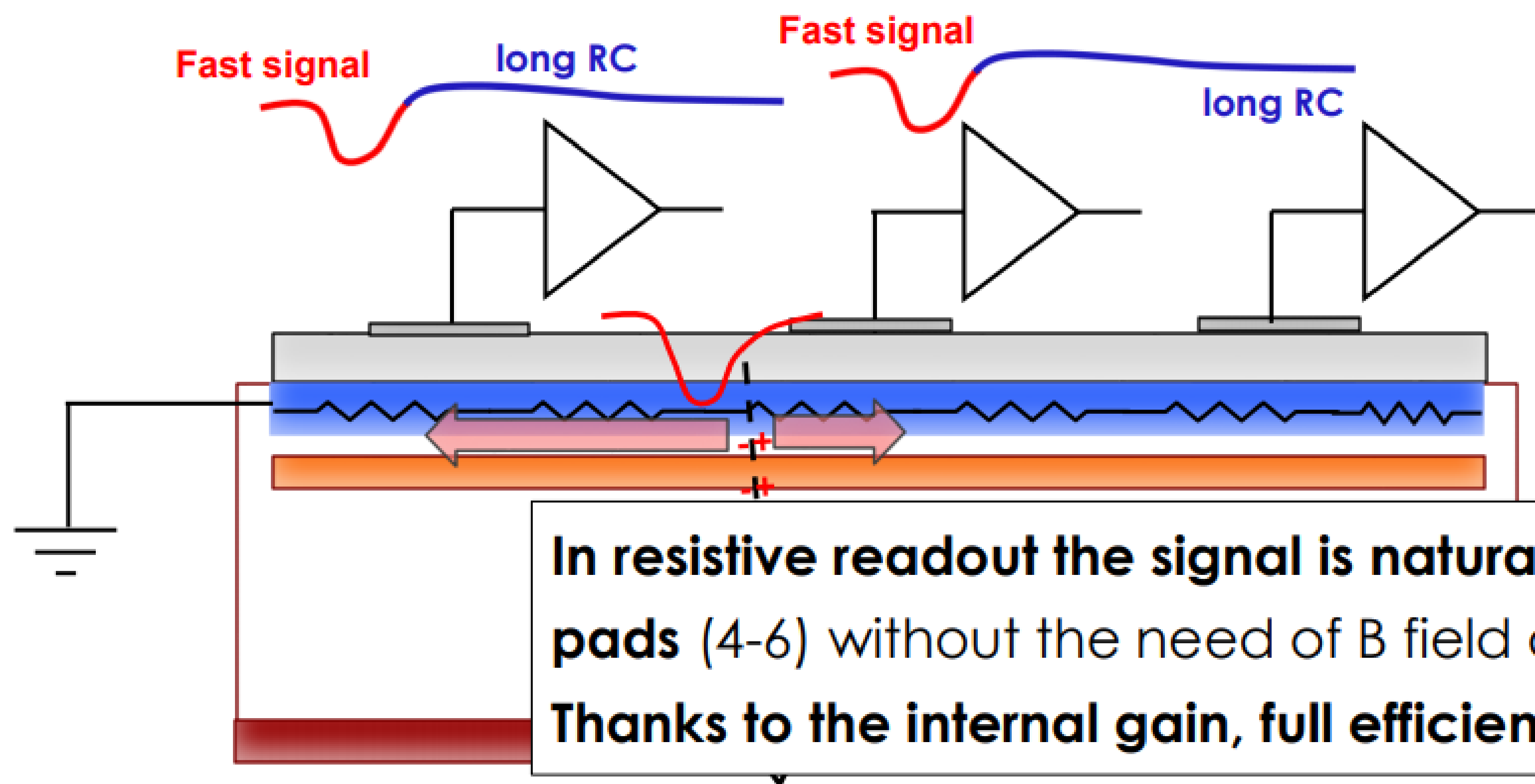
around 15 ps better time resolution than for similar cell size with 3D-columns.

Outlook for the future – σ_t=10 ps goal

- Small cell size 25x25 μm^2 /25x50 μm^2 required for position resolution and high rates would allow also hit time resolutions close to 10-15 ps.
  - the column width reduction ~10 μm to <5 μm (reduction of capacitance, improvement of S/N, reduction of the jitter/power and increase of fill factor) – in the future column widths as low as ~1-2 μm may be possible allowing possible multi-cell configurations.
  - improved aspect ratio of Deep Reactive Ion Etching (DRIE) is crucial -> current aspect ratio of 25 should be improved, particularly for thicker detectors that may be required to improve the signal required in severe radiation hard environment - larger clusters become the problem.
  - The choice of design (Trench/Column) will be a matter of optimization σ_{wf} vs. σ_j vs. fill factor and there is no clear answer to which is better (it depends on application)
- New ideas will be important and may become possible and/or mature over the years:
  - "Marriage" of LGADs and 3D (either by trench filling, careful substrate selection with small interelectrode distance allowing charge multiplication without special processing of gain layer)
  - "Marriage" of CMOS and 3D.
- The scalability is a question for the producers:
  - single sided processing is a major step forward, the next is move to >=8" wafers, where thicker wafers are required
  - Yield improvement , robustness of the designs are key
- Operation conditions: cooling down as low as possible improves the performance in all respects not only power dissipation/leakage current, but also in speed and possible charge multiplication

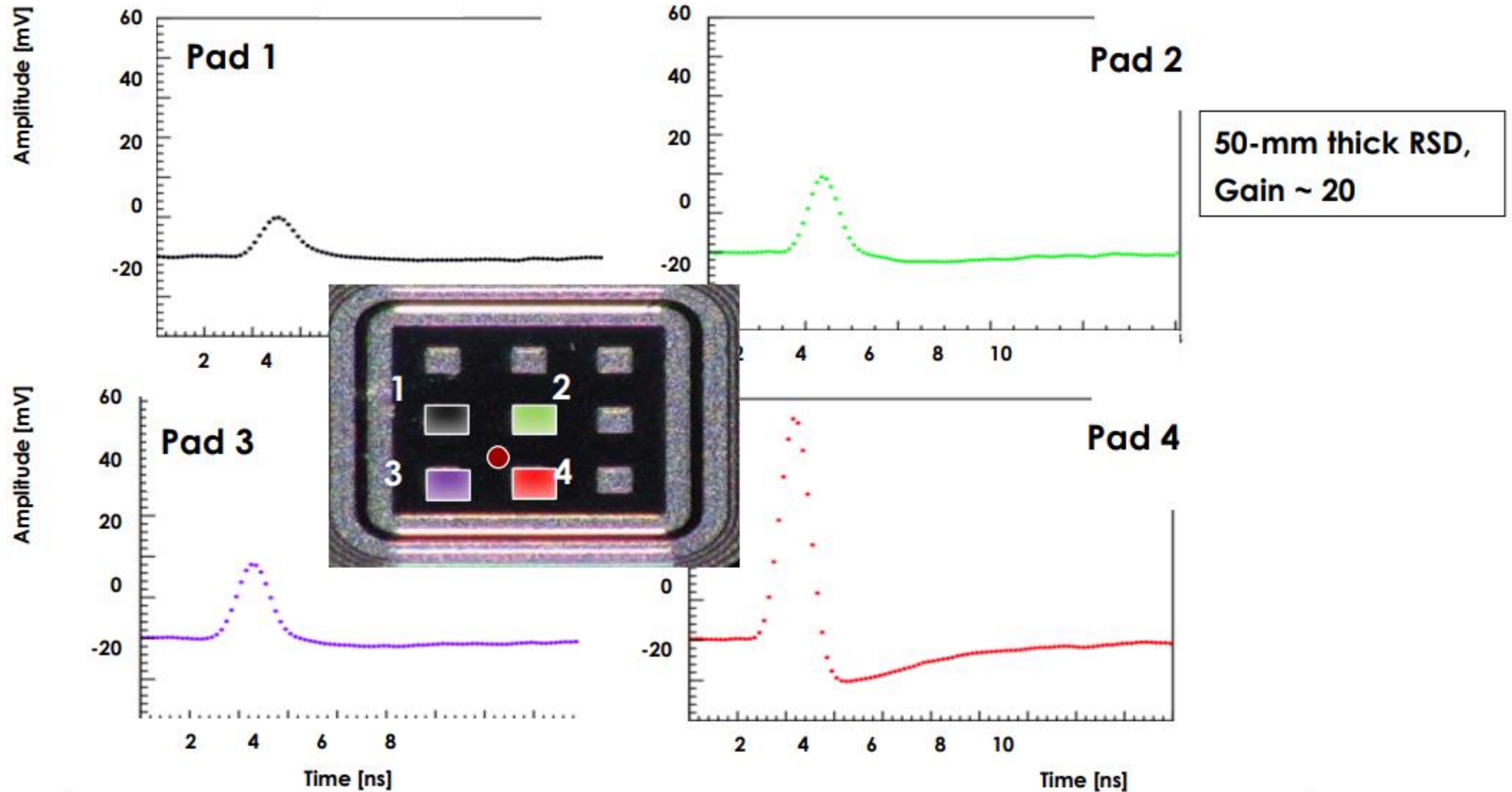
Second design innovation: resistive read-out

- The signal is formed on the n+ electrode ==> no signal on the AC pads
- The AC pads offer the smallest impedance to ground for the fast signal
- The signal discharges to ground



In resistive readout the signal is naturally shared among pads (4-6) without the need of B field or floating pads
Thanks to the internal gain, full efficiency even with sharing

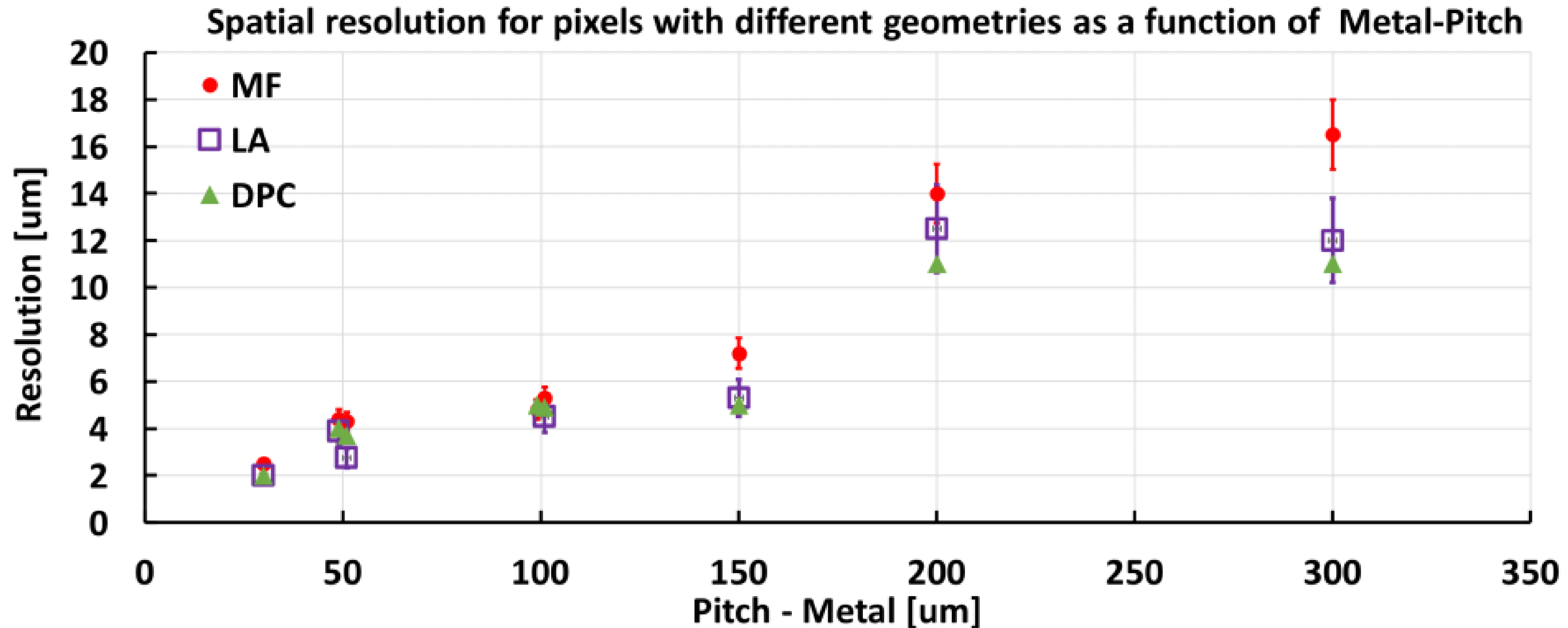
Example of a signal in an RSD



50-mm thick RSD,
Gain ~ 20

The laser is shot at the position of the magenta dot: the signal is seen in 4 pads

Summary of RSD position resolution

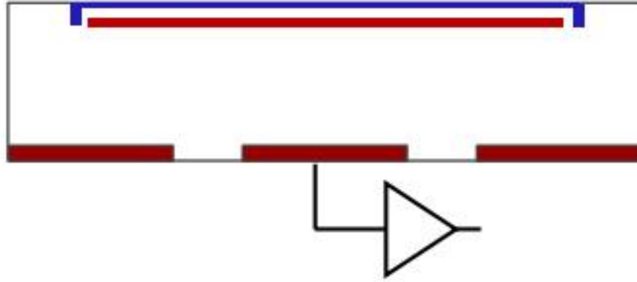


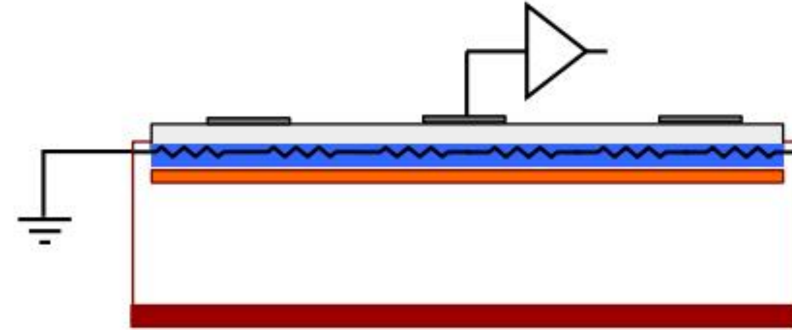
RSDs reach a spatial resolution that is about 5% of the inter-pad distance

➔ ~ 5 µm resolution with 150 µm pitch

RSDs have the "usual" LGAD temporal resolution of 30-40 ps

Present results & short term evolutions - II



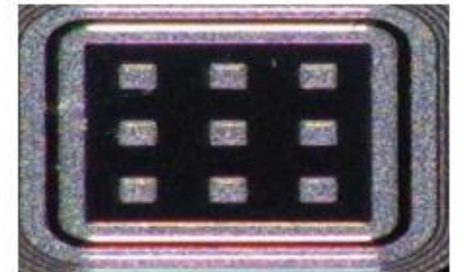


i-LGAD

- p-side segmentation
- Signal in a single pixel
- 100% fill factor
- Thin i-LGAD with single side processing under development (using trenches, spring 2021 @ CNM)
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied

RSD: resistive readout

- Signal in many pixels
- 100% fill factor
- Excellent position resolution:
  ~ 5 μm with large pixels
- Temporal resolution (50 μm) : 35-40 ps
- Rate ~ 10-50 MHz
- Rad hardness: to be studied



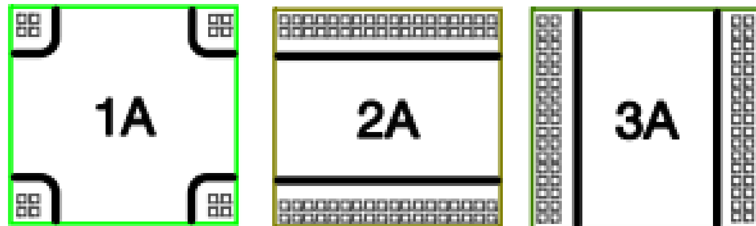
Presentation plan

- Towards more density
- Towards faster sensors
- Towards bigger sensors
- Conclusion

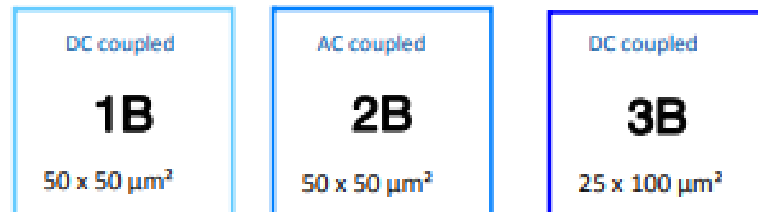
STITCHING

- Sensor size > reticle size
  → Stitching needed
- Additional rules for stitching (no fine-pitch)
  → Not too relevant for sensor designs
- Different blocks:

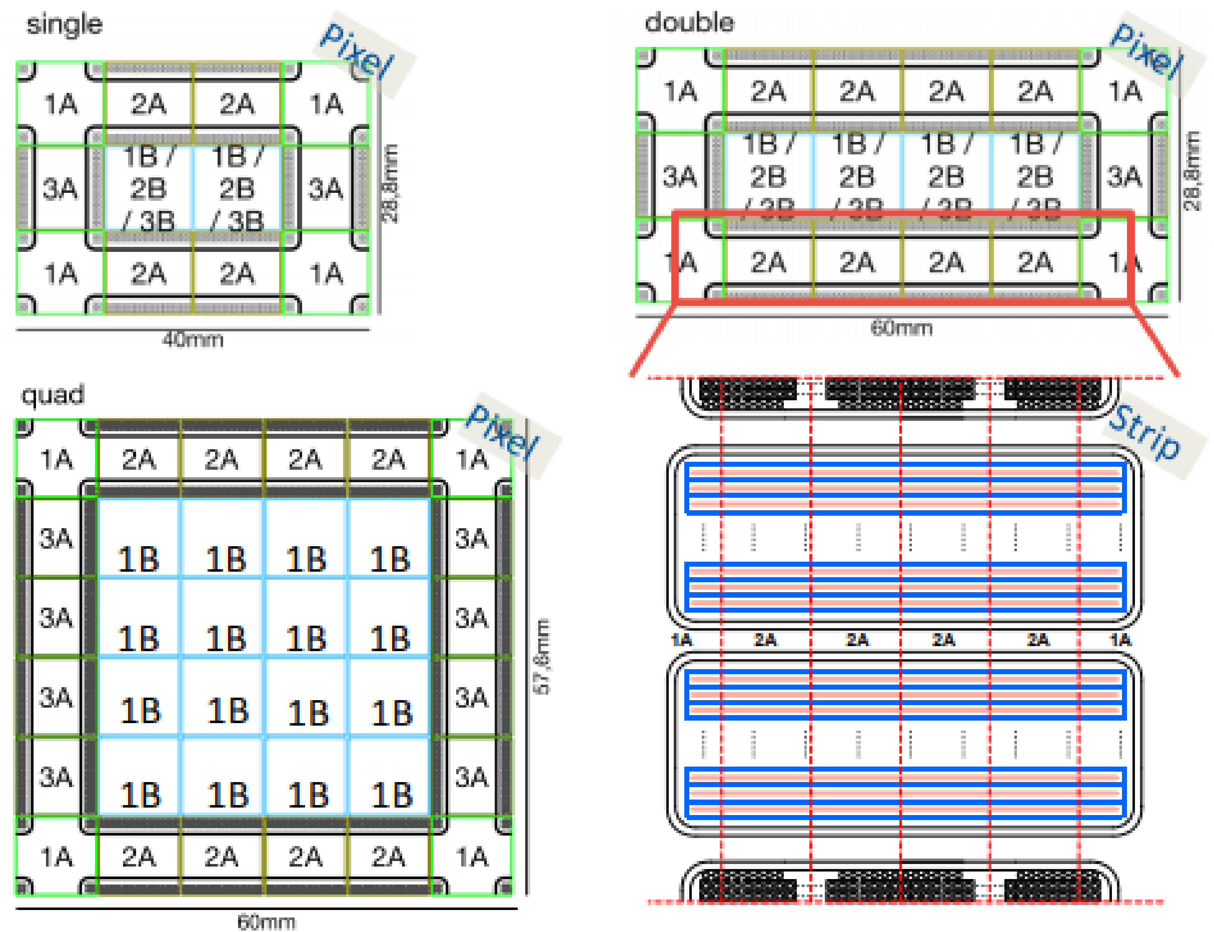
Edge blocks with guard rings, strip sensors and test structures



Center blocks with different pixel flavors

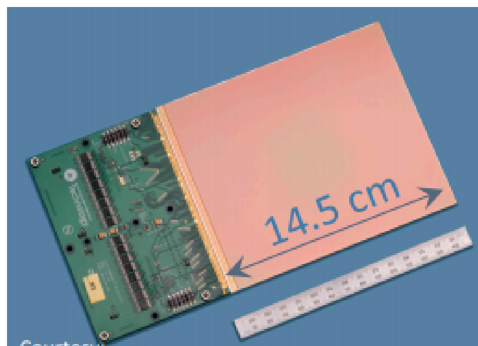


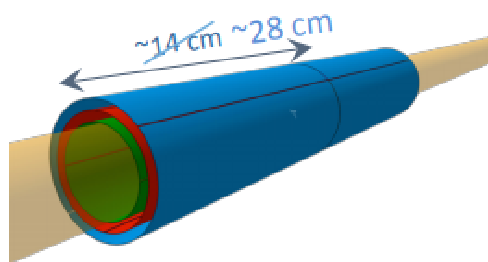
- Different configurations possible
  → arrange and repeat blocks in different order

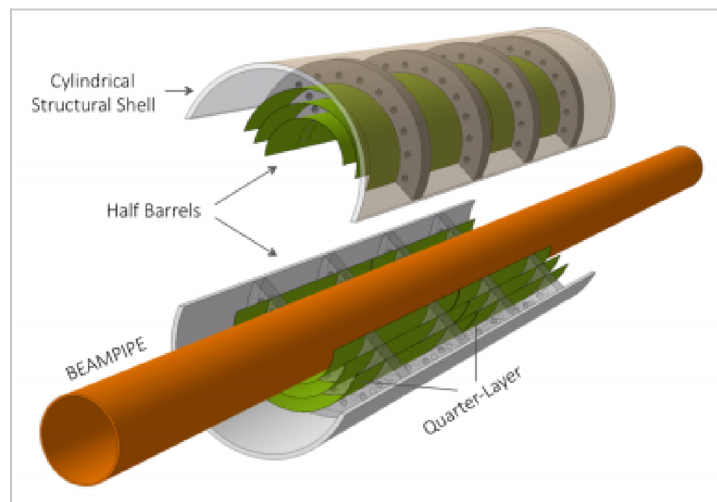


Stitching for better integration, lower mass and constructing larger areas

Exploiting flexible nature of thin silicon and stitching





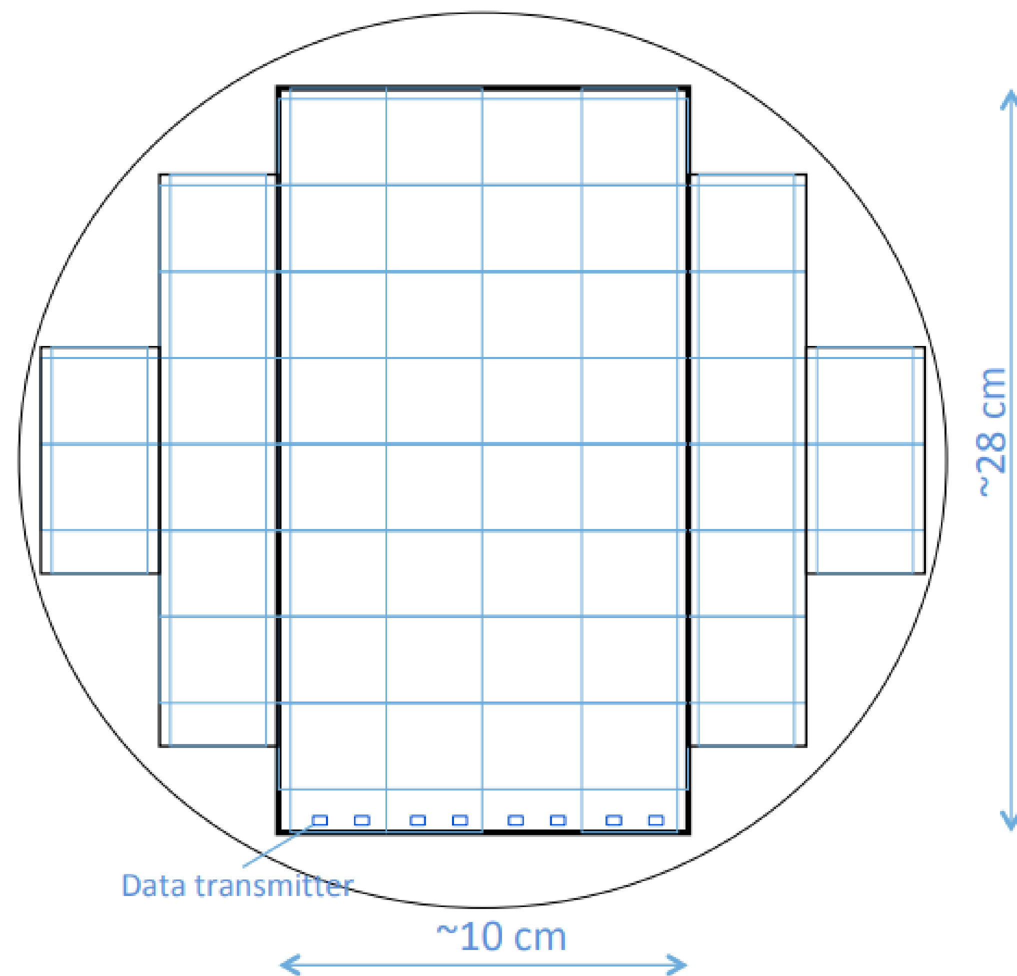


Truly cylindrical vertex detector
New ultra light barrel in LS3 0.05% X/X0 per layer
ALICE-PUBLIC-2018-013

Motivated by lower material budget

Of general interest to cover large areas
Stitching details and bending tool
-> P. Riedler's presentation

Work under the assumption of a wafer-scale sensor, ~28 x 10 cm^2, to be revised if needed
Power budget ~ 20 mW/cm^2 for ~2.5 $Mhit/cm^2/s$



Stitched sensor: challenges

Power consumption: only considering the matrix, pixel size 200 μm^2 (~ 15 µm pixel pitch on a hexagonal grid) 1nA/pixel = 0.5 mW/cm^2

Dynamic hit-rate related power density proportional to column height (28 cm, on average 14 cm x CV^2) and hit rate

- First simulations (parasitic extraction) encouraging dynamic power consumption and possible hit rates: most optimistic values (not on finalized design !!!!) around 25 mW/cm^2 @ 100 $Mhit/cm^2/sec$
- Avoid distribution of a clock over the matrix (150 – 200 mW/cm^2 for 40 MHz)

Static leakage not negligible at all, analog power determined by sensor Q/C (slow front end ~10-20 nA)

Power distribution:

- Additional thick metal(s) for power distribution to contain voltage drop, otherwise 10's of $mV/mW/cm^2$
- Power regulation for uniformity
- Beyond 50 mW/cm^2 :
  - Power pads no longer only at the bottom, or
  - on-chip serial powering,

    interesting even for lower hit rates, for a single point connection of power/data/slow control

    1mW/cm^2 corresponds to 280 mA…

Yield:

- Conservative stitching rules represent a significant area penalty, need to find ways to regain density
- Power regulation for uniformity but also segmented with current limitation to protect against shorts

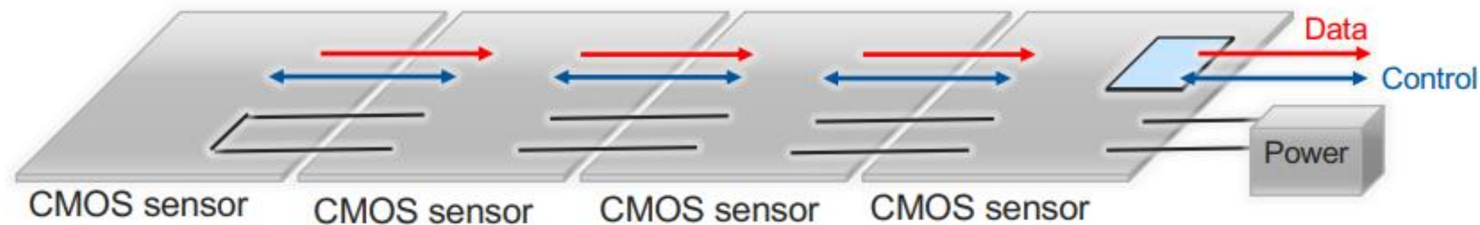
Very large chip:

- One column ~ 2^{14} pixels, extract hit info with limited number of lines
- Need digital on-top design and verification

Larger system aspects

Consider aspects for integration into larger systems where areas much larger than wafer sizes are needed and/or a modular approach is required, such as:

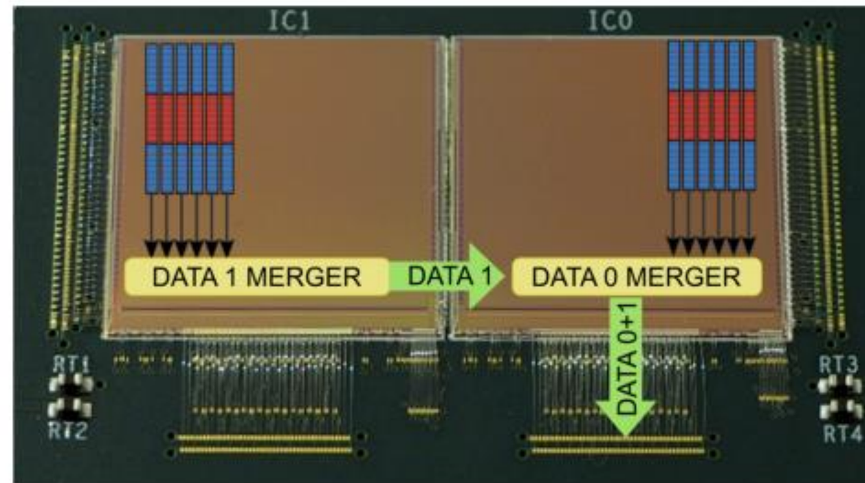
- Daisy-chain chips (high speed chip to chip connection, power connection)
- Serial powering
- Digital back-end to move time-stamped serialized information and integrating specific requirements (e.g. track trigger, time measurement, etc.)

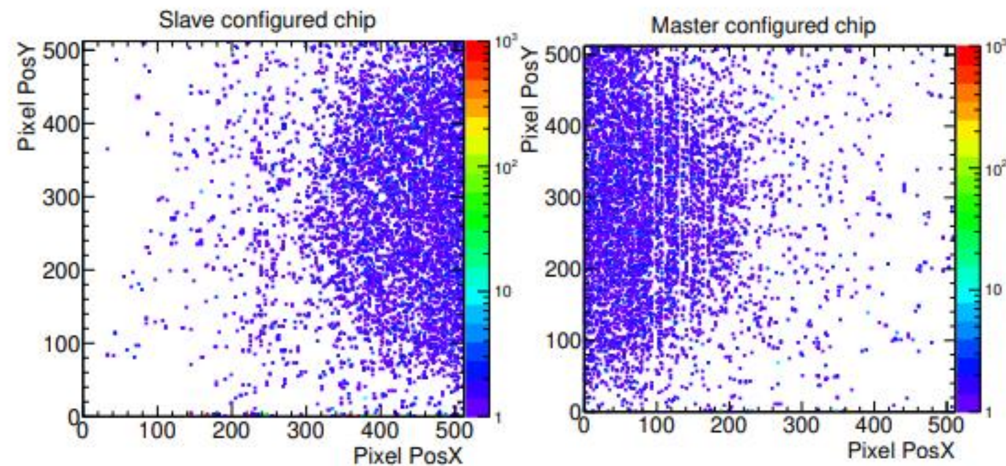


- modular approach, compatible with data volumes
- compact layout with high level of integration into the sensors
- minimizing connectivity using chip-to-chip transfer
- reduce material budget
- optimized assembly process

Example: MALTA chip-to-chip communication

- Source tests to validate data transfer from one chip to the other (Sr90 source)
- High speed signal routing from sensor to sensor via edge pads from (GHz)
- All measurements done with same exposure time; white lines are masked double columns





Transfer of data/power from one chip to the next successful, now being extended to 4-chip boards.

Presentation plan

- Towards more density
- Towards faster sensors
- Towards bigger sensors
- Conclusion

Conclusion

- **Towards more density**
  - Technology nodes go on decreasing (down to 5 nm)
  - We reached the limit for planar structures, and new technologies are developped exploiting the 3rd dimension: FinFet and GAA transistors.
  - We have no sufficient information on the radiation tolerance of these new technologies
  - 3D integration: Chip2Chip, Wafer2Wafer, Chip2Wafer
  - µbumps of 1µm with 2 µm pitch
  - Muti-layer integration of complex systems

Conclusion

- **Towards faster sensors:**
  - 4D tracking is essential for future HEP detectors
  - 10 ps is impossible for classical planar sensors
  - 3D detectors (column and trench) are good candidates: σ_t of 20 – 30 ps and very good radiation tolerance but high detector capacitance.
  - LGAD also good candidates, σ_t of 20 – 30 ps for thin detectors are high reverse bias. Rad hard up to 3 x 10^{15} n_{eq}/cm^2.
  - MAPS are a promising solution after sensor optimization with a simulated σ_t of 50 ps. Optimised MAPS are rad hard up to 1 x 10^{15} n_{eq}/cm^2.
  - RSD are also good candidates, with excellent fill factor (100%) and spatial resolution (5µm with a pitch of 150 µm) and σ_t of 30 – 40 ps. Radiation tolerance are however still to be studied

Conclusion

- **Towards bigger sensors:**
  - R&D stitched sensor of 28 cm x 10 cm
  - Flexible and bent sensors. Very low material budget
  - Many challenges, mainly:
    - Power distribution
    - Yield
  - Chip 2 Chip data and power transmission are realized and successfully tested.

- **General Comment**
  - Detectors design are becoming more and more complex and requires a digital-on-top approach with an increasing verification effort.
  - It takes years to develop the full detector.
  - There is a need for an expert team of designers, complemented with device/TCAD/Monte-Carlo experts. It takes years to train these people and our community does not sufficiently preserve critical mass and know-how for this activity.

Thank you for your attention