# Time Distribution System Proposal for the Hyper-Kamiokande Experiment's Far Detector and IWCD

LPNHE - INFN Roma

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## 1 Introduction

A crucial information to reconstruct the Cherenkov ring associated with an event is the arrival time of the light emitted in water of the Hyper-Kamiokande detector and registered by different PMTs. To achieve this goal a common time base has to be established and distributed to all the front-end (FE) modules of PMT readout electronics.

The time synchronisation precision is directly related to the event's reconstruction accuracy; therefore, great care must be devoted to this task to control all sources of errors and inaccuracies. The Hyper-Kamiokande experiment requires a time distribution jitter smaller than 100 ps RMS and the clock skew between front-end boards to be constant over any power-up and reset.

The time tag of each particle interaction needs to be in a format that allows its correlation with data collected by other experiments worldwide; for this reason the generated local time base has to be associated with the Coordinated Universal Time (UTC) with an accuracy of 50 ns or better. This absolute time tagging will also be used to identify the events generated in the detector by the particles sent from the J-PARC accelerator. Along with the time synchronisation some "critical information"

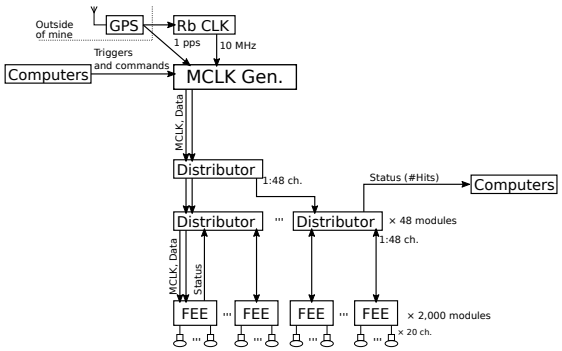


Figure 1: The timing and auxiliary transfer design overview.

like remote firmware FPGA updating stream and slow control data have to be transmitted by this subsystem hence a 100 Mbps or greater bandwidth bidirectional data channel has to be provided.

The basic experimental requirements relative to the time distribution system, as currently defined, are summarised in Table 1 while the conceptual block scheme is depicted in Fig. 1. The whole system can be subdivided into 3 main parts, as shown in the block scheme reported in Figure 2 which highlights also the envisioned positions of each of them and its sub-constituents.

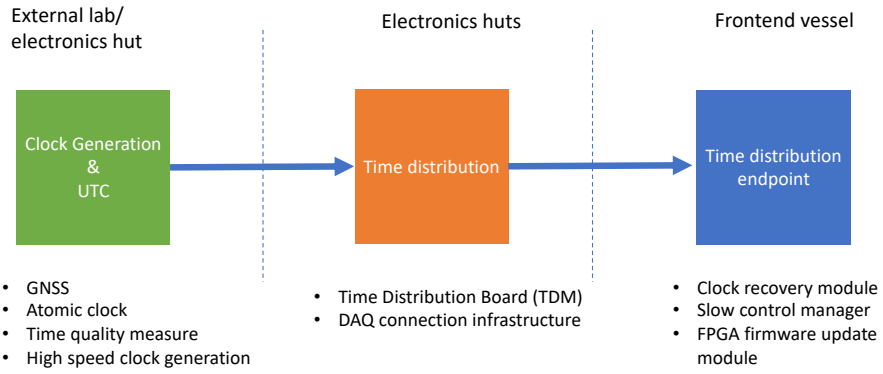


Figure 2: The block scheme that describes the 3 main time distribution sub-systems.

To guarantee the most stable and precise reference, the local time base originates in an atomic clock and a GNSS (Global Navigation Satellite System) working together to generate a Pulse Per Second (PPS) and a 10 MHz signals which are synthesised in the MCLK Gen to produce a 125 MHz output. This frequency is then distributed over different branches by means of Time Distribution Modules (TDM) and delivered to all the leaves represented by the FE modules using the so-called Time Distribution Endpoints or TDE. The PPS and the 10 MHz signals, along with information about the detected satellites, reach also a computer infrastructure to form the UTC time synchronous with the local time base and, from there, propagated to all the elements in the form of data packets to the DAQ system.

| **Time Synchronization Experimental Constraints** | |
|---|---|
| Total Jitter | $\leq$ 100 ps |
| Board to Board skew | fixed over any reset and power cycle |
| Accuracy to UTC | $\leq$ 50 ns |
| Critical Slow Control Data bandwidth | $\geq$ 100 Mbps |

Table 1: Current experimental requirements for the time distribution and synchronisation system.

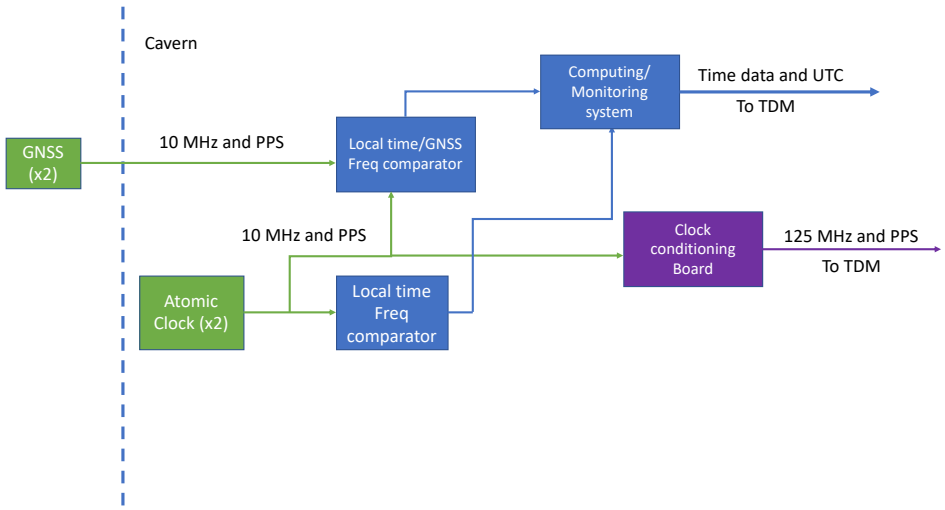


Figure 3: Detailed scheme of the clock generation section. The green boxes represent the clock and time generation instruments, the blue boxes represents systems used to monitor the stability and accuracy of the produced signals while the purple box is the conditioning box used before sending the signal to the electronics.

An R&D program to study the technologies capable of meeting the requirements described above has been established with the goal of highlighting the pros and cons of each proposed solution and selecting the most suitable for the experiment, to be used both for the far detector and IWCD. **This document describes this R&D program that has been performed by LPNHE and INFN, summarising all the efforts made over the last 2 years, and presents the solution we envision for the Hyper-Kamiokande experiment. In the last part the candidate final prototypes for the whole system are presented. They are already available for evaluation and tests.**

# 2 Clock Generation and UTC

## 2.1 General Concept

The base clock represents the foundation of the cadence delivered to all the detector electronics elements; therefore it must be very stable and precise to guarantee, at each end-point, a signal that still meets all the requirements in spite of the deterioration due to the distribution process. To achieve this goal many elements must work together as shown in the block scheme of Figure 3.

This section describes all these items.

## 2.2 Atomic Clock

The cadence generator technology that guarantees the best performance is the atomic clocks, but, currently on the market there is a vast range of instruments with different noise levels, stability characteristics and prices. The technologies selected and proposed for Hyper-Kamiokande are the Passive Hydrogen Maser (PHM) (microwave amplification by stimulated emission for radiation) and the Rubidium (Rb) standard which provide a 10 MHz clock and a PPS with characteristics summarised in Table 2[1].

**Individual performances of the clocks:** As evident from the Table 2, the Passive Hydrogen Maser shows much better performance that could go up to 2 orders of magnitude with respect to the Rubidium, both at short and long timescales. A more visual comparison involving Allan Standard Deviation (ASD) [1] can be found in Figure 4. The time when the curve reaches the minimum indicates

[1]The Passive Hydrogen Maser also provides a 100 MHz clock output.

| technology | Passive Hydrogen Maser | Rubidium |
|---|---|---|
| Frequency stability | $\sim 5 \times 10^{-13}$ @ 1 s | $\sim 2 \times 10^{-11}$ @ 1 s |
| equivalent jitter | 0.5 ps | 2 ps |
| Frequency drift | $\sim 5\times 10^{-15}$ @ 1 day | $\sim 1.6\times 10^{-12}$ @ 1 day |

Table 2: Passive Hydrogen Maser and Rubidium atomic clock characteristics.

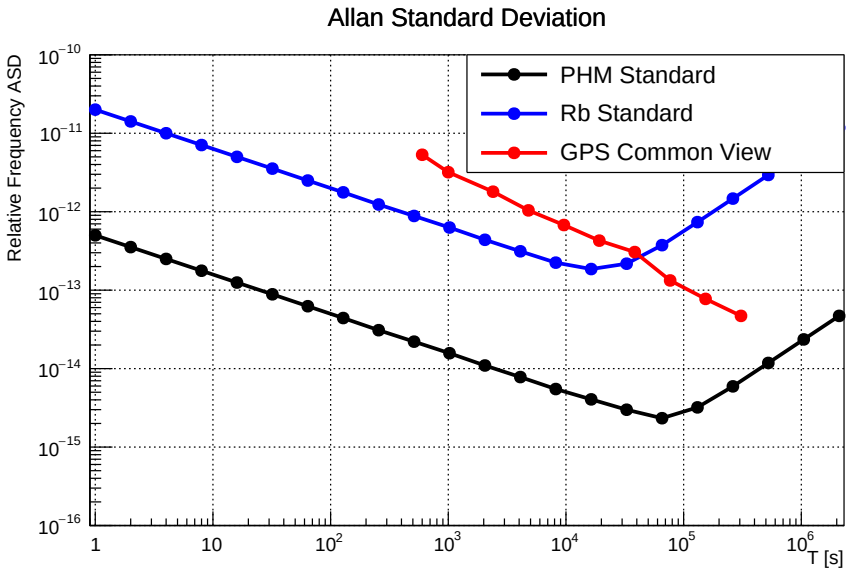


Figure 4: Allan Standard Deviation of the two clock generation systems selected and the GPS Single View performances [2].

the time at which long-term frequency drifts are dominating short-time fluctuations: it defines the timescale on which it would be useful to consider another system to monitor and correct for these drifts. The improved performances of the PHM compared with the Rb clock would allow to correct for the drift every day instead of every five hours, making the system more robust against possible malfunctions.

**Why using several clocks at the same time.** The system presented in Figure 3 depicts a set of two atomic clocks used to produce the 10 MHz clock and PPS signals. Such redundancy is necessary in order to recover from potential hardware failures on one of the two clocks and to assure minimum dead time. In addition, having two clocks would allow also a constant comparison between them to detect possible temporary malfunction or frequency drifts. Indeed, using frequency comparators on the two clocks would allow to detect whether one of the clocks is drifting in time or having sudden instabilities[2]. The candidate instrument to perform this task is the Keysight 5323A frequency counter [3] which measures the two inputs time distance periodically and saves data to a file, allowing offline timing corrections in the event reconstruction.

**Mitigation of mid- and long-term drifts.** To mitigate the medium and long term instabilities, the atomic clock output will work in conjunction with a GNSS receiver (see Section 2.3) so that the time information from the satellites will be used to identify and correct the drifts by means of a constant frequency comparison achieved using a dedicated universal frequency counter. Here again, the task can be performed using the Keysight 5323A frequency counter. This check will allow also a permanent comparison between the local generated time and the UTC provided by the GNSS to know exactly the relationship between them. As evident from the scheme in Fig. 3, the 125 MHz clock will be generated from the local atomic clock source and the GNSS will be solely used to accord it with the

[2]Actually, a third clock would be required in order to detect which one of the clocks is experiencing instabilities.

universal coordinated time. This is the most effective scheme for a detector such as Hyper-Kamiokande because the event reconstruction relies mostly on the short term clock stability while the universal time tagging will be used to date an interesting event and to label the neutrino interactions generated by the particles accelerated at J-PARC as explained below.

## 2.3 Global Navigation Satellite System (GNSS)

As already mentioned, the GNSS will also be used to correlate the local time base with the universal coordinated time by means of the information included in their data stream. To guarantee an accuracy at the level of 50 ns or better, many parameters must be taken under control and corrected, if needed. Some of them are related to the satellites, like e.g. the position of each transmitter at any given time. This implies that each satellite's orbit must be known with a precision that sometimes goes beyond the one included in the data stream. Some other elements are relative to the receiver and concern the electromagnetic signal that reach the antenna, the interference and the reflection to which it is subjected. To improve the first kind of uncertainty, correction algorithms will be implemented on the received data by means of a computer infrastructure that elaborates information coming from the UTC consortium. This consortium is composed from many laboratories spread around the world working together on the UTC definition. As part of their duty, they publish a weekly report that includes parameters needed to reconstruct the universal time at the "state of the art" precision. The uncertainty related to the local equipment can be mitigated performing an accurate calibration of the receiver, the associated antenna and the connection cable against a cadence generated by a so-called group 1 laboratory (like SYRTE in Paris) taking part in the UTC consortium and able to guarantee a resolution below 5 ns.

To reduce the data post-processing and reach great precision, a crucial role is played by the GNSS receiver, and its antenna position which is a non-trivial aspect in Hyper-Kamiokande. The far detector's electronics will be hosted in a cavern where the satellites signal cannot arrive directly and the atomic clocks will be placed next to it to minimise the local time base uncertainty. The GNSS equipment will be placed at the cavern's entrance, several kilometers away in a position that maximises the signal reception characteristics, and the signals exchanged by the two elements have to travel over a very long optical fibre without loosing their synchronicity characteristics. To build this link the same technologies proposed for the time distribution module (described below) will be used.

The events generated by the particles packets sent by the J-PARC accelerator must be identified and separated from the noise and astrophysical events. A specific acquisition's window must be opened for each event however a direct "trigger" signal can't be sent due to the distance between the accelerator and the far detector. The most effective solution to this problem is the so-called "common view" technique where the two sites are both equipped with a GNSS receiver locked on the same satellites. The effectiveness of this method is related to the number of satellites "seen" by both sides at the same time and this could be a limiting factor in this case since the far detector's receiver will be installed in a valley surrounded by mountains that narrow the antenna "field of view". To mitigate these limitations multi-constellation receivers will be used so that the number of the available sources will not be limited only to the American GPS (Global Positioning System) but include also the European Galileo, the Russian GLONASS and the Japanese QZSS (Quasi-Zenith Satellite System).

A data collection campaign will be performed, with a portable GNSS receiver, at the far detector site well ahead of the system deployment. This test will be useful to establish the best final antenna position and to check the number of common satellites available. The data collected will determine also the entity of the post-processing needed to achieve the experimental requirements. The portable equipment, composed from the same elements installed at far detector site, will also be helpful during the regular data acquisition to check the resident infrastructure and measure the accord to UTC. This "re-calibration" process could happen every 5 years or so.

An R&D study has already started in order to define the off-the-shelf equipment to be used in Hyper-K and the Septentrio PolaRx5 multi-frequency multi-constellation timing/reference receiver associated with a multi-frequency B3E6 choke ring antenna have been selected [4, 5].

The same reliability considerations described for the atomic clocks are valid also of the GNSS equipments so a minimum set of 2 receivers and 2 antennas will be installed at the Hyper-Kamiokande far detector site and constantly monitored to guarantee that at least 1 functional set will be operational at any time.

### 2.4 Clock synthesizer Board

The frequency that has been selected as main front-end electronics clock is 125 MHz then, such a cadence has to be generated starting form the atomic clock signals. The frequency synthesis must be performed limiting as much as possible any additional jitter and keeping the reference with the PPS and the UTC. The current plan is to design a custom board which will be equipped with a stable 1 GHz oscillator and a PLL used to condition this frequency with the 10 MHz signal coming from the atomic clocks. The PLL output will then be a 1 GHz clock with one edge every hundred aligned with the one coming from the atomic clock which is in turn aligned with the PPS. A clock divider will then be used to provide the final 125 MHz frequency and a set of fan-out buffer chips will provide the signals for all the time distribution modules. The board is still under design at this stage and more details will be provided after construction and characterization.

## 3 Time Distribution Module

Once a stable and precise local time base has been generated, its output cadence has to be distributed to all the front-end modules of the HK detector. Also in this case, a research on the best technologies available to perform the task has been carried out and the two solutions listed below have been selected:

- **Custom solution:** the clock is embedded in a custom data link and distributed by means of a custom design protocol that guarantees a very low jitter characteristics and a bandwidth adapted to the experiment's needs.
- **White Rabbit solution:** The clock and data are distributed together over one bidirectional link where the CERN White Rabbit protocol [6] is implemented. This protocol guarantees a precise time distribution and board to board skew compensation.

Details on these two time distribution systems are given in the next subsections.

### 3.1 Custom Solution

The custom solution relies on the Clock and Data Recovery (CDR) technology which is the process of extracting time information (clock) and data from a single serial stream. The CDR is implemented by means of a specific serializer-deserializer (ser-des) couple to be used on both sides of the link. The simplicity, reliability and the convenience of this technique has fueled its use in many different fields so that all the modern FPGAs have CDR compliant ser-des already embedded on the silicon. This represents a further advantage for the experiment because it is possible to send slow control data and distribute the system clock using one single fibre. It doesn't require any dedicated chip-set beside the FPGA already used to perform all the digital operations needed for the data collection and communication with the DAQ. Reducing the components on the electronics boards has advantages on many critical aspects of the HK's design like the in-water electronics footprint, its power dissipation and the number of links and connectors between the design entities.

A time distribution scheme based on the CDR requires that one entity (called master) receives the precise clock (the master clock), generated as described in the previous section, and distributes it to the different nodes (called slaves). This implies that the master has a CDR compliant link to each slave. The number of slaves, i.e. the front ends, in the HK case, doesn't allow the implementation of all the master's functionalities on a single electronics board hence they have to be divided upon different cards as depicted in the block scheme of Fig. 5. This diffused architecture requires that the base clock must be fan-out to all the different distributors also called Time Distribution Module (TDM) as described before.

In order to guarantee the time performances required by the experiment, extreme care must be devoted to the ser-des configuration to achieve low jitter and a fixed phase relation between the transmitter's and receiver's clock. This last aspect is particularly critical since, in the standard configuration, the FPGA's ser-des locks on a random phase after each reboot or reset.

A minimum number of data transitions per second needs to happen on the line to properly extract time information therefore the data must be encoded in a specific way that guarantees the clock reconstruction on the receiving side. One of the most common encoding techniques is the so called "8b/10b" and all its variants like "64b/66b".

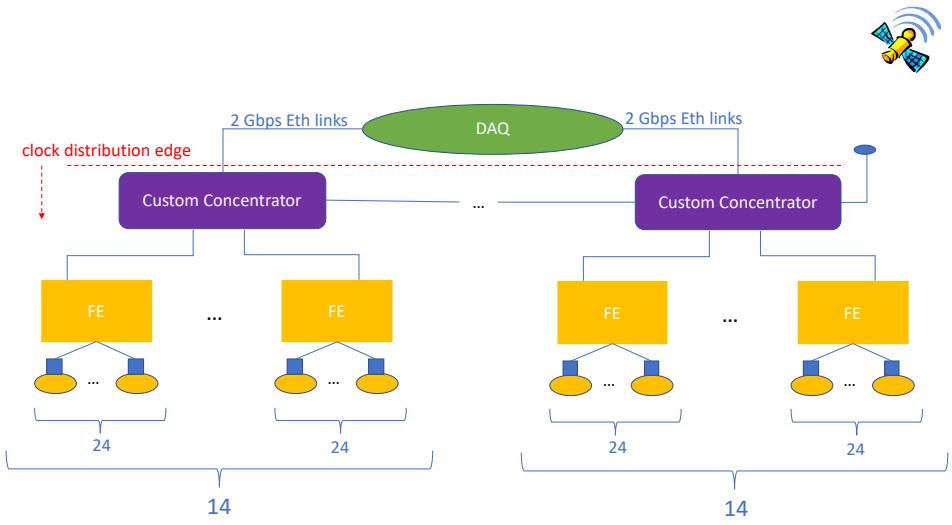


Figure 5: A block scheme of the time distribution based on custom solution.

Each TDM is also connected to the data acquisition system using a standard Ethernet link to exchange slow control information, like the upload firmware for the FE FPGAs or the acquisition related commands, and pass them to all the front-end modules connected to it. A non-deterministic channel from the in-water electronics to the TDM is also established and is used to send housekeeping information and slow control data to the DAQ.

For the custom solution each time distribution module is designed to perform the following tasks:

- Receive the master clock and distribute it embedded into data with a jitter at the endpoint smaller than experimental requirement.
- Guarantee a constant channel to channel phase difference over each reset and power up.
- Guarantee a bidirectional data bandwidth of at least 100 Mbps (at net of the data encoding).
- Distribute the master clock to the neighborhood TDMs (optional).

## 3.2 White Rabbit Solution

White Rabbit (WR) is the name of a collaborative project including CERN, GSI Helmholtz Centre for Heavy Ion Research and other partners from universities and industry to develop a fully deterministic Ethernet-based network for general purpose data transfer and sub-nanosecond accuracy time transfer. Its initial use was as a timing distribution network for control and data acquisition of the accelerator sites at CERN as well as in GSI's Facility for Antiproton and Ion Research (FAIR) project. The hardware designs and the source code are publicly available [7].

This protocol too is based on the clock and data recovery so, also in this case, one optical fibre can be used to distribute the master clock and for a bi-directional communication link between each front end and the data acquisition system.

White Rabbit uses Synchronous Ethernet (SyncE) to achieve sub nanosecond synchronisation and IEEE 1588 Precision Time Protocol (PTP) to communicate time. The phase difference between the master reference clock and the local clock is measured using a specific module based on phase frequency detectors [8]. A two-way exchange of the Precision Time Protocol synchronisation messages allows precise adjustment of clock phase and offset. The link delay is known precisely via accurate hardware timestamps and the calculation of delay asymmetry. The measurements results are computed to align the master and the slave clocks and remove skew due to the cabling and thermal effects. This feature is certainly useful but not fundamental in the Hyper-Kamiokande due to the fact that the fibers and the electronics are in a caver where the temperature excursions are very limited.

The White Rabbit can be considered a sort of an off-the-shelf solution since the hardware can be bought from companies that produce and sell WR compliant electronics devices. As mentioned earlier, hardware, firmware and software designs are distributed with an open hardware license hence the WR functionalities can be embedded in custom systems that host FPGA devices. This aspect is both a limitation and a feature since it is very simple to implement a default White Rabbit infrastructure but any functional modification requires a deep knowledge of a complex project. One example is the data bandwidth. WR is based on the 1 Gbps Ethernet protocol which on one side is very convenient because the data stream can be also fed to a standard computer but, modifying the bandwidth is particularly difficult because it requires a modification of a complex and vast design.

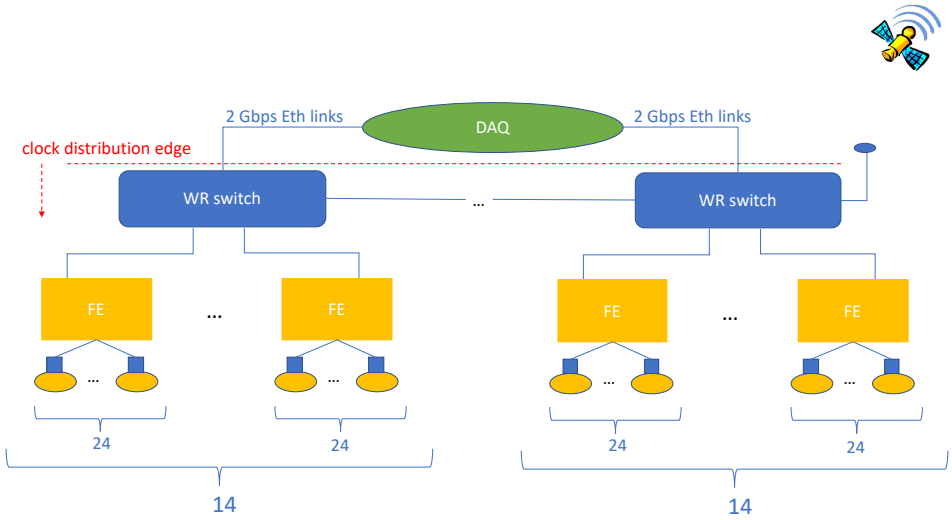


Figure 6: A block scheme of the time distribution based on White Rabbit solution.

Distributing the clock using this infrastructure means building an Ethernet network where each front-end is a network endpoint and the connections can be routed through a special network switch. Each node, including the switch, can act as a master or slave meaning that it can receive the master clock base (called grand master clock in the WR language) and distribute it to all the other endpoints through a network that can have even multiple layers. Each White Rabbit compliant endpoint that receives the data stream, can reconstruct the master clock and compensate the phase differences as explained above. If a node is not WR compliant all the time information is filtered following the standard Ethernet rules but the data content is preserved. This feature is particularly useful in the HK case because the time synchronisation network can be included in the data acquisition infrastructure. A possible scheme is depicted in Fig. 6.

The grand-master module is one of the network switches. Some of its ports are connected to the front-ends, some others are connected to the DAQ and the rest are connected to other switches. This topology allows the system clock distribution in a so-called daisy-chain scheme.

A White Rabbit clock distribution network allows to:

- Receive the master clock and distribute it embedded into data with a jitter at the endpoint smaller than experimental requirement.
- Compensate the channel to channel phase difference at any time.
- Guarantee a data bandwidth of 1 Gbps at net of the data encoding and time synchronisation packets.

# 4 Time Distribution Endpoint

The Time Distribution Endpoint (TDE) is the entity integrated in the front-end electronics that receives the data stream from the Time Distribution Module, reconstructs the clock embedded, cleans

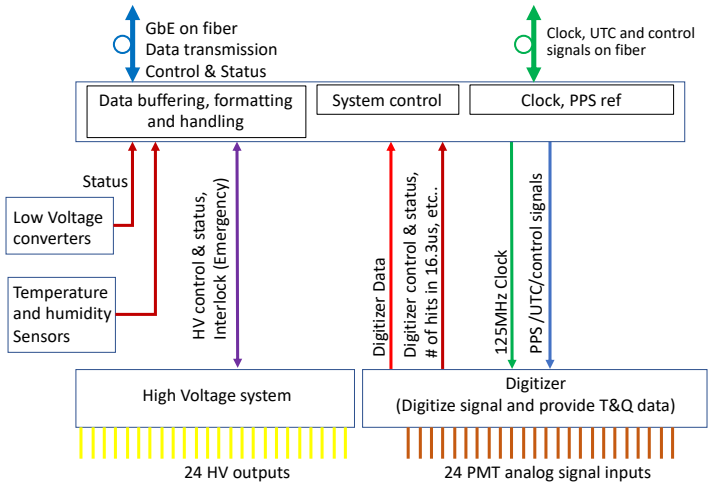


Figure 7: A front end electronics scheme with all the functional blocks reported. The shown grouping doesn't necessarily reflect the final hardware arrangement.

it by means of a PLL and provides it to all the logic elements that need it. A FE general block scheme that reports all the logic elements is depicted in Figure 7. From a hardware point of view the TDE needs an optical transceiver to establish the connection over the optical fiber, an FPGA with the corresponding ser-des to extract the clock, and a PLL to eventually clean the jitter and can be also used as a fan-out in case more than one device need to receive it. The described functionalities and components can be either implemented on a stand alone board or installed along with other components on a shared platform. The main difference between these two approaches is that, in the first configuration extra connectors are needed to propagate the clock cadence in the front-end. An integrated scheme, where the time distribution endpoint is part of the digitizer or the concentration board, seems more advantageous because this would allow to share the FPGA reducing the total power consumption and the heat dissipation, to enhance the reliability reducing the number of connectors and to simplify the entire system reducing the number of wires needed to exchange the relevant signals between the different FE boards. If this integrated scheme will be selected at the end, the TDE would consist of just the optical ser-des (2 in case of redundancy), the PLL and a firmware IP to handle the time data stream and extract the clock to be integrated in the shared FPGA. All these elements will be provided as part of the time distribution package. In case the final architecture would require an independent board, it will be designed and produced as a part of the time distribution system.

Independently of the implementation details, the established channel will be also used to exchange slow control data between the front end and the DAQ. Even though the exact number of sensors to be read and its routing schemes are not completely defined, the TDE will be equipped with enough ports to handle environmental sensors and convey the information on the data transmission link. The firmware IP will also manage some critical data like an emergency acquisition stop and the procedure to remote upload the front end FPGAs.

## 4.1 Experimental Results

A test campaign has been conducted to evaluate the proposed solutions. The experimental tests are based on evaluation boards and prototypes used as platforms to develop the firmware and the methods that will be used in the final release.

For the "custom solution" the study has stated using a couple of Xilinx evaluation boards KC705 equipped with the Xilinx Kintex 7 FPGA [9]. A specific firmware has been written to establish a 1 Gigabit Ethernet communication link over an optical fibre with a special ser-des configuration that implements the fixed phase CDR method. The firmware has been installed on the boards set, one acting as transmitter (TX) and the other as receiver (RX). On each board, SMA connectors were used to output the transmitted and reconstructed clock signals so that their quality could be measured.

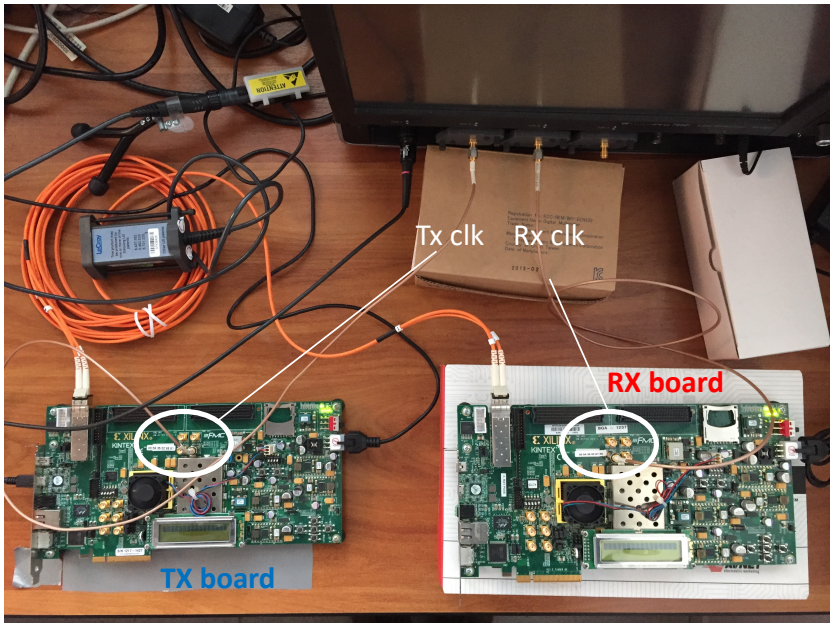


Figure 8: The custom solution test-bench based on the KC705 evaluation boards. On the left the first board configured as transmitter (TX) and on the right the second configured as receiver (RX). In the photo, the orange optical fibre and the 2 cables that bring the transmitted and reconstructed clock to an oscilloscope are visible.

The described setup is presented in Figure 8.

The first phase has been devoted to the data bandwidth compliance verification with the 1 Gbps Ethernet protocol; then, the attention has been focused on the jitter performances measurement for the embedded clock which represents the most important element at this stage of the R&D. An extensive measurement campaign has been carried out and the cadence characteristics have been evaluated in time and frequency domains. In the time domain the jitter has been measured by means of an oscilloscope (Lecory Wavepro 760Zi 6 GHz 40Gsps) and the results are reported in Figure 9.

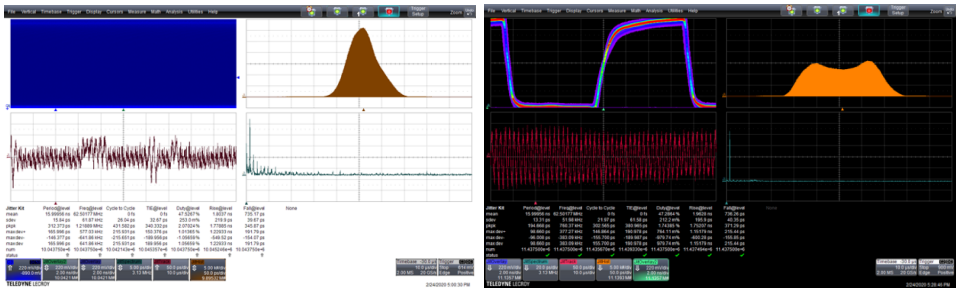

Figure 9: Time domain jitter measurements for the custom solution implemented on the KC705 evaluation boards set. On the left the transmitted clock is reported with a total jitter of 32 ps. On the right the received clock has 50 ps jitter and an evident deterministic component.

The jitter that affects the transmitted clock is equal to 32 ps which gives a measure of the cadence quality before the distribution. As can be seen from the Figure, the reported histogram doesn't have a perfect gaussian shape, sign of a deterministic component. This effect is even more evident on the receiver board where the reconstructed clock has a total jitter of 61 ps and the relative histogram has two clear peaks. Unfortunately, the measurement in the time domain doesn't provide any other detail about that.

The same clock signals have been evaluated also in the frequency domain using a phase noise

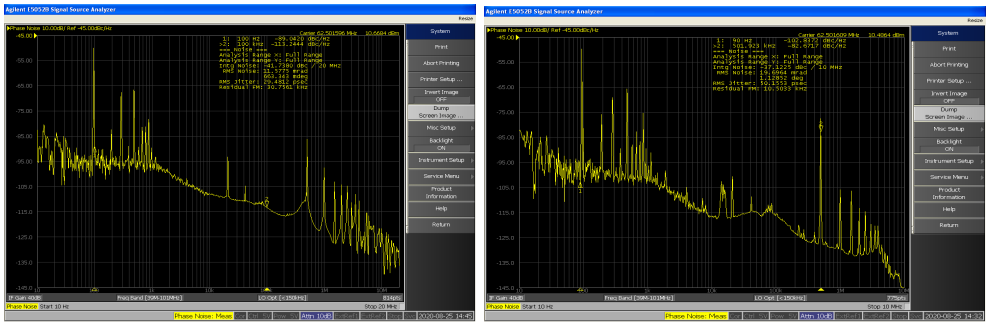

Figure 10: Frequency domain jitter measurements for the custom solution implemented on the KC705 evaluation boards set. On the left the transmitted clock is reported with a total jitter of 29.5 ps with evident components at 500 kHz. On the right the received clock is presented with a 50.1 ps jitter and the same evident deterministic component.

analyser. The principle of this kind of measurement can be explained in a simplified way as follows. The clock under study is sent to an instrument capable to recognise its frequency and generate a cadence of equal characteristics but with very low jitter. The two clocks, the input one and the one generated internally, are combined using the heterodyne function (the same used in the demodulation operation) which result is the difference between the two. This waveform is then plotted and represents the frequency deconvolution of the clock jitter while the area under the curve is equal to the total jitter.

For this test a Keysigth E5052B has been used and the phase analysis plots of the transmitted and received clocks are reported in Figure 10. From the plots the total jitter values can be obtained: 29.5 ps for the TX and 50.1 ps for the RX, very similar to the measurement in the time domain. Moreover spikes at 500 kHz (spurious) are evident on both the transmitted and received clock which are the source of the deterministic jitter. The fact that the same "modulation" frequency is present on both sides of the link calls for an effect generated by the board hardware. The cause has then been identified in the DC to DC power supply converters that feed the FPGA.

A second test-bench has been realised using a custom board as receiver (see Fig. 11) with a different power supply scheme and FPGA: a Xilinx Zynq 7000. For this new chip a compatible firmware has been designed so that the same 1 Gigabit Ethernet link has been established and a similar set of measurements has been carried out. The jitter on the received clock this time is lower (40.6 ps total)

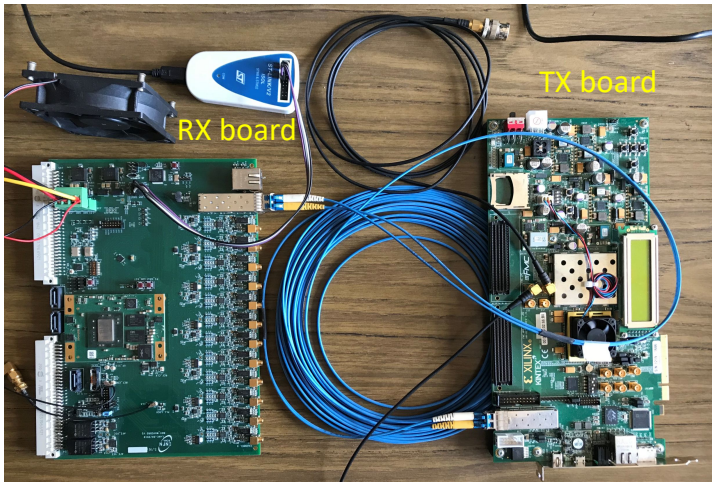


Figure 11: The custom solution test-bench modified using a custom board (on the left) as receiver and a KC705 as transmitter on the right. The connection scheme is the same as in the previous setup.

and the "modulation spikes" are less pronounced (Fig. 12 left). The custom board is equipped also with a so called jitter cleaner component, a Phase-Locked Loop (PLL) SI5345 capable to filter the

jitter and produce a cleaner clock. A measurement of the jitter as been performed also on the clock treated by this filter and the results are shown in the right plot of Figure 12. The excellent filtering capability of the PLL is evident since the measured jitter is now 2.4 ps and the modulation components are almost gone.

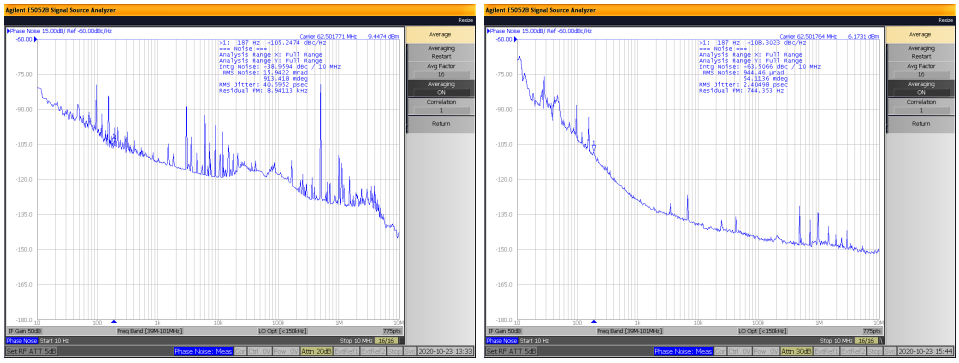

Figure 12: Frequency domain jitter measurements performed on the clock reconstructed by the custom board. On the left the clock before the jitter cleaner PLL and on the right as measured after the filter.

The phase stability has been also tested using an oscilloscope in infinite persistence mode triggered on the transmitted clock. The receiver board has then been reset at regular intervals and the RX clock has been reconstructed always with the same phase distance to the TX clock every time the link has been re-established.

The results of this extensive test campaign are very encouraging because all the Hyper-Kamiokande specifications are largely met and this clock distribution scheme is mature enough to be used in the experiment.

A similar test campaign has been carried out to evaluate the White Rabbit solution using a couple of custom boards realised by the INFN branch of Rome 1 and presented in Figure 13. The connection

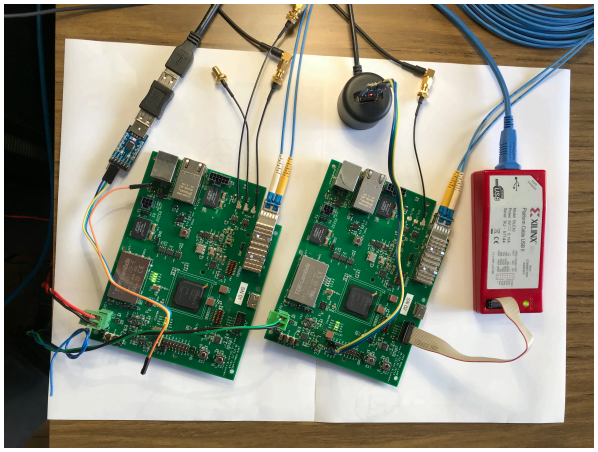

Figure 13: The White Rabbit test bench composed by two custom boards developed in the INFN test bench of Rome 1.

scheme is very similar to the one used for the custom solution: the two boards, equipped with Xilinx Spartan VI FPGA, are connected with an optical fibre (the blue cable) and the transmitted and received clocks are extracted by means of black coaxial cables. The data bandwidth has been measured compliant to the Gigabit Ethernet standard, moreover, connecting one board to a computer, it has been verified that the data packets are correctly exchanged while the time information is dropped as described in the previous paragraph.

The clock characterisation has been carried out in two steps. First, the PPS provided by the two WR nodes has been verified to be stable over different resets and its total jitter on the RX side has

been measured at 17.9 ps. Then the jitter on reconstructed clock has been measured in the frequency domain and is reported in the plot of Figure 14. The phase noise analysis starting form 10 Hz shows a

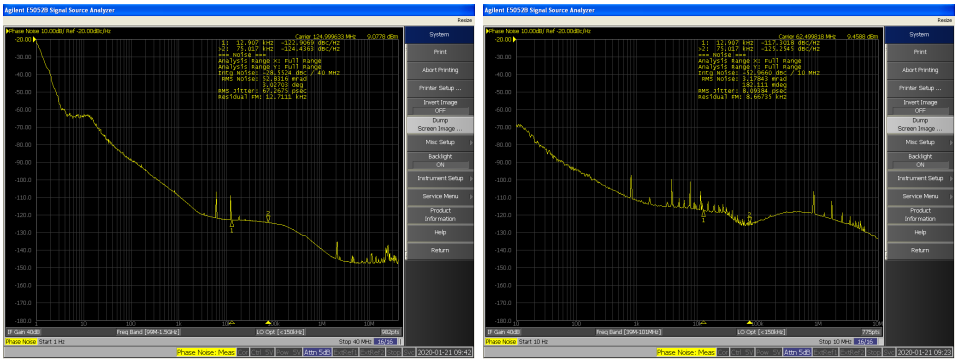

Figure 14: Frequency domain jitter measurements performed on the reconstructed clock using the White Rabbit scheme. On the left the phase noise analysis including frequencies as low as 1 Hz. On the right the same measurement starting at 10 Hz.

jitter as low as 8 ps RMS while at frequencies below that threshold there is a great quantity of noise. If the same measurement is performed starting form 1 Hz the total jitter rises to 67 ps and there are some hints that this additional noise is generated by the local oscillator on the transmission side.

## 4.2 First Integration Test

Once clock distribution concept based on CDR has been evaluated a new test campaign has been launched to evaluate its performances against the first prototypes of the digitizers under development for the experiment. Since that R&D is still ongoing a limited set of tests can be carried out but still sufficient to give indications of the possibility to integrate the different parts at the final stage. This effort is also a first attempt to realise the so-called "vertical slice test" which consists in realizing an electronics chain with all the components needed to acquire signals from a PMT. Starting the time distribution integration with the front-end at this early stage allows also to better identify the interfaces and prevent problems which will be hard to solve once the designs will be more mature.

At this time the 4 proposed digitizers are at different stages of development and only the QTC and discrete solution have built prototypes to allow tests. In this framework efforts have been made to start the time distribution integration and measurements are ongoing. The idea is to perform time related measurements, like the event's time stamp generation, using the clock distributed as explained before and compare them against the one made using the local oscillator. The test can be considered passed if the integrated measurement shows equal or better results.

## 4.3 Summary

The test campaign conducted on the prototypes described above has shown that the CDR technology is very well suited for the Hyper-Kamiokande experiment since both of its implementations, the custom solution and the White Rabbit, can achieve performances that are well below the experiment's requirements. Moreover, the development group has shown to be capable of implementing these technologies on custom designs. Another important achievement has been the successful implementation and use of a jitter cleaner PLL which will be of great help in case, in the final architecture, the distributed clock will suffer from noise induced by other FE electronics components. Moreover, a communication channel implemented on the links has a bandwidth 10x larger than required and this will ensure that there will be no problem of transporting the information planned for the experiment.

During this R&D phase the difference between the custom solution and the White Rabbit has been confirmed especially for what concern the flexibility of the first one. This aspect, associated with the fact that in HK the active phase alignment doesn't seem crucial, would make the custom solution more preferable. This is just a first evaluation, though, and the R&D group is open to discuss this aspect

also considering that it has all the means to deliver a final system based on White Rabbit as shown in this document.

# 5 The Proposed Prototypes

To better evaluate the concepts and the architecture described above a set of prototypes, one per each section, has been assembled. This system will allow the test of the entire chain and will support the experiment's vertical slice test. The results of this characterization will be used to give the final figure of merit of the proposed time distribution system.

## 5.1 Clock Generation and UTC

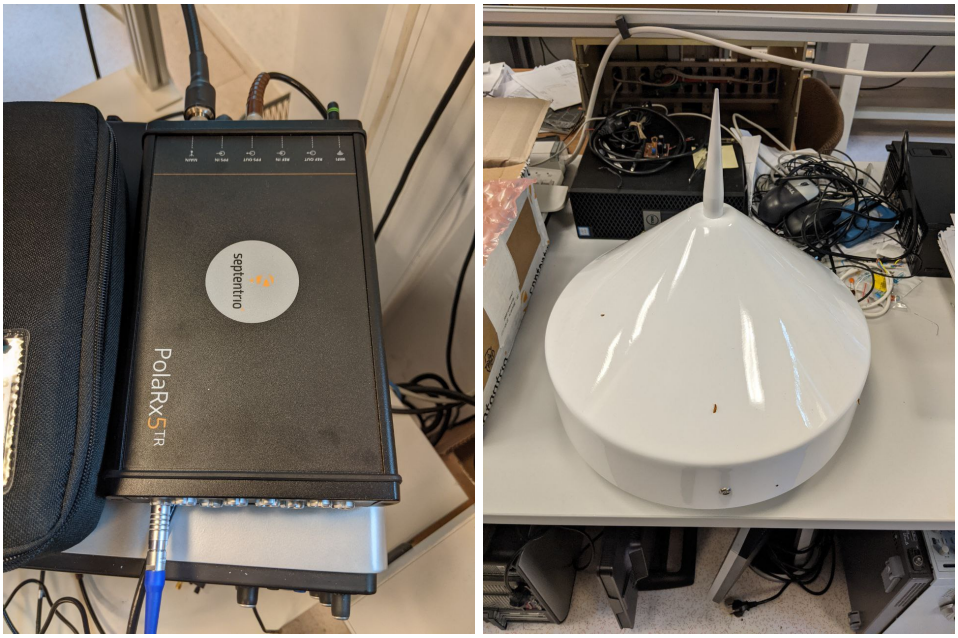


Figure 15: The Septentrio PolaRx5 GNSS receiver and the associated antenna.


Figure 16: The Stanford Research System FS725 Rubidium atomic clock.

The architecture proposed for the clock generation and UTC synchronisation is composed almost entirely from commercial components. The selected GNSS receiver is the Septentrio PolaRx5 multi-frequency multi-constellation timing/reference receiver associated with a multi-frequency B3E6 choke ring antenna. A first sample of this set has been already acquired and is under test (Fig. 15). As

described above, the atomic clock selection is still ongoing due to the price difference between the two candidate instruments that are: the T4science ph maser 1080 [10] Passive Hydrogen Maser and the Stanford Research System FS725 Rubidium atomic clock [11]. The second clock generator has already been purchased and is under characterization (Fig. 16). For frequency difference measurement the Keysight 5323A has been selected, a first sample has been purchased and is in use in our laboratory. The instruments already in our possession compose an almost entire clock generation system. To complete it we are designing the clock multiplication board which will be finalized and the prototype tested by the time of the final review.

## 5.2 Time Distribution Module

### 5.2.1 Custom Solution

The selected time distribution module to implement the custom scheme is the System On Module (SOM) TE0745 [12] built around a Xilinx Zynq 7000 (XC7Z035) hosted on a carrier module TEB0745 [13] both from Trenz. The platform can be equipped with 8 optical ser-des to implement as many time distribution links to the front-ends. The connection to the DAQ will be provided by an Ethernet communication link implemented on a standard RJ45 connector and handled by the embedded processor. This commercial solution represents a cost effective system that doesn't require any other hardware engineering effort so all the developing time can be devoted to the firmware and software. The only limitation is represented by the fact that the board set cannot be expanded further and the number of optical fiber links is defined hence the link redundancy has to be handled outside the board by means of an optical switch. This solution however has already been implemented on the Km3Net experiment and its technology can be exploited in Hyper-Kamiokande.

Figure 17: The custom board proposed as Time Distribution Module prototype to implement the custom distribution scheme. The design can be easily modified to host more optical ser-des.

In case the link redundancy has to be handled on the TDM the number of ser-des has to be doubled but only half of them have to be active at any given time. The link switching will be supervised by the FPGA's firmware. In this case the proposed TDM is based on a custom designed board built at INFN by the same group that is participating to this effort and shown in Figure 17. As evident from the figure the electronics is equipped with all the features needed. It has 8 optical transceivers connected to 8 FPGA's ser-des and an RJ45 connector for the DAQ connection. There is also a set of coaxial

connectors to receive the main clock and distribute it to other elements. The used FPGA is a Xilinx Kintex 7 160T, the actual power consumption is less than 15 W. As it is, this equipment can be used as a prototype, while a modification to add extra 8 optical transceivers is needed for the production. This work doesn't seem very difficult and time consuming since the extra transceivers will be connected in parallel to the existing one and the switching method will be implemented in firmware.

### 5.2.2 White Rabbit Solution

The TDM proposed solution to implement the White Rabbit scheme is the commercially available White Rabbit switch. As all the hardware included in this framework the switch has been designed by CERN and engineered and produced by different commercial companies engaged to deliver and sell a product that is compliant with the defined specifications. This switch can than been considered as an off the shelf product to be bought and used as it is with no extra engineering effort required (neither for the hardware nor for the firmware). This solution has already been selected by other experiments and the reliability of the companies in terms of production has already been established. For the ongoing R&D we have purchased via CERN a WR switch from the Seven Solutions company. The switch available today has 18 ports that can serve 8 FEs, in case an on-board optical transceiver redundancy is required, otherwise up to 16 clock distribution links can be implemented. The extra ports will be used for the DAQ communication. The protocol available at this time is a 1 Gbps Ethernet that fully meets the experiment's specification but a new version is under design. It will feature a 10 Gbps links backward compatible with the actual one that can be used as well just replacing the hardware.

## 5.3 Time Distribution Endpoint

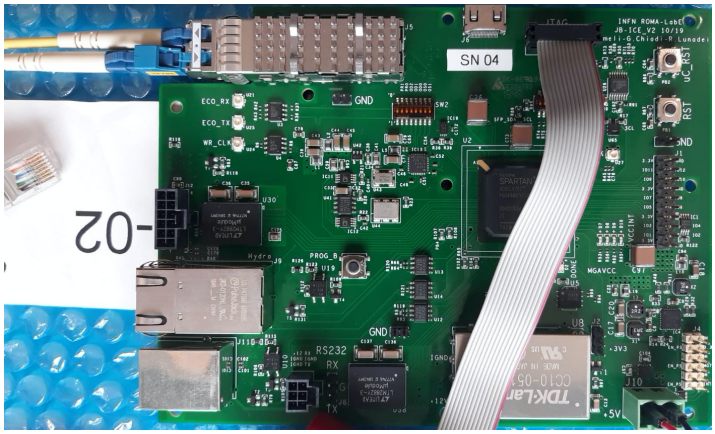


Figure 18: The proposed candidate for the TDE in case a stand-alone board is required.

As mentioned before, integrating the time distribution endpoint functionalities in either the concentration or the digitization board seems much more advantageous, as well as we can judge, because it can increase the reliability and simplify the design by reducing the footprint, the power consumption and heat dissipation. However, we are ready to support also a solution that requires a separate board using the electronics shown in Figure 18. It has been designed around a Xilinx Spartan VI and hosts an optical transceiver to receive the time distribution serial data stream. The reconstructed clock can be distributed to other elements using miniaturized coaxial connectors. Humidity and temperature probes are already present on the board but, a set of extra IO ports can drive other environmental sensors. In the actual configuration this system requires a single 5V power line and consumes 3W. The design will require some minor modification to be ready for the final production like adding a second optical serdes and removing some features not needed in Hyper-Kamiokande. Nevertheless, the board can be used as it is during test phase having all the required functionalities to support both the custom and the White Rabbit distribution schemes. In terms of reliability this solution is very well advanced since it has been used for the Km3Net experiment and all the needed evaluations have been

already performed. The current design is rated to survive for more than 20 years and, we think that, the minor modifications needed to adapt it for HK won't change this characteristic.

Even in case the collaboration will decide to opt for an integrate solution, this setup could be used in a preliminary phase to test the entire electronics chain while wating for the final boards.

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