Fec test report:

Date: 2021-05-07 15:08:09

Tester name: Boris

Test#1 Monitoring values — Passed

0	FEC label	069	OK
1	FEC DC2438 ID	8a0000024db46d26	OK
2	FEC_T (to 35°C)	21.094	OK
3	FEC_Vdd (3.2V to 3.4V)	3.290	OK
4	FEC_I (1.1A to 1.5A)	1.221	OK
5	FEC_Vad (1.9V to 2.0V)	1.960	OK

Test#2 Slow control registers: — Passed

Test#3 Pedestal run: — Passed

Mean in range (245.0:255.0), 3.5 < rms < 8.0 (fpn 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns — Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run — Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3108	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3075	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3074	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3119	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3067	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3043	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3092	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3021	OK

FEC test final result: — Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
2	fe 0 moni T 0	0	0 Tdcm(0) Fem(00) FEC_T: 21.094 degC
3	fe 0 moni V 0	0	0 Tdcm(0) Fem(00) FEC_Vdd: 3.290 V
4	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
5	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
6	fe 0 pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
7	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
8	fe 0 moni I 0	0	0 Tdcm(0) Fem(00) FEC_I: 1.221 A
9	fe 0 moni S 0	0	0 Tdcm(0) Fem(00) FEC_Serial: 8a0000024db46d26

Slow control registers test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
2	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
3	fe fec_enable	0	0 Tdcm(0) Fem(00) Reg(1) = 0x12248000 (304381952) FEC_Enable: 1
4	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
12	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
13	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
14	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
15	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
16	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
17	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
18	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
19	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
20	fe 0 after 0 read 3	0	0 Tdcm(0) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
21	fe 0 after 1 read 3	0	0 Tdcm(0) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
22	fe 0 after 2 read 3	0	0 Tdcm(0) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
23	fe 0 after 3 read 3	0	0 Tdcm(0) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
24	fe 0 after 4 read 3	0	0 Tdcm(0) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
25	fe 0 after 5 read 3	0	0 Tdcm(0) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
26	fe 0 after 6 read 3	0	0 Tdcm(0) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
27	fe 0 after 7 read 3	0	0 Tdcm(0) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
28	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
35	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(0) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x3 (Aligned SCA_Write)
6	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(0) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)

19	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
21	fe adc 0 write 0x5 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(0) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE WAIT_FEM_PKT Curren
52	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test			
NO	Command	Error	Response
0	daq 0xFFFFFF F	0	0 Tdcm(0): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(0) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(0) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(0) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(0) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(0) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(0) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(0) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(0) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done

35	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(0) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)
37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xfffd	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xfffb	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff

113	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
114	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
115	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
116	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
117	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
118	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
119	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
120	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
121	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
122	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
123	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
124	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
125	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
126	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
127	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
128	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
129	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
130	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
131	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
132	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
133	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
134	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
135	fe 0 asic_mask 0xfff7	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfff70000
136	fe 0 after 3 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(3) Reg(1) <- Test_mode=calibration
137	fe 0 after 3 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
138	fe 0 after 3 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(3) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
139	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
140	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
141	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
142	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
143	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
144	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
145	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
146	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
147	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
148	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
149	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
150	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
151	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
152	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
153	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
154	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
155	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
156	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
157	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
158	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
159	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
160	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
161	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
162	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
163	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
164	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
165	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
166	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
167	fe 0 asic_mask 0xffef	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffef0000
168	fe 0 after 4 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(4) Reg(1) <- Test_mode=calibration
169	fe 0 after 4 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
170	fe 0 after 4 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(4) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
171	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
172	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
173	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
174	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
175	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
176	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
177	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
178	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
179	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
180	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
181	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
182	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
183	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
184	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
185	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
186	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
187	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
188	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
189	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
190	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)

191	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
192	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
193	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
194	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
195	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
196	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
197	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
198	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
199	fe 0 asic_mask 0xffdf	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffdf0000
200	fe 0 after 5 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(5) Reg(1) <- Test_mode=calibration
201	fe 0 after 5 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
202	fe 0 after 5 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(5) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
203	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
204	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
205	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
206	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
207	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
208	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
209	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
210	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
211	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
212	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
213	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
214	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
215	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
216	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
217	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
218	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
219	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
220	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.960 V
221	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
222	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
223	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
224	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
225	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
226	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
227	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
228	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
229	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
230	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
231	fe 0 asic_mask 0xffbf	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffbf0000
232	fe 0 after 6 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(6) Reg(1) <- Test_mode=calibration
233	fe 0 after 6 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
234	fe 0 after 6 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(6) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
235	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
236	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
237	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
238	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
239	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
240	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
241	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
242	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
243	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
244	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
245	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
246	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
247	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
248	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
249	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
250	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
251	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
252	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
253	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
254	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
255	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
256	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
257	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
258	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
259	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
260	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
261	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
262	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
263	fe 0 asic_mask 0xff7f	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xff7f0000
264	fe 0 after 7 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(7) Reg(1) <- Test_mode=calibration
265	fe 0 after 7 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
266	fe 0 after 7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(7) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
267	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
268	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed

269	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
271	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7		
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0	0 r	0.0	0.0
1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0	1 r	511.0	0.0
2 r	278.9	0.7	2 r	275.9	0.7	2 r	301.3	0.7	2 r	268.4	0.7	2 r	315.0	0.7	2 r	295.3	0.7	2 r	305.8	0.6	2 r	340.9	0.7
3	262.9	7.3	3	247.2	6.7	3	292.4	6.7	3	278.6	7.0	3	326.8	7.9	3	225.0	7.2	3	321.7	7.3	3	342.8	7.1
4	223.1	4.7	4	221.0	4.6	4	274.9	4.8	4	194.2	4.7	4	276.2	5.0	4	194.7	5.3	4	283.3	5.0	4	340.7	4.7
5	190.9	6.6	5	249.2	6.4	5	274.2	6.9	5	333.9	6.6	5	277.9	7.6	5	213.8	7.0	5	238.0	7.1	5	400.6	6.8
6	165.0	4.8	6	350.7	4.6	6	379.8	4.6	6	220.8	4.4	6	249.9	5.0	6	244.2	4.7	6	362.2	4.7	6	308.0	4.7
7	240.9	6.9	7	270.0	6.7	7	237.5	6.8	7	288.5	6.9	7	313.6	7.2	7	203.4	6.8	7	272.7	6.7	7	370.6	6.4
8	206.1	4.8	8	185.7	4.5	8	282.7	4.5	8	236.7	4.8	8	303.4	4.7	8	220.5	4.8	8	277.6	4.8	8	305.7	4.4
9	161.4	7.0	9	318.2	6.4	9	237.4	6.4	9	345.5	6.4	9	257.4	6.9	9	182.1	6.6	9	268.6	6.7	9	381.2	6.5
10	242.4	5.1	10	264.9	4.8	10	302.9	4.6	10	266.1	4.6	10	324.2	4.8	10	200.6	4.9	10	283.1	4.8	10	274.1	4.5
11	244.8	6.7	11	275.9	6.1	11	215.6	6.1	11	200.1	6.0	11	287.1	6.9	11	206.6	6.8	11	233.6	6.7	11	313.3	6.7
12	237.8	4.6	12	271.6	4.5	12	175.8	4.6	12	287.5	4.7	12	353.6	4.9	12	240.6	4.8	12	328.9	4.7	12	294.4	4.7
13	190.0	6.1	13	240.2	5.9	13	258.1	6.4	13	214.8	6.1	13	266.2	6.9	13	245.2	6.6	13	329.0	6.6	13	353.7	6.3
14	215.8	4.8	14	224.4	4.4	14	226.1	4.4	14	358.9	4.4	14	283.0	4.7	14	216.8	4.5	14	314.2	4.8	14	258.6	4.5
15 f	153.3	1.9	15 f	235.5	1.6	15 f	129.1	1.7	15 f	212.8	1.7	15 f	328.6	1.6	15 f	215.4	1.7	15 f	256.4	1.6	15 f	260.3	1.6
16	250.0	6.2	16	219.5	6.4	16	252.3	6.1	16	257.5	6.0	16	272.9	6.6	16	238.9	6.2	16	288.0	6.4	16	270.1	5.9
17	153.5	4.4	17	196.7	4.6	17	197.4	4.5	17	294.8	4.4	17	264.3	4.8	17	181.7	4.6	17	261.1	4.7	17	268.9	4.5
18	307.9	6.3	18	225.8	5.9	18	229.2	6.2	18	339.9	6.0	18	244.1	6.8	18	171.2	6.2	18	235.6	6.6	18	349.3	6.1
19	261.1	4.5	19	235.0	4.2	19	283.4	4.7	19	244.0	4.4	19	208.8	4.8	19	200.6	4.6	19	247.3	4.9	19	304.8	4.7
20	297.1	6.1	20	182.4	5.8	20	300.8	6.0	20	248.9	6.1	20	314.2	6.7	20	228.0	6.2	20	256.4	6.1	20	315.8	5.9
21	215.6	4.5	21	253.6	4.5	21	219.2	4.3	21	159.4	4.6	21	216.9	5.2	21	266.3	4.8	21	221.6	4.7	21	352.3	4.5
22	174.7	6.3	22	225.8	5.7	22	238.5	5.6	22	251.5	5.8	22	237.8	6.5	22	223.4	6.3	22	232.8	6.1	22	243.7	6.0
23	201.0	4.5	23	304.6	4.4	23	253.8	4.5	23	199.4	4.5	23	267.9	4.6	23	210.0	4.9	23	236.8	4.6	23	383.5	4.3
24	179.6	6.2	24	228.5	5.7	24	214.0	6.0	24	236.0	5.9	24	222.6	6.7	24	260.4	6.2	24	263.4	6.3	24	300.3	5.8
25	189.6	4.7	25	225.7	4.4	25	197.2	5.0	25	270.3	4.7	25	285.4	4.8	25	224.8	4.6	25	278.4	4.7	25	223.7	4.6
26	167.7	5.7	26	156.5	5.7	26	317.9	5.5	26	241.6	5.9	26	296.1	6.5	26	240.5	6.1	26	267.8	6.3	26	297.4	5.8
27	169.0	4.5	27	266.7	4.2	27	251.3	4.4	27	243.4	4.2	27	290.0	4.8	27	237.6	4.6	27	325.7	4.8	27	295.3	4.7
28 f	108.0	1.9	28 f	274.3	1.8	28 f	264.3	1.8	28 f	294.8	1.7	28 f	252.6	1.7	28 f	296.1	1.6	28 f	246.9	1.7	28 f	337.2	1.7
29	255.1	5.8	29	277.1	5.8	29	183.7	5.6	29	310.0	5.8	29	306.1	6.5	29	223.9	5.7	29	294.2	6.0	29	258.2	5.8
30	147.9	4.5	30	275.5	4.5	30	241.0	4.4	30	217.3	4.5	30	281.3	4.8	30	234.9	4.4	30	267.6	4.8	30	318.1	4.2
31	220.7	6.1	31	215.3	5.8	31	325.1	5.6	31	208.7	5.4	31	258.7	6.2	31	141.8	5.9	31	287.0	5.8	31	200.1	5.8
32	223.1	4.6	32	217.3	4.5	32	265.6	4.6	32	286.8	4.6	32	263.7	4.8	32	284.3	4.8	32	294.6	4.5	32	237.5	4.3
33	247.8	5.7	33	310.9	5.5	33	150.8	5.6	33	175.4	5.7	33	178.0	6.2	33	256.9	6.0	33	247.7	6.1	33	274.1	5.5
34	193.1	4.5	34	212.1	4.3	34	259.2	4.4	34	277.1	4.5	34	347.5	4.8	34	237.3	4.5	34	308.3	4.6	34	308.3	4.3
35	189.2	5.7	35	229.1	5.4	35	278.0	5.7	35	174.1	5.6	35	331.1	6.3	35	246.4	6.2	35	268.9	5.8	35	290.4	5.5
36	243.4	4.5	36	274.6	4.4	36	254.7	4.5	36	285.1	4.3	36	371.4	4.7	36	195.6	4.8	36	322.8	4.5	36	327.1	4.5
37	177.0	5.8	37	354.6	5.2	37	239.1	5.5	37	190.6	5.4	37	269.9	5.8	37	294.7	5.9	37	256.1	5.7	37	299.3	5.4
38	261.2	4.5	38	257.7	4.3	38	203.2	4.3	38	311.7	4.5	38	400.7	4.8	38	233.7	4.7	38	286.7	4.5	38	383.0	4.4
39	153.8	5.3	39	354.0	5.2	39	212.8	5.0	39	211.9	5.2	39	270.2	5.8	39	326.1	5.3	39	294.6	5.5	39	230.8	5.0
40	300.2	4.2	40	347.2	4.2	40	257.3	4.4	40	262.2	4.4	40	331.1	4.8	40	272.2	4.7	40	227.1	4.5	40	306.8	4.2
41	169.8	4.5	41	267.4	4.3	41	251.5	4.2	41	261.9	4.2	41	229.7	4.5	41	289.4	4.5	41	240.0	4.2	41	302.4	4.2
42	229.6	5.8	42	272.3	5.6	42	303.4	5.7	42	199.6	5.7	42	346.7	6.4	42	204.4	6.3	42	221.9	6.1	42	256.2	5.6
43	167.9	4.4	43	251.8	4.2	43	235.2	4.1	43	283.6	4.2	43	184.4	4.3	43	320.2	4.5	43	320.7	4.5	43	307.5	4.0
44	204.7	6.1	44	247.0	5.4	44	207.8	5.9	44	217.0	5.9	44	371.5	6.1	44	187.4	6.3	44	358.6	6.2	44	314.4	5.8
45	193.2	4.2	45	170.3	4.3	45	269.4	4.3	45	252.1	4.3	45	296.4	4.4	45	184.8	4.2	45	276.9	4.3	45	384.6	4.2
46	224.9	6.0	46	291.3	5.6	46	230.0	5.9	46	214.4	5.8	46	262.4	6.2	46	228.0	5.9	46	188.3	6.0	46	373.6	5.5
47	248.6	4.4	47	288.4	4.3	47	232.7	4.4	47	221.9	4.3	47	250.7	4.4	47	256.7	4.4	47	285.0	4.4	47	292.4	4.3
48	243.0	5.9	48	207.6	5.6	48	324.2	6.0	48	294.1	6.0	48	277.7	6.4	48	230.9	6.1	48	253.4	6.2	48	253.4	5.5
49	191.0	4.3	49	217.6	4.3	49	217.5	4.4	49	229.2	4.3	49	258.8	4.3	49	193.8	4.4	49	285.1	4.5	49	371.7	4.2
50	287.9	6.1	50	221.5	6.0	50	263.3	6.0	50	250.6	5.6	50	192.0	6.1	50	224.5	6.0	50	258.6	6.0	50	216.1	5.5
51	307.6	4.6	51	365.7	4.0	51	215.6	4.4	51	193.8	4.2	51	236.8	4.3	51	263.6	4.3	51	297.0	4.4	51	323.7	4.3
52	293.3	5.9	52	301.3	5.8	52	290.1	5.6	52	234.6	6.0	52	289.2	6.4	52	253.7	6.0	52	310.8	6.0	52	258.7	5.7
53 f	208.6	1.6	53 f	252.3	1.6	53 f	263.1	1.5	53 f	297.4	1.7	53 f	255.4	1.6	53 f	279.8	1.5	53 f	302.3	1.6	53 f	327.4	1.4
54	185.3	4.7	54	275.4	4.1	54	266.1	4.2	54	258.1	4.5	54	263.8	4.3	54	265.5	4.4	54	210.1	4.4	54	327.3	4.1
55	97.1	5.8	55	260.2	6.0	55	294.6	5.8	55	268.6	5.8	55	302.3	6.2	55	218.1	6.2	55	281.7	6.5	55	306.4	5.6
56	245.8	4.4	56	145.0	4.2	56	248.9	4.3	56	202.4	4.2	56	280.5	4.4	56	186.5	4.3	56	254.4	4.5	56	274.5	4.3
57	241.9	6.2	57	213.4	5.7	57	230.5	5.8	57	314.2	6.0	57	285.3	6.5	57	219.2	6.1	57	307.0	6.2	57	406.2	5.7
58	149.2	4.5	58	289.4	4.0	58	316.5	4.3	58	236.0	4.3	58	318.6	4.5	58	262.2	4.1	58	285.9	4.5	58	289.1	4.3
59	153.6	6.1	59	300.1	6.1	59	216.2	5.9	59	271.0	6.1	59	350.6	6.2	59	236.9	6.3	59	185.9	6.5	59	212.3	5.4
60	256.9	4.2	60	251.7	4.2	60	261.7	4.2	60	268.7	4.2	60	350.2	4.4	60	246.4	4.3	60	228.0	4.4	60	357.2	4.3
61	287.9	6.2	61	325.4	6.0	61	222.4	6.2	61	240.9	6.0	61	227.4	6.4	61	188.8	6.3	61	264.7	6.4	61	219.8	5.7
62	230.8	4.5	62	243.9	4.2	62	263.2	4.2	62	299.7	4.5	62	288.5	4.3	62	235.6	4.0	62	251.7	4.7	62	276.7	4.2
63	251.0	6.3	63	310.1	5.9	63	146.7	5.8	63	251.4	6.1	63	242.6	6.5	63	205.0	6.7	63	249.9	6.6	63	310.1	5.6
64	241.9	4.2	64	151.9	4.2	64	239.0	4.2	64	281.4	4.4	64	237.7	4.6	64	292.7	4.2	64	215.0	4.8	64	298.2	4.4
65	206.8	6.2	65	218.9	6.2	65	236.7	6.0	65	246.7	6.1	65	292.7	6.6	65	249.9	6.4	65	322.4	6.6	65	337.3	5.6
66 f	268.9	1.5	66 f	272.0	1.5	66 f	292.4	1.6	66 f	233.2	1.5	66 f	226.2	2.0	66 f	258.6	1.5	66 f	367.4	1.6	66 f	320.3	1.4
67	123.1	4.2	67	223.0	4.2	67	204.8	4.2	67	281.2	4.4	67	224.7	4.4	67	206.4	4.3	67	291.7	4.3	67	353.0	4.2
68	193.6	6.3	68	258.2	6.1	68	240.1	6.0	68	293.3	6.3	68	269.3	6.4	68	145.1	6.5	68	301.9	6.5	68	353.3	5.6
69	280.9	4.3	69	222.8	4.2	69	255.6	4.3	69	269.0	4.6	69	217.2	4.7	69	189.3	4.4	69	260.7	4.7	69	340.8	4.0
70	251.0	6.4	70	235.6	6.1	70	226.5	6.2	70	289.5	6.2	70	262.7	6.5	70	245.8	6.5	70	247.0	6.7	70	224.8	5.9
71	231.4	4.2	71	314.5	4.2	71	248.8	4.4	71	368.4	4.3	71	253.9	4.4	71	135.5	4.2	71	283.3	4.5	71	249.1	4.3
72	156.8	6.3	72	299.8	6.2	72	344.8	6.3	72	270.9	6.2	72	327.4	6.8	72	233.2	6.3	72	340.4	6.6	72	289.8	5.7
73	172.2	4.5	73	310.8	4.5	73	178.6	4.2	73	282.2	4.5	73	227.9	4.4	73	199.6	4.2	73	212.4	4.6	73	315.8	4.2
74	253.1	6.8	74	321.1	6.2	74	324.1	6.4	74	331.9	6.6	74	387.8	6.8	74	229.5	6.6	74	306.9	6.7	74	391.5	5.8
75	224.7	4.5	75	292.2	4.4	75	227.1	4.3	75	280.0	4.3	75	305.9	4.7	75	232.4	4.4	75	238.8	4.3	75	343.4	4.3
76	232.9	6.5	76	254.0	6.2	76	279.4	6.5	76	305.5	6.5	76	283.4	6.8	76	275.9	6.7	76	313.2	7.0	76	247.0	5.7
77	168.5	5.0	77	259.7	4.6	77	252.2	4.3	77	256.4	4.5	77	190.6	4.5	77	245.4	4.4	77	281.2	4.6	77	322.8	4.4
78	222.9	6.9	78	231.2	6.8	78	341.3	6.5	78	252.1	6.7	78	266.8	7.2	78	308.6	6.8	78	250.6	7.1	78	289.1	6.0

Pedestal after centermean.

CHIP 0		
CH	M	STD
0 r	250.0	0.0
1 r	361.1	9.3
2 r	250.1	0.7
3	250.7	6.2
4	250.6	4.8
5	250.9	6.0
6	250.3	4.6
7	250.5	5.9
8	248.3	4.5
9	250.8	6.2
10	250.6	4.7
11	249.5	5.9
12	250.1	4.7
13	250.6	5.9
14	249.1	4.5
15 f	251.0	1.9
16	251.2	5.6
17	250.2	4.8
18	250.7	5.7
19	250.3	4.3
20	250.1	5.4
21	249.1	4.5
22	250.0	5.4
23	249.1	4.3
24	248.6	5.5
25	250.3	4.4
26	248.9	5.5
27	250.4	4.4
28 f	250.7	1.8
29	249.5	5.3
30	250.2	4.2
31	248.5	5.8
32	250.2	4.6
33	249.9	5.1
34	249.5	4.2
35	250.7	5.3
36	250.0	4.4
37	250.6	5.2
38	249.1	4.6
39	248.4	5.1
40	250.7	4.7
41	249.1	4.3
42	250.7	5.2
43	251.7	4.2
44	249.6	5.2
45	250.6	4.2
46	251.0	5.1
47	250.6	4.1
48	250.1	5.4
49	251.3	4.2
50	250.7	5.1
51	251.9	4.2
52	250.3	5.4
53 f	249.8	1.6
54	251.8	4.2
55	251.2	5.2
56	249.9	4.2
57	251.4	5.5
58	250.6	4.1
59	249.9	5.5
60	248.4	4.5
61	250.0	5.3
62	250.8	4.2
63	249.6	5.3
64	248.7	4.0
65	249.9	5.7
66 f	250.1	1.6
67	250.7	4.6
68	249.7	5.6
69	251.3	4.5
70	250.1	5.7
71	250.1	4.2
72	251.1	5.7
73	249.8	4.3
74	249.6	5.9
75	250.6	4.5
76	249.7	5.6
77	249.1	4.7
78	250.9	5.9

CHIP 1		
CH	M	STD
0 r	250.0	0.0
1 r	315.1	9.7
2 r	250.0	0.7
3	251.0	6.2
4	251.2	4.5
5	248.9	5.9
6	247.2	4.4
7	249.6	6.2
8	250.1	4.8
9	251.1	5.7
10	248.5	4.4
11	251.6	5.6
12	248.3	4.6
13	251.4	5.8
14	250.9	4.6
15 f	250.8	1.6
16	250.2	5.4
17	248.3	4.7
18	249.3	5.4
19	250.7	4.4
20	250.2	5.5
21	249.6	4.3
22	250.4	5.5
23	251.5	4.5
24	249.6	5.4
25	249.7	4.4
26	250.6	5.3
27	250.4	4.4
28 f	249.8	1.8
29	250.6	5.2
30	251.0	4.4
31	249.8	5.1
32	250.1	4.5
33	250.1	5.4
34	249.2	4.2
35	250.4	5.1
36	249.9	4.6
37	249.8	5.1
38	251.6	4.3
39	251.6	4.5
40	249.2	4.4
41	251.1	4.2
42	249.6	5.2
43	249.3	4.1
44	251.1	5.0
45	250.5	4.2
46	250.8	5.2
47	251.1	4.2
48	249.2	5.3
49	250.9	4.3
50	249.1	5.3
51	249.8	4.3
52	250.9	5.4
53 f	250.2	1.7
54	249.8	4.2
55	250.4	5.4
56	251.1	4.1
57	250.1	5.3
58	251.0	4.2
59	249.5	5.5
60	250.6	4.0
61	249.8	5.8
62	250.9	4.0
63	250.6	5.5
64	249.7	4.4
65	248.4	5.4
66 f	249.8	1.6
67	249.4	4.4
68	249.4	5.5
69	249.9	4.2
70	249.8	5.5
71	248.7	4.1
72	249.4	5.7
73	249.5	4.3
74	249.6	5.7
75	250.7	4.4
76	249.4	5.6
77	248.7	4.3
78	248.9	5.8

CHIP 2		
CH	M	STD
0 r	250.0	0.0
1 r	374.6	9.9
2 r	250.5	0.7
3	250.3	6.4
4	250.4	4.5
5	249.2	6.3
6	249.4	4.4
7	249.8	6.3
8	249.9	4.5
9	250.8	5.8
10	250.1	4.3
11	250.1	6.1
12	249.3	4.3
13	250.1	5.8
14	251.1	4.6
15 f	250.4	1.8
16	250.4	5.9
17	251.5	4.5
18	251.3	5.9
19	249.8	4.4
20	249.2	5.7
21	250.1	4.4
22	249.0	5.5
23	250.4	4.5
24	249.4	5.2
25	249.5	4.5
26	248.7	5.5
27	251.1	4.7
28 f	250.0	1.9
29	248.5	5.7
30	249.3	4.5
31	249.9	5.7
32	250.2	4.4
33	250.3	5.3
34	249.8	4.4
35	251.4	5.3
36	248.9	4.4
37	251.1	5.0
38	249.8	4.3
39	250.6	5.1
40	250.8	4.3
41	249.9	4.3
42	250.4	5.2
43	250.6	4.2
44	249.6	5.5
45	251.2	4.0
46	250.0	5.5
47	249.8	4.2
48	249.2	5.4
49	249.9	4.3
50	250.7	5.5
51	252.2	4.2
52	251.5	5.3
53 f	250.8	1.5
54	250.4	4.1
55	249.9	5.4
56	250.3	4.1
57	250.8	5.6
58	249.4	4.3
59	251.1	5.5
60	250.3	4.3
61	250.1	5.7
62	251.6	4.1
63	251.0	5.5
64	250.0	4.1
65	249.4	5.7
66 f	250.7	1.5
67	250.0	4.2
68	250.7	6.0
69	248.7	4.2
70	249.0	5.7
71	250.0	4.2
72	249.7	5.6
73	249.8	4.2
74	249.4	5.8
75	250.0	4.1
76	251.1	6.0
77	252.5	4.3
78	249.6	5.6

CHIP 3		
CH	M	STD
0 r	250.0	0.0
1 r	325.7	11.4
2 r	250.5	0.7
3	249.3	6.4
4	250.6	4.5
5	249.1	6.4
6	250.2	4.6
7	249.8	6.5
8	250.7	4.5
9	250.3	6.1
10	250.5	4.3
11	251.1	5.9
12	250.5	4.4
13	251.4	6.0
14	251.4	4.4
15 f	250.1	1.7
16	251.0	6.0
17	251.1	4.4
18	249.1	6.0
19	251.2	4.4
20	248.8	6.0
21	251.0	4.7
22	249.1	5.5
23	252.4	4.3
24	250.0	5.8
25	251.8	4.3
26	248.9	5.6
27	252.3	4.7
28 f	250.0	1.8
29	249.6	5.9
30	249.8	4.5
31	250.9	5.5
32	250.1	4.3
33	251.1	5.5
34	252.5	4.5
35	249.4	5.4
36	250.2	4.2
37	249.5	5.3
38	251.8	4.3
39	249.5	5.2
40	250.2	4.3
41	249.9	4.2
42	251.4	5.6
43	250.4	4.1
44	251.3	5.5
45	250.2	4.3
46	250.9	5.6
47	251.2	4.2
48	251.8	5.6
49	250.0	4.1
50	249.1	5.7
51	251.1	4.2
52	251.1	5.7
53 f	250.7	1.6
54	250.3	4.3
55	250.0	5.8
56	250.6	4.3
57	249.4	5.8
58	249.6	4.3
59	250.4	6.0
60	249.3	4.2
61	249.8	5.6
62	249.6	4.2
63	251.0	5.7
64	250.6	4.2
65	249.5	5.8
66 f	250.0	1.5
67	251.9	4.1
68	249.8	5.9
69	249.5	4.3
70	249.5	6.2
71	250.2	4.1
72	250.5	6.0
73	250.8	4.4
74	250.8	6.2
75	250.6	4.4
76	249.9	6.2
77	249.3	4.6
78	251.9	6.2

CHIP 4		
CH	M	STD
0 r	250.0	0.0
1 r	419.8	9.9
2 r	250.2	0.7
3	249.5	6.4
4	250.7	4.7
5	251.0	6.3
6	250.5	4.7
7	248.9	6.0
8	249.8	5.0
9	248.5	5.9
10	250.0	4.5
11	249.7	5.8
12	250.1	4.7
13	250.5	5.7
14	250.4	4.6
15 f	250.0	1.7
16	250.0	5.8
17	250.6	4.4
18	249.6	5.7
19	250.4	4.3
20	250.7	5.6
21	250.5	4.5
22	249.9	5.4
23	250.0	4.5
24	249.0	5.5
25	250.3	4.8
26	249.6	5.3
27	249.3	4.5
28 f	249.2	1.7
29	249.8	5.2
30	250.0	4.7
31	250.2	5.3
32	249.7	4.8
33	250.3	5.4
34	250.6	4.7
35	250.3	5.2
36	250.8	4.6
37	250.3	5.2
38	249.3	4.8
39	249.0	5.0
40	249.1	4.5
41	249.7	4.0
42	250.7	5.1
43	248.3	4.2
44	251.7	5.5
45	249.9	4.1
46	250.7	5.4
47	250.1	4.2
48	250.2	5.4
49	250.2	4.2
50	249.6	5.2
51	249.2	4.1
52	249.9	5.4
53 f	250.2	1.5
54	250.4	4.2
55	251.1	5.3
56	249.0	4.3
57	250.6	5.3
58	250.2	4.1
59	250.3	5.6
60	250.1	4.5
61	250.6	5.3
62	249.2	3.9
63	250.0	5.7
64	249.1	4.3
65	249.8	5.4
66 f	250.1	1.5
67	247.6	4.3
68	250.4	5.6
69	249.2	4.2
70	250.1	5.8
71	250.2	4.1
72	251.1	5.7
73	249.5	4.1
74	251.6	5.7
75	251.1	4.1
76	249.8	6.0
77	249.1	4.0
78	250.8	5.9

CHIP 5		
CH	M	STD
0 r	250.0	0.0
1 r	311.2	10.1
2 r	250.3	0.7
3	250.1	6.1
4	249.8	4.8
5	249.4	6.1
6	249.4	4.6
7	250.4	6.0
8	248.3	4.7
9	250.6	5.8
10	248.9	4.5
11	250.0	5.8
12	250.8	4.5
13	250.3	5.8
14	250.1	4.5
15 f	250.6	1.8
16	250.9	5.6
17	249.4	4.5
18	250.7	5.5
19	250.3	4.9
20	248.9	5.6
21	249.9	4.7
22	250.2	5.7
23	250.9	5.0
24	248.9	5.3
25	250.1	4.5
26	250.6	5.3
27	249.6	4.4
28 f	250.2	1.7
29	250.0	5.4
30	249.5	4.5
31	249.7	5.6
32	252.3	4.5
33	249.1	5.3
34	249.7	4.5
35	251.5	5.3
36	249.8	4.6
37	250.5	5.3
38	250.8	4.5
39	251.6	4.8
40	251.3	4.5
41	250.7	4.2
42	251.9	5.3
43	250.5	4.2
44	250.8	5.2
45	251.1	4.0
46	250.8	5.2
47	248.6	4.2
48	250.5	5.7
49	248.2	4.2
50	250.7	5.3
51	249.5	4.3
52	249.5	5.5
53 f	249.6	1.4
54	248.8	4.1
55	249.9	5.7
56	249.9	4.2
57	250.2	5.4
58	249.9	4.2
59	248.7	5.5
60	250.3	4.1
61	250.6	5.7
62	250.0	4.0
63	250.4	5.6
64	250.0	4.0
65	248.9	5.5
66 f	249.7	1.4
67	250.0	4.2
68	250.8	5.7
69	249.6	4.2
70	250.2	5.7
71	251.4	4.1
72	250.2	5.8
73	250.3	4.4
74	249.3	5.7
75	250.9	4.3
76	250.8	6.2
77	251.7	4.1
78	249.8	6.2

CHIP 6		
CH	M	STD
0 r	250.0	0.0
1 r	461.3	9.1
2 r	249.9	0.6
3	250.5	6.7
4	251.0	4.8
5	251.6	6.5
6	249.9	4.8
7	249.8	6.2
8	251.9	4.8
9	251.0	6.2
10	250.7	4.7
11	249.3	5.9
12	249.7	4.9
13	251.9	6.0
14	250.6	4.8
15 f	250.9	1.6
16	250.7	5.9
17	250.6	4.7
18	250.9	5.8
19	250.1	4.5
20	249.1	5.5
21	249.1	4.4
22	249.8	6.0
23	250.1	5.0
24	251.2	5.6
25	249.9	4.5
26	249.3	5.6
27	250.5	4.6
28 f	250.3	1.9
29	250.8	5.5
30	249.3	4.6
31	249.8	5.4
32	248.8	4.5
33	248.8	5.6
34	250.8	4.8
35	249.7	5.2
36	249.7	4.6
37	250.9	5.3
38	248.9	4.7
39	248.8	5.3
40	250.4	4.5
41	251.0	4.2
42	251.5	5.7
43	250.1	4.3
44	250.0	5.8
45	250.8	4.2
46	251.1	5.7
47	251.3	4.2
48	252.0	6.0
49	249.6	4.5
50	250.5	5.6
51	250.2	4.5
52	250.5	5.8
53 f	250.1	1.6
54	251.3	4.4
55	249.8	5.9
56	251.0	4.4
57	251.3	5.6
58	249.9	4.3
59	249.6	5.8
60	251.1	4.5
61	250.1	5.9
62	250.4	4.4
63	249.6	5.9
64	251.4	4.4
65	249.8	5.8
66 f	250.5	1.5
67	249.6	4.2
68	249.7	5.7
69	250.0	4.2
70	249.4	5.9
71	251.1	4.3
72	250.9	6.0
73	250.5	4.3
74	249.8	6.4
75	252.3	4.4
76	250.8	6.5
77	250.8	4.5
78	249.9	6.4

CHIP 7		
CH	M	STD
0 r	250.0	0.0
1 r	416.6	8.9
2 r	249.9	0.7
3	249.3	6.7
4	251.6	4.5
5	250.3	6.4
6	251.4	4.7
7	248.6	6.1
8	249.8	4.5
9	250.4	6.2
10	250.1	4.5
11	250.4	6.1
12	251.1	4.6
13	250.3	6.2
14	248.5	4.6
15 f	250.0	1.7
16	249.8	6.0
17	247.8	4.4
18	249.5	5.8
19	250.4	4.4
20	250.0	5.8
21	250.0	4.5
22	250.7	5.5
23	249.7	4.3
24	250.6	5.6
25	249.7	4.4
26	250.6	5.4
27	250.8	4.3
28 f	250.3	1.9
29	250.1	5.4
30	250.6	4.5
31	250.0	5.8
32	249.1	4.4
33	251.5	5.4
34	251.3	4.4
35	249.8	5.4
36	249.3	4.4
37	251.4	5.3
38	250.6	4.4
39	249.9	4.9
40	249.7	4.5
41	251.0	4.2
42	250.4	5.3
43	250.0	4.2
44	249.4	5.3
45	250.3	4.4
46	249.7	5.7
47	250.1	4.3
48	250.2	5.3
49	248.2	4.2
50	250.7	5.4
51	250.0	4.0
52	249.6	5.5
53 f	250.1	1.4
54	249.5	4.3
55	250.0	5.2
56	249.9	4.1
57	251.1	5.5
58	248.3	4.2
59	250.3	5.3
60	250.8	4.3
61	250.4	5.5
62	249.7	4.1
63	250.1	5.3
64	250.8	4.3
65	251.5	5.3
66 f	250.6	1.4
67	250.5	4.3
68	249.3	5.2
69	250.5	4.0
70	249.0	5.7
71	249.5	4.2
72	250.1	5.6
73	249.3	4.0
74	249.9	5.5
75	251.5	4.0
76	250.2	5.5
77	249.2	4.5
78	250.1	5.6