

Fec test report:

Date: 2021-04-14 15:18:47

Tester name: Boris

Test#1 Monitoring values

Passed

0	FEC label	069	OK
1	FEC DC2438 ID	8a0000024db46d26	OK
2	FEC_T (to 35°C)	21.562	OK
3	FEC_Vdd (3.2V to 3.4V)	3.300	OK
4	FEC_I (1.1A to 1.5A)	1.211	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

Test#2 Slow control registers:

Passed

Test#3 Pedestal run:

Passed

Mean in range (245.0:255.0), 3.5 < rms < 8.0 (fpm 4.0)

0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns

Passed

0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run

Passed

0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3145	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3082	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3073	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3123	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3052	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3075	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3107	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3007	OK

FEC test final result:

Passed

Monitoring test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
2	fe 0 moni T 0	0	0 Tdcm(0) Fem(00) FEC_T: 21.562 degC
3	fe 0 moni V 0	0	0 Tdcm(0) Fem(00) FEC_Vdd: 3.300 V
4	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
5	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
6	fe 0 pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
7	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
8	fe 0 moni I 0	0	0 Tdcm(0) Fem(00) FEC_I: 1.211 A
9	fe 0 moni S 0	0	0 Tdcm(0) Fem(00) FEC_Serial: 8a0000024db46d26

Slow control registers test			
NO	Command	Error	Response
0	fe fec_mask 0x2	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x200000
1	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
2	fe fec_enable 1	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x40000
3	fe fec_enable	0	0 Tdcm(0) Fem(00) Reg(1) = 0x12248000 (304381952) FEC_Enable: 1
4	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
5	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
6	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
7	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
8	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
9	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
10	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
11	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
12	fe 0 after 0 wrchk 3 0x0 0x0101 0x0101	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x101 0x101 (1 chip verified)
13	fe 0 after 1 wrchk 3 0x0 0x0202 0x0202	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x202 0x202 (1 chip verified)
14	fe 0 after 2 wrchk 3 0x0 0x0303 0x0303	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x303 0x303 (1 chip verified)
15	fe 0 after 3 wrchk 3 0x0 0x0404 0x0404	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x404 0x404 (1 chip verified)
16	fe 0 after 4 wrchk 3 0x0 0x0505 0x0505	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x505 0x505 (1 chip verified)
17	fe 0 after 5 wrchk 3 0x0 0x0606 0x0606	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x606 0x606 (1 chip verified)
18	fe 0 after 6 wrchk 3 0x0 0x0707 0x0707	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x707 0x707 (1 chip verified)
19	fe 0 after 7 wrchk 3 0x0 0x0808 0x0808	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x808 0x808 (1 chip verified)
20	fe 0 after 0 read 3	0	0 Tdcm(0) Fem(00) After(0) Reg(3): 0x0 0x101 0x101
21	fe 0 after 1 read 3	0	0 Tdcm(0) Fem(00) After(1) Reg(3): 0x0 0x202 0x202
22	fe 0 after 2 read 3	0	0 Tdcm(0) Fem(00) After(2) Reg(3): 0x0 0x303 0x303
23	fe 0 after 3 read 3	0	0 Tdcm(0) Fem(00) After(3) Reg(3): 0x0 0x404 0x404
24	fe 0 after 4 read 3	0	0 Tdcm(0) Fem(00) After(4) Reg(3): 0x0 0x505 0x505
25	fe 0 after 5 read 3	0	0 Tdcm(0) Fem(00) After(5) Reg(3): 0x0 0x606 0x606
26	fe 0 after 6 read 3	0	0 Tdcm(0) Fem(00) After(6) Reg(3): 0x0 0x707 0x707
27	fe 0 after 7 read 3	0	0 Tdcm(0) Fem(00) After(7) Reg(3): 0x0 0x808 0x808
28	fe 0 after 0 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
29	fe 0 after 1 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
30	fe 0 after 2 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
31	fe 0 after 3 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(3) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
32	fe 0 after 4 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(4) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
33	fe 0 after 5 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(5) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
34	fe 0 after 6 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(6) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)
35	fe 0 after 7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(7) Reg(3) <- 0x0 0x0 0x0 (1 chip verified)

ADC pattern test			
NO	Command	Error	Response
0	fe 0 mode after	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x400
1	fe 0 test_mode	0	0 Tdcm(0) Fem(00) Reg(5) = 0x3042000 (50601984) Test_Mode: 0
2	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x2020003 (Event_Builder: COLLECTING_SOE_WAIT_FEM_PKT Current
3	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x2020003 (Trigger_Generator: WAITING_TRIG)
4	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x2020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
5	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x3 (Aligned_SCA_Write)
6	daq 0xFFFFFFFF F	0	0 Tdcm(0): daq paused
7	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
8	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
10	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
11	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
12	fe adc 0 model AD9637	0	0 Tdcm(0) Fem(00) ADC_model <- 3 (AD9637)
13	fe adc 0 write 0x14 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(20) <- 0x0 (0)
14	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
15	fe adc 0 write 0x5 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x1 (1)
16	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
17	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
18	fe adc 0 write 0x5 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x2 (2)

19	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
20	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
21	fe adc 0 write 0x5 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x4 (4)
22	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
23	fe adc 0 write 0x4 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x0 (0)
24	fe adc 0 write 0x5 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x8 (8)
25	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
26	fe adc 0 write 0x4 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x1 (1)
27	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
28	fe adc 0 write 0xD 0x01	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x1 (1)
29	fe adc 0 write 0x4 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x2 (2)
30	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
31	fe adc 0 write 0xD 0x02	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x2 (2)
32	fe adc 0 write 0x4 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x4 (4)
33	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
34	fe adc 0 write 0xD 0x04	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x4 (4)
35	fe adc 0 write 0x4 0x08	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0x8 (8)
36	fe adc 0 write 0x5 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0x0 (0)
37	fe adc 0 write 0xD 0x07	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x7 (7)
38	fe 0 subtract_ped 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
39	fe 0 zero_suppress 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
40	fe 0 zs_pre_post 4 8	0	0 Tdcm(0) Fem(00) Reg(5) <- 0xc4
41	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
42	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
43	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
44	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
45	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
46	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
47	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
48	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH_SCA_START auto-clear)
49	be 0 trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x1000
50	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0
51	be 0 state eb	0	0 Tdcm(0) Reg(27) = 0x48020003 (Event_Builder: COLLECTING_SOE_WAIT_FEM_PKT Current)
52	be 0 state tg	0	0 Tdcm(0) Reg(27) = 0x48020003 (Trigger_Generator: FEM_BUSY_NO_BUSY_MISS)
53	be 0 state pm	0	0 Tdcm(0) Reg(27) = 0x48020003 (Packet_Mover: WAIT_PKT_FIFO_NE)
54	fe 0 state	0	0 Tdcm(0) Fem(00) State = 0x11 (Aligned Dev_Ready)
55	fe adc 0 write 0x4 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(04) <- 0xf (15)
56	fe adc 0 write 0x5 0x0F	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(05) <- 0xf (15)
57	fe adc 0 write 0xD 0x00	0	0 Tdcm(0) Fem(00) Front-End ADC Reg(13) <- 0x0 (0)

Pulser test

NO	Command	Error	Response
0	daq 0xFFFFFFFF F	0	0 Tdcm(0): daq paused
1	fe 0 after 0:7 wrchk 3 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
2	fe 0 after 0:7 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
3	fe 0 emit_hit_cnt 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
4	fe 0 emit_empty_ch 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
5	fe 0 emit_lst_cell_rd 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
6	fe 0 keep_rst 0	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x0
7	fe 0 skip_rst 2	0	0 Tdcm(0) Fem(00) Reg(0) <- 0x40000
8	fe 0 test_enable 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
9	fe 0 test_mode 1	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x400
10	fe 0 tdata A 0x1FF	0	0 Tdcm(0) Fem(00) TestData: linear ramp from 0 to 510
11	fe 0 test_zbt 0	0	0 Tdcm(0) Fem(00) Reg(5) <- 0x0
12	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
13	fe 0 asic_mask	0	0 Tdcm(0) Fem(00) Reg(9) = 0x80 (128) Asic_Mask: 0x0
14	fe 0 pulser 0 enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
15	fe 0 pulser 0 ft_enable 0	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x0
16	fe 0 pulser 0 model T2K2	0	0 Tdcm(0) Fem(00) pulser_DAC <- 3 (T2K2)
17	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
18	fe 0 pulser 0 ampl 16383	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3fff
19	fe 0 pulser 0 delay 3000	0	0 Tdcm(0) Fem(00) Reg(3) <- 0xbb8
20	fe pulser load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
21	fe 0 pulser 0 enable 1	0	0 Tdcm(0) Fem(00) Reg(3) <- 0x10000
22	be 0 eb keep_fem_soe 0	0	0 Tdcm(0) Reg(0) <- 0x0
23	be 0 eb check_ev_nb 1	0	0 Tdcm(0) Reg(0) <- 0x800000
24	be 0 eb check_ev_ts 1	0	0 Tdcm(0) Reg(0) <- 0x1000000
25	be 0 eb ts_tolerance 0	0	0 Tdcm(0) Reg(0) = 0x1a40000 (27525120) Time_Stamp_Tolerance +/-: 0
26	be 0 event_limit 0x0	0	0 Tdcm(0) Reg(6) <- 0x0
27	be 0 trig_rate 0 50	0	0 Tdcm(0) Reg(6) <- 0x32
28	be 0 trig_delay 0 0	0	0 Tdcm(0) Reg(8) <- 0x0
29	be 0 trig_delay 1 0	0	0 Tdcm(0) Reg(8) <- 0x0
30	be 0 trig_delay 2 0	0	0 Tdcm(0) Reg(9) <- 0x0
31	be 0 trig_delay 3 0	0	0 Tdcm(0) Reg(9) <- 0x0
32	be 0 ss_trig_delay 0x4	0	0 Tdcm(0) Reg(14) <- 0x4
33	be 0 ss_trig_ena 1	0	0 Tdcm(0) Reg(6) <- 0x10000
34	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done

35	be 0 restart	0	0 Tdcm(0) Reg(5) <- restart done
36	be 0 isobus 0x0C	0	0 Tdcm(0) Reg(5) <- 0x0000000c (CLR_EVCNT CLR_TSTAMP auto-clear)
37	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
38	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
39	fe 0 asic_mask 0xfffe	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xfffe0000
40	fe 0 after 0 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(0) Reg(1) <- Test_mode=calibration
41	fe 0 after 0 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
42	fe 0 after 0 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(0) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
43	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
44	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
45	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
46	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
47	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
48	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
49	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
50	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
51	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
52	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
53	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
54	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
55	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
56	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
57	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
58	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
59	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
60	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
61	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
62	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
63	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
64	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
65	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
66	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
67	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
68	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
69	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
70	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
71	fe 0 asic_mask 0xffffd	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffffd0000
72	fe 0 after 1 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(1) Reg(1) <- Test_mode=calibration
73	fe 0 after 1 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
74	fe 0 after 1 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(1) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
75	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
76	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
77	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
78	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
79	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
80	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
81	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
82	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
83	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
84	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
85	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
86	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
87	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
88	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
89	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
90	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
91	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
92	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
93	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
94	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
95	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
96	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
97	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
98	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
99	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
100	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
101	fe 0 after 0:7 wrchk 3 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(3) <- 0x0 0x0 0x0 (8 chip verified)
102	fe 0 after 0:7 wrchk 4 0x0 0x0000 0x0000	0	0 Tdcm(0) Fem(00) After(0:7) Reg(4) <- 0x0 0x0 0x0 (8 chip verified)
103	fe 0 asic_mask 0xffffb	0	0 Tdcm(0) Fem(00) Reg(9) <- 0xffffb0000
104	fe 0 after 2 test_mode 0x1	0	0 Tdcm(0) Fem(00) After(2) Reg(1) <- Test_mode=calibration
105	fe 0 after 2 wrchk 3 0x0 0x1000 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(3) <- 0x0 0x1000 0x0 (1 chip verified)
106	fe 0 after 2 wrchk 4 0x0 0x0 0x0	0	0 Tdcm(0) Fem(00) After(2) Reg(4) <- 0x0 0x0 0x0 (1 chip verified)
107	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
108	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
109	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
110	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
111	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
112	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff

269	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
270	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
271	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
272	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
273	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
274	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
275	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
276	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
277	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
278	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
279	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
280	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
281	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
282	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
283	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
284	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
285	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
286	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
287	fe 0 pulser 0 base 16383	0	0 Tdcm(0) Fem(00) Pulser_Base <- 0x3fff
288	fe pulser 0 load	0	0 Tdcm(0) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
289	fe 0 moni A 0	0	0 Tdcm(0) Fem(00) FEC_Vad: 1.950 V
290	fe 0 pulser 0 ampl 15900	0	0 Tdcm(0) Fem(00) Pulser_Amplitude <- 0x3e1c
291	be 0 isobus 0x60	0	0 Tdcm(0) Reg(5) <- 0x00000060 (WCK_SYNCH SCA_START auto-clear)
292	fe 0 asic_mask 0x0	0	0 Tdcm(0) Fem(00) Reg(9) <- 0x0
293	be 0 trig_ena 0	0	0 Tdcm(0) Reg(6) <- 0x0

Pedestal data before centermean

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7					
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0	0r	0.0	0.0			
1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0	1r	511.0	0.0			
2r	276.7	0.7	2r	278.0	0.7	2r	301.1	0.7	2r	268.6	0.7	2r	316.6	0.7	2r	295.8	0.7	2r	306.7	0.7	2r	341.7	0.7			
3	261.1	5.7	3	250.3	5.5	3	292.3	5.2	3	279.3	5.7	3	327.8	5.8	3	227.5	5.6	3	323.5	5.5	3	344.4	5.3			
4	221.9	4.5	4	223.3	4.3	4	275.7	4.5	4	195.4	4.4	4	277.8	5.2	4	195.3	5.0	4	284.6	4.5	4	343.2	4.6			
5	189.3	5.4	5	251.6	5.5	5	274.2	5.3	5	333.8	5.2	5	280.4	5.8	5	213.9	5.8	5	240.0	5.2	5	401.0	5.2			
6	164.2	4.7	6	349.8	4.4	6	380.6	4.8	6	221.8	4.4	6	253.6	4.7	6	245.7	4.7	6	362.7	4.5	6	310.5	4.3			
7	239.2	5.6	7	271.9	5.2	7	236.8	5.2	7	288.6	5.1	7	315.5	5.3	7	205.1	5.3	7	275.1	5.1	7	370.8	5.1			
8	203.6	4.7	8	189.2	4.5	8	282.4	4.4	8	349.4	4.4	8	305.2	4.4	8	220.5	4.5	8	280.3	4.5	8	305.7	4.4			
9	159.7	5.3	9	321.0	4.9	9	236.9	5.2	9	345.9	5.1	9	260.0	5.3	9	181.6	5.4	9	270.1	5.4	9	383.4	5.0			
10	240.7	4.7	10	268.2	4.5	10	304.1	4.3	10	266.8	4.4	10	326.1	4.6	10	200.2	4.7	10	284.1	4.5	10	274.8	4.3			
11	242.6	5.3	11	278.1	5.0	11	215.1	4.8	11	200.7	4.9	11	288.3	5.4	11	208.1	5.2	11	234.2	5.2	11	314.7	5.1			
12	236.2	4.7	12	274.1	4.3	12	176.0	4.3	12	288.1	4.6	12	355.7	4.5	12	243.4	4.5	12	328.9	4.5	12	295.5	4.4			
13	189.3	5.5	13	242.5	4.8	13	258.2	5.0	13	215.8	4.9	13	267.4	5.2	13	245.9	4.9	13	330.8	5.1	13	354.6	5.0			
14	214.1	4.6	14	226.1	4.3	14	225.5	4.2	14	360.8	4.5	14	285.3	4.7	14	216.8	4.5	14	316.1	4.2	14	259.0	4.5			
15 f	151.9	1.8	15 f	237.8	1.6	15 f	129.3	1.8	15 f	213.0	1.7	15 f	330.3	1.7	15 f	216.8	1.7	15 f	257.9	1.6	15 f	261.2	1.7			
16	250.3	5.1	16	223.1	4.8	16	251.7	5.0	16	258.3	5.1	16	275.6	5.4	16	241.3	5.3	16	291.3	4.9	16	271.6	5.1			
17	151.9	4.7	17	200.4	4.3	17	198.5	4.5	17	296.4	4.1	17	265.1	4.8	17	182.8	4.5	17	262.3	4.6	17	269.9	4.2			
18	305.7	5.2	18	227.6	5.0	18	229.6	5.1	18	340.1	5.2	18	245.1	5.4	18	171.9	4.9	18	237.2	5.1	18	349.8	5.0			
19	258.4	4.5	19	238.7	4.2	19	281.6	4.3	19	245.8	4.2	19	210.9	4.5	19	201.8	4.6	19	247.8	4.3	19	305.3	4.3			
20	294.5	5.0	20	186.8	5.0	20	300.9	4.9	20	248.2	5.1	20	316.3	4.9	20	229.9	4.9	20	257.6	4.8	20	316.6	4.8			
21	212.6	4.3	21	257.3	4.2	21	219.8	4.2	21	161.1	4.2	21	219.7	4.3	21	268.0	4.5	21	222.6	4.2	21	352.7	4.2			
22	172.6	5.3	22	228.9	4.9	22	237.1	4.7	22	250.9	4.8	22	240.8	5.2	22	224.2	5.0	22	233.8	5.1	22	244.6	4.6			
23	198.9	4.4	23	308.0	4.3	23	253.9	4.3	23	201.0	4.2	23	270.1	4.5	23	211.1	4.6	23	236.2	4.5	23	384.7	4.3			
24	176.5	5.0	24	230.2	4.7	24	213.9	4.8	24	236.8	4.7	24	224.0	5.0	24	260.6	5.0	24	263.8	4.9	24	300.9	4.9			
25	187.5	4.3	25	228.3	4.2	25	196.7	4.5	25	270.6	4.2	25	285.8	4.3	25	225.4	4.6	25	280.2	4.6	25	225.5	4.6			
26	165.2	5.0	26	159.9	5.0	26	318.3	4.9	26	242.2	4.9	26	296.6	5.2	26	240.9	4.8	26	269.0	5.0	26	298.6	4.7			
27	168.0	4.3	27	268.5	4.0	27	252.3	4.3	27	243.8	4.1	27	291.7	4.5	27	238.9	4.3	27	327.5	4.3	27	297.9	4.3			
28 f	106.2	1.9	28 f	276.1	1.8	28 f	264.3	1.8	28 f	295.0	1.7	28 f	254.5	1.8	28 f	296.5	1.7	28 f	248.1	1.8	28 f	338.5	1.7			
29	251.7	4.9	29	279.1	4.7	29	183.9	4.9	29	309.7	4.7	29	308.1	5.1	29	224.2	4.9	29	295.1	4.9	29	258.9	5.0			
30	147.3	4.4	30	278.2	4.6	30	241.2	4.4	30	218.4	4.2	30	284.4	4.8	30	235.6	4.3	30	267.8	4.5	30	319.0	4.1			
31	218.8	5.0	31	216.1	4.9	31	325.6	4.8	31	208.7	4.9	31	261.6	4.9	31	141.5	4.9	31	288.4	4.8	31	201.3	4.5			
32	221.3	4.5	32	220.0	4.5	32	266.5	4.2	32	286.3	4.4	32	265.4	4.3	32	286.0	4.2	32	294.7	4.3	32	238.5	4.2			
33	245.9	5.1	33	312.6	4.7	33	151.7	5.0	33	176.6	4.7	33	179.6	4.8	33	258.2	4.9	33	248.8	4.8	33	276.6	4.7			
34	192.5	4.8	34	214.5	4.3	34	259.5	4.1	34	277.9	4.3	34	350.2	4.3	34	237.7	4.4	34	309.2	4.4	34	308.5	4.3			
35	187.4	4.8	35	229.5	5.1	35	277.9	4.5	35	173.7	4.7	35	331.9	5.0	35	247.0	5.0	35	269.8	4.9	35	291.5	4.8			
36	241.2	4.4	36	277.0	4.3	36	254.6	4.4	36	286.1	4.3	36	373.4	4.6	36	196.1	4.3	36	323.9	4.4	36	327.7	4.1			
37	175.2	4.9	37	355.7	4.9	37	239.3	4.6	37	191.7	4.8	37	271.1	4.8	37	294.4	4.7	37	257.4	4.6	37	301.4	4.8			
38	258.4	4.2	38	260.9	4.2	38	203.9	4.0	38	313.8	4.1	38	401.8	4.1	38	236.5	4.6	38	287.3	4.7	38	383.8	4.3			
39	151.6	4.8	39	356.8	4.6	39	213.9	4.6	39	212.7	4.5	39	271.3	4.9	39	328.0	4.6	39	295.1	4.8	39	231.1	4.9			
40	300.1	4.8	40	348.8	4.4	40	258.5	4.2	40	263.1	4.3	40	333.3	4.5	40	274.9	4.4	40	227.9	4.3	40	307.6	4.1			
41	166.5	4.2	41	269.9	4.2	41	251.0	4.3	41	263.3	4.1	41	231.7	4.2	41	290.6	4.1	41	241.0	4.3	41	302.5	4.0			
42	227.0	4.8	42	275.6	4.5	42	302.5	4.7	42	200.6	4.5	42	349.9	4.9	42	204.8	4.9	42	223.7	4.9	42	257.4	4.8			
43	166.9	4.7	43	253.3	4.1	43	235.5	4.1	43	284.9	4.1	43	185.2	4.1	43	320.9	4.3	43	320.8	4.1	43	308.8	3.9			
44	204.2	4.7	44	248.7	4.4	44	206.7	4.3	44	218.5	4.7	44	374.0	4.9	44	187.2	5.0	44	359.0	4.9	44	314.5	4.8			
45	191.1	4.3	45	173.1	4.1	45	268.7	4.0	45	252.2	4.1	45	297.4	4.0	45	187.7	4.2	45	277.5	4.2	45	386.3	4.2			
46	224.1	4.8	46	292.6	4.5	46	230.5	4.8	46	214.3	4.7	46	264.6	5.0	46	229.2	4.7	46	189.2	4.8	46	373.8	4.6			
47	247.8	4.3	47	290.2	4.0	47	233.7	3.9	47	223.5	4.0	47	252.5	4.1	47	256.1	3.9	47	286.0	4.0	47	292.9	3.9			
48	241.9	4.8	48	210.1	4.7	48	322.8	4.7	48	294.8	4.5	48	279.2	4.8	48	231.5	4.8	48	254.8	4.9	48	254.2	4.7			
49	190.8	4.3	49	220.2	4.3	49	216.4	4.1	49	229.9	4.1	49	261.1	4.2	49	194.4	4.3	49	286.3	4.3	49	371.3	3.9			
50	287.6	5.1	50	224.0	4.7	50	263.8	5.0	50	251.5	4.7	50	193.3	4.8	50	225.2	4.8	50	260.5	4.7	50	217.3	4.7			
51	307.2	4.3	51	367.6	4.1	51	217.4	4.3	51	195.2	4.1	51	237.0	4.2	51	263.7	4.5	51	300.4	4.3	51	323.7	4.0			
52	290.6	5.0	52	303.5	4.6	52	288.8	4.7	52	235.1	4.8	52	291.0	4.9	52	254.3	4.8	52	312.1	5.0	52	259.6	4.9			
53 f	206.7	1.8	53 f	254.7	1.7	53 f	263.7	1.6	53 f	297.8	1.6	53 f	256.9	1.7	53 f	280.5	1.5	53 f	303.0	1.7	53 f	328.4	1.4			
54	184.2	4.1	54	275.4	4.5	54	266.3	4.2	54	259.0	4.2	54	265.7	4.2	54	267.1	4.3	54	212.4	4.1	54	327.5	4.0			
55	95.6	4.9	55	261.4	4.6	55	294.5	4.7	55	271.1	4.5	55	304.6	4.8	55	219.7	4.9	55	283.5	4.8	55	308.6	4.5			
56	244.1	4.5	56	147.1	4.1	56	249.1	4.2	56	203.2	4.1	56	282.9	4.1	56	186.2	4.3	56	255.8	4.4	56	275.2	4.0			
57	240.0	5.0	57	216.2	4.7	57	230.7	4.6	57	316.2	4.5	57	287.2	5.0	57	219.9	4.6	57	307.9	4.8	57	407.8	4.8			
58	147.3	4.1	58	292.6	4.2	58	315.6	4.1	58	236.6	4.1	58	320.1	4.3	58	262.5	4.1	58	285.7	4.2	58					

Pedestal after centermean.

CHIP 0			CHIP 1			CHIP 2			CHIP 3			CHIP 4			CHIP 5			CHIP 6			CHIP 7					
CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD	CH	M	STD
0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0	0 r	250.0	0.0
1 r	365.5	9.5	1 r	319.4	9.4	1 r	378.8	9.6	1 r	328.1	11.1	1 r	423.0	9.9	1 r	312.6	10.3	1 r	461.8	9.0	1 r	421.6	8.6	1 r	421.6	8.6
2 r	250.0	0.7	2 r	250.1	0.7	2 r	250.3	0.7	2 r	249.8	0.7	2 r	249.7	0.7	2 r	249.9	0.7	2 r	249.9	0.7	2 r	249.9	0.7	2 r	249.8	0.7
3	251.6	6.8	3	250.2	6.4	3	250.3	6.3	3	248.9	6.1	3	249.3	7.0	3	249.3	6.9	3	248.6	6.8	3	249.3	6.4	3	249.3	6.4
4	250.1	4.9	4	251.4	4.5	4	248.8	4.5	4	248.3	4.6	4	249.6	4.9	4	252.1	4.9	4	251.7	4.7	4	251.7	4.7	4	250.6	4.5
5	250.4	6.3	5	249.8	6.1	5	250.3	6.3	5	249.8	6.4	5	250.3	6.7	5	250.4	6.8	5	250.6	6.7	5	250.6	6.7	5	250.4	6.5
6	249.7	4.9	6	251.2	4.4	6	249.0	4.6	6	249.2	4.6	6	247.9	5.2	6	248.2	4.6	6	250.4	4.9	6	249.7	4.6	6	249.7	4.6
7	249.8	6.4	7	250.4	6.2	7	250.7	6.1	7	250.2	6.4	7	249.0	6.7	7	249.4	6.3	7	248.9	6.4	7	249.7	5.9	7	249.7	5.9
8	249.0	4.8	8	249.6	4.4	8	250.8	4.7	8	249.9	4.6	8	250.7	4.6	8	250.3	4.6	8	250.1	4.7	8	249.3	4.6	8	249.3	4.6
9	249.5	6.7	9	249.0	6.1	9	251.4	6.0	9	250.7	5.9	9	249.9	6.2	9	249.9	6.1	9	250.8	6.1	9	250.1	5.9	9	250.1	5.9
10	250.2	4.5	10	249.1	4.6	10	249.6	4.7	10	249.8	4.5	10	249.9	4.8	10	250.8	4.7	10	250.9	4.5	10	250.2	4.4	10	250.2	4.4
11	249.2	6.2	11	251.1	5.8	11	250.3	5.8	11	250.4	5.8	11	250.6	6.0	11	249.1	6.0	11	250.6	6.3	11	250.4	5.9	11	250.4	5.9
12	250.4	4.6	12	249.4	4.5	12	250.6	4.5	12	249.7	4.4	12	250.2	4.7	12	251.3	4.7	12	251.0	4.6	12	250.6	4.6	12	250.6	4.6
13	250.1	6.3	13	250.9	5.7	13	249.3	5.8	13	250.5	5.8	13	251.8	6.3	13	250.2	6.0	13	250.9	6.0	13	249.2	6.1	13	249.2	6.1
14	250.0	4.7	14	250.5	4.4	14	250.8	4.5	14	248.6	4.6	14	250.6	4.8	14	248.8	4.6	14	249.1	4.8	14	250.8	4.8	14	250.8	4.8
15 f	250.1	1.7	15 f	249.9	1.6	15 f	250.6	1.8	15 f	250.4	1.7	15 f	250.4	1.7	15 f	249.7	1.6	15 f	250.3	1.7	15 f	250.3	1.7	15 f	250.8	1.6
16	249.2	5.8	16	250.3	5.7	16	249.9	5.7	16	250.2	5.7	16	248.3	6.1	16	250.1	5.8	16	248.6	5.7	16	249.5	5.8	16	249.5	5.8
17	249.7	4.5	17	249.1	4.5	17	250.5	4.4	17	251.0	4.5	17	250.8	5.0	17	249.3	4.7	17	250.5	4.6	17	249.7	4.6	17	249.7	4.6
18	251.3	6.0	18	250.4	5.5	18	250.5	5.5	18	249.8	5.5	18	250.0	5.9	18	249.7	5.8	18	250.9	5.9	18	250.7	5.8	18	250.7	5.8
19	251.2	4.5	19	249.5	4.5	19	251.5	4.6	19	249.6	4.3	19	250.7	4.5	19	250.8	4.5	19	249.9	4.7	19	250.8	4.5	19	250.8	4.5
20	251.1	5.7	20	248.1	5.5	20	249.5	5.7	20	251.5	5.5	20	249.5	5.9	20	248.6	5.9	20	248.4	5.8	20	249.9	5.6	20	249.9	5.6
21	250.4	4.5	21	248.9	4.5	21	249.4	4.4	21	250.5	4.7	21	249.9	4.8	21	249.2	4.5	21	248.9	4.6	21	249.5	4.6	21	249.5	4.6
22	250.2	6.0	22	249.8	5.7	22	250.6	5.5	22	251.0	5.5	22	249.4	5.8	22	251.4	5.7	22	250.5	5.8	22	249.1	5.7	22	249.1	5.7
23	250.3	4.9	23	249.6	4.4	23	249.9	4.5	23	250.6	4.6	23	250.4	4.6	23	250.2	4.6	23	250.4	4.7	23	250.7	4.3	23	250.7	4.3
24	251.8	5.6	24	250.1	5.8	24	250.0	5.5	24	249.8	5.3	24	250.4	6.0	24	250.0	5.8	24	251.1	5.7	24	251.1	5.4	24	251.1	5.4
25	250.4	4.8	25	250.3	4.5	25	250.2	4.5	25	250.5	4.3	25	251.6	4.6	25	250.3	4.5	25	249.8	4.6	25	248.4	4.3	25	248.4	4.3
26	250.9	5.8	26	249.5	5.3	26	249.9	5.6	26	249.8	5.4	26	248.8	5.7	26	250.7	6.0	26	249.7	5.7	26	250.2	5.6	26	250.2	5.6
27	250.3	4.5	27	251.4	4.3	27	250.6	4.8	27	250.3	4.4	27	249.3	4.8	27	249.0	4.6	27	249.2	4.7	27	249.4	4.5	27	249.4	4.5
28 f	250.9	1.9	28 f	250.8	1.8	28 f	250.3	1.8	28 f	250.3	1.7	28 f	250.5	1.8	28 f	250.0	1.8	28 f	250.3	1.9	28 f	249.1	1.7	28 f	249.1	1.7
29	250.5	5.7	29	251.0	5.3	29	248.5	5.7	29	250.3	5.8	29	250.2	5.8	29	251.4	5.7	29	251.0	5.7	29	249.2	5.7	29	249.2	5.7
30	250.8	4.4	30	250.0	4.4	30	250.9	4.3	30	250.0	4.3	30	250.0	4.6	30	250.0	4.5	30	250.2	4.5	30	250.7	4.5	30	250.7	4.5
31	250.5	5.9	31	251.3	5.3	31	248.0	5.5	31	251.2	5.4	31	249.7	5.7	31	250.8	5.7	31	250.8	5.5	31	250.7	5.3	31	250.7	5.3
32	250.3	4.5	32	248.6	4.6	32	249.7	4.3	32	251.1	4.5	32	249.8	4.7	32	251.1	4.5	32	250.7	4.5	32	249.2	4.6	32	249.2	4.6
33	249.1	5.5	33	250.7	5.2	33	249.1	5.5	33	249.8	5.3	33	250.3	5.7	33	250.2	5.4	33	249.4	6.0	33	248.8	5.2	33	248.8	5.2
34	250.6	4.6	34	251.3	4.3	34	249.7	4.5	34	251.2	4.5	34	249.0	4.7	34	249.3	4.6	34	251.6	4.4	34	250.7	4.3	34	250.7	4.3
35	250.7	5.7	35	251.2	5.2	35	251.3	5.3	35	250.7	5.4	35	251.1	5.5	35	252.0	5.7	35	251.1	5.5	35	250.2	5.4	35	250.2	5.4
36	250.8	4.4	36	249.2	4.3	36	251.2	4.5	36	250.3	4.4	36	249.9	4.6	36	250.4	4.8	36	250.7	4.5	36	249.8	4.3	36	249.8	4.3
37	251.2	5.5	37	251.8	5.0	37	250.2	5.2	37	249.8	5.3	37	251.0	5.3	37	252.4	5.3	37	250.8	5.7	37	249.3	5.2	37	249.3	5.2
38	250.8	4.6	38	250.7	4.6	38	249.3	4.3	38	249.3	4.3	38	249.8	4.7	38	249.0	4.7	38	250.8	4.5	38	250.9	4.9	38	250.9	4.9
39	249.9	5.1	39	250.2	5.0	39	249.9	5.1	39	249.4	5.0	39	250.4	5.4	39	249.1	5.3	39	249.9	5.1	39	249.9	5.0	39	249.9	5.0
40	250.1	4.3	40	249.9	4.2	40	249.9	4.6	40	249.1	4.3	40	250.7	4.7	40	249.1	4.6	40	250.1	4.6	40	250.7	4.3	40	250.7	4.3
41	250.2	4.3	41	250.3	4.2	41	250.3	4.3	41	250.9	4.3	41	249.3	4.3	41	249.1	4.1	41	250.6	4.2	41	250.8	4.2	41	250.8	4.2
42	250.7	5.4	42	248.1	5.2	42	249.8	5.4	42	249.8	5.1	42	248.8	5.8	42	250.3	5.7	42	249.9	5.8	42	250.3	5.5	42	250.3	5.5
43	250.2	4.6	43	250.4	4.3	43	249.7	4.3	43	249.7	4.2	43	250.4	4.2	43	249.6	4.4	43	251.0	4.4	43	249.6	4.0	43	249.6	4.0
44	249.6	5.5	44	250.7	5.3	44	249.8	5.3	44	249.8	5.3	44	250.4	5.8	44	250.9	5.6	44	250.1	5.7	44	250.0	5.5	44	250.0	5.5
45	250.8	4.4	45	251.5	4.2	45	250.4	4.1	45	250.4	4.2	45	250.2	4.2	45	248.8	4.2	45	250.5	4.4	45	249.8	4.3	45	249.8	4.3
46	251.2	5.4	46	251.1	5.4	46	249.9	5.1	46	250.7	5.3	46	249.7	5.8	46	249.8	5.5	46	250.9	5.6	46	250.2	5.4	46	250.2	5.4
47	250.2	4.4	47	250.4	4.2	47	250.2	4.2	47	249.7	4.2	47	248.9	4.1	47	250.8	4.4	47	250.2	4.2	47	250.5	4.4	47	250.5	4.4
48	248.5	5.6	48	248.9	5.3	48	250.2	5.2	48	249.4	5.5	48	249.9	5.9	48	250.1	5.6	48	250.6	5.5	48	250.3	5.5	48	250.3	5.5
49	248.9	4.3	49	250.3	4.3	49	251.7	4.2	49	249.1	4.2	49	249.2	4.3	49	251.2	4.5	49	251.4	4.1	49	251.7	3.8	49	251.7	3.8
50	249.6	5.8	50	250.5	5.3	50	249.3	5.5	50	249.5	5.3	50	250.6	5.6	50	251.2	5.6	50	250.3	5.5	50	250.7	5.2	50	250.7	5.2
51	249.4	4.4	51	248.8	4.1	51	251.3	4.4	51	251.7	4.2	51	250.0	4.3	51	249.3	4.3	51	247.9	4.3	51	249.5	4.3	51	249.5	4.3
52	250.8	5.6	52	250.1	5.5	52	251.7	5.5	52	250.4	5.3	52														