Current knowledge on the TJ-65nm process

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Disclaimer:

Information presented limited by NDA

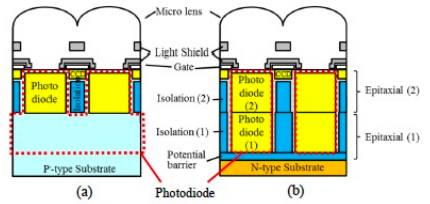
Some technology details

The ISC process

- Various flavours of 65nm at TJ,
  we start with the one devoted to « sensor » (i.e. ISC)
- 5 metal layers available
  - 4 thin + 1 thicker
- Sensitive layer:
  - thin ~10 µm,
  - p-type, high resistivity ⇨ usual n-type collection node
- Modification with shallow N-layer available
  - Continuous, with gaps, …
- Deep n-wells available
  - OK for complex functionalities in pixel
- 2D stitching available over 12" wafers

Questions

- Could we get more metal layers ?
  - May require to move to another flavour (RF, high-density logic) but then: price? Sensitive layer?
- Other non-usual options
  - Stacked photodiode (deep-n within P-trenches)



- Can we get other starting material? (not clear)
  - Always mentioned but not much info…
  - Thicker ones? interest depends on pixel-size required by appli.
  - If new material => re-optimization needed!!

About stitching (a pedestrian understanding point of view)

- Observations
  - Only group in "our domain" with stitching experience = STFC-RAL
    - Their sensors have < 10 transistors/pixel
  - Our current MAPS embeds > 50 transistors/pixels

- Issue one = Failure or yield
  - Failure = small defects somewhere takes down the entire functionality (chip-killing defects)
  - Mitigated by layout precautions

- Issue two = specific Rules
  - Stitching is about repeating blocks, but there are boundary conditions…

- Issue Three = Power
  - Of course, as usual, power rises with (nb of pixels) x (power/pixel)
  - Additional difficulty with long transmission line (power drop)
  - Power regulation probably mandatory